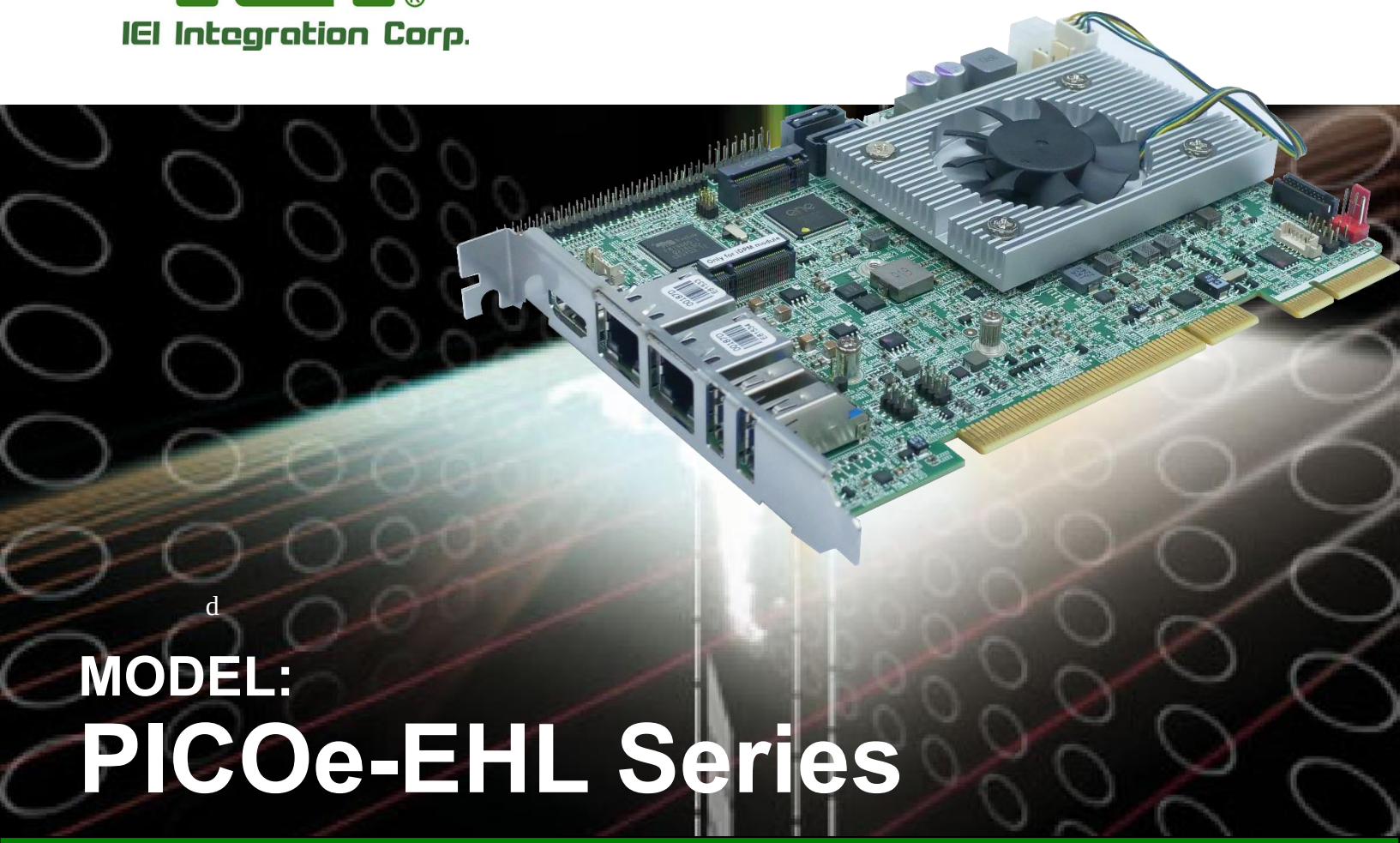
IEI Integration Corp.



d

MODEL:

PICOe-EHL Series

Half-size PCIe CPU Card supports Intel® Elkhart Lake Processor Intel® Celeron® J6412 on-board SoC, with 8GB LPDDR4x memory on board default, DDR4, HDMI, iDPM display module, Dual Lan, USB 3.2, SATA 6Gb/s, M.2, iAUDIO and RoHS

User Manual

Rev. 1.00 - November 13, 2023

RoHS Lead Free

Revision

Date	Version	Changes
November 13, 2023	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Introduction

1.1 Introduction

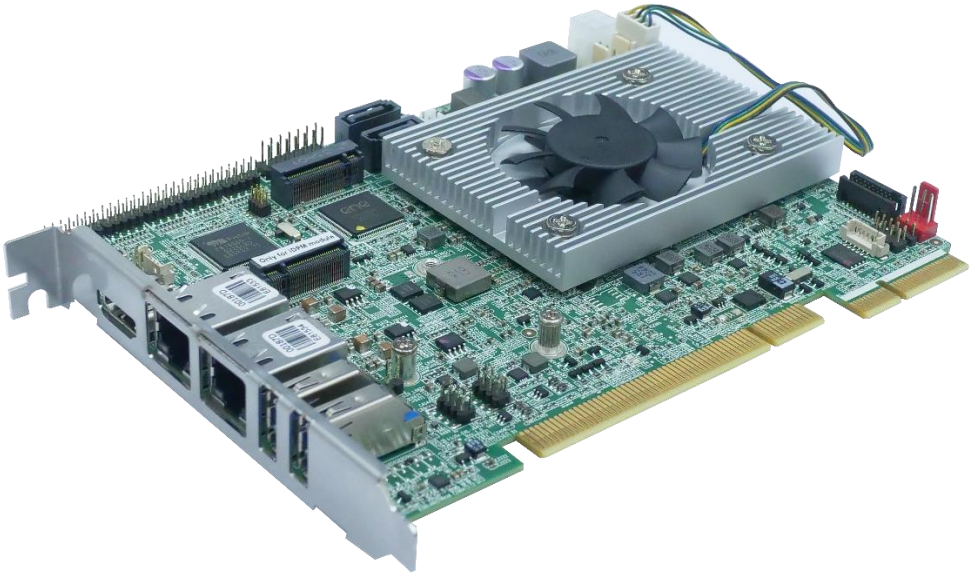


Figure 1-1: PICOe-EHL

The PICOe-EHL is a Half-size PCIe CPU Card equipped with an Intel® Celeron® J6412 quad-core Elkhart Lake processor, turbo up-to 2.60 GHz with 1.5M cache, and onboard LPDDR4x-3200MHz with 8 GB memory, up to 16GB.

The PICOe-EHL includes a HDMI1.4 (up to 4096 x 2160@30Hz) connector and one IEI iDPM slot for double independent display.

Expansion and I/O include one M.2 M-key slot for NVME storage, 1 x PCIe x4 (1 x PCIe x4 or 4 x PCIe x1) and 4 x PCI signal to the backplane. Two USB 3.2 Gen2 on the rear panel, four USB 2.0 connectors by pin header. Two SATA 6Gb/s connectors are also included for connecting with storage devices. Serial device connectivity is provided by internal two RS-232/422/485 and two RS-232 pin header. Two RJ-45 GbE connectors provide the system with smooth connections to an external LAN.

1.2 Features

Some of the PICOe-EHL motherboard features are listed below:

- 10nm Intel® Celeron® J6412 on-board SoC, 4 cores and 4 threads, base frequency 2.00GHz, turbo frequency up to 2.60GHz, 1.5MB cache
- Two Intel® I210 2.5GbE ports
- Two USB 3.2 Gen 2, four USB 2.0, two RS-232/422/485, two RS-232
- M.2 M key, 1 x PCIe x4 (1 x PCIe x4 or 4 x PCIe x1) and 4 x PCI signal to the backplane
- Support double independent display via HDMI and IEI iDPM

1.3 Connectors

The connectors on the PICOe-EHL are shown in the figure below.

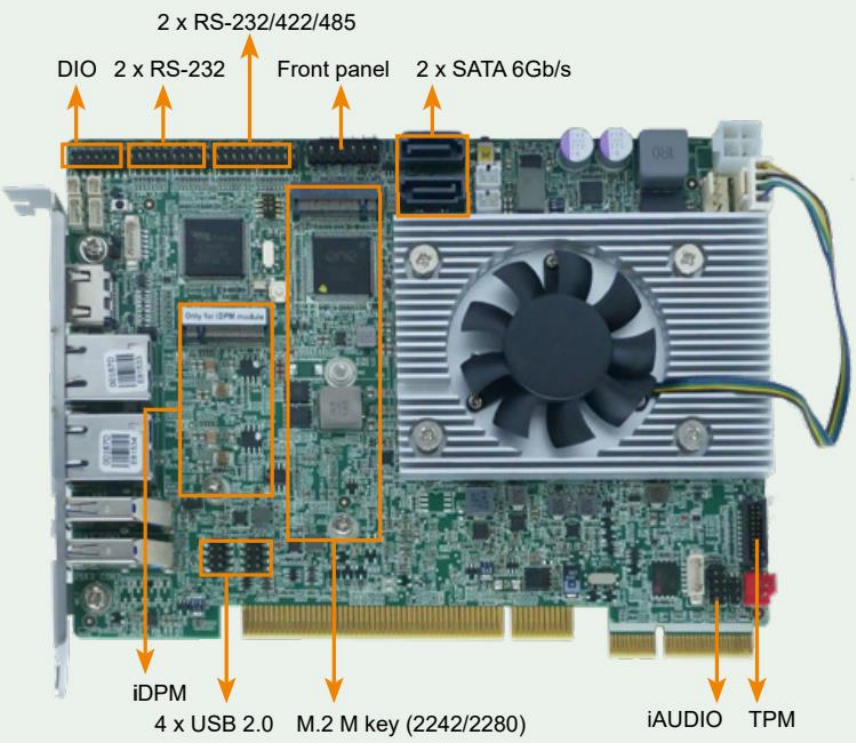


Figure 1-2: Connectors

1.4 Dimensions

The dimensions of the board are listed below:

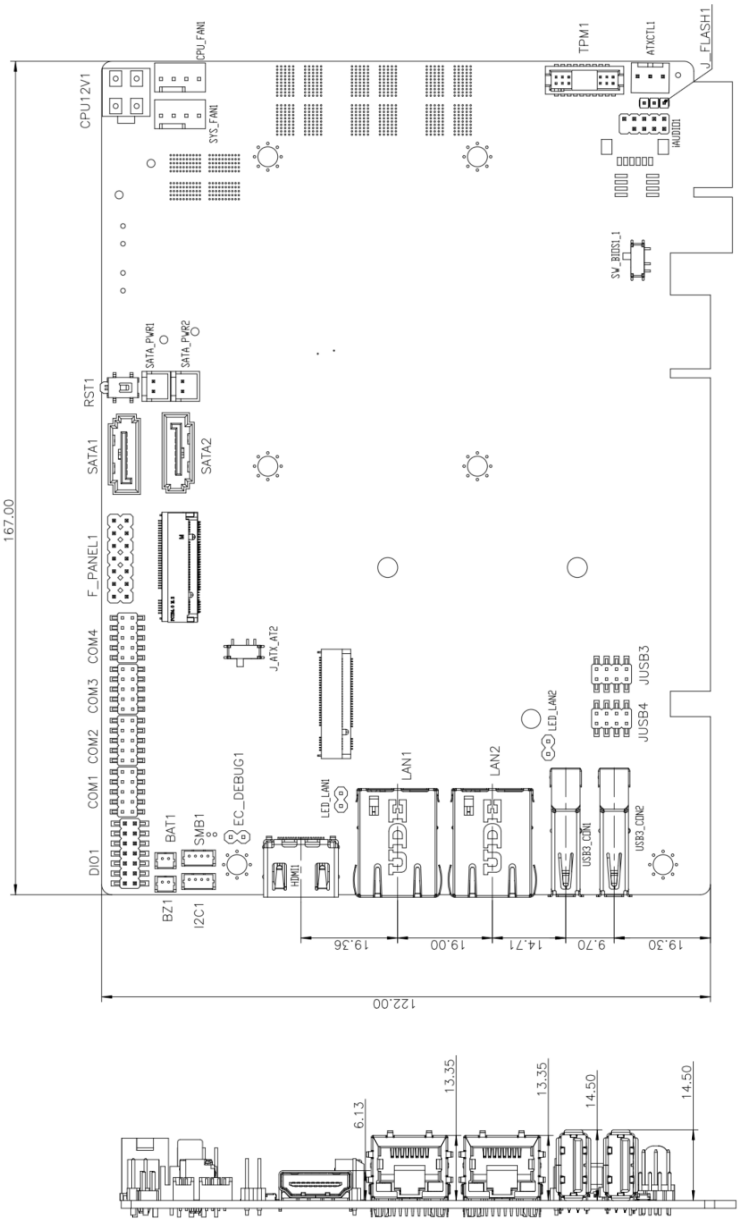


Figure 1-3: Dimensions (mm)

1.5 Data Flow

Shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

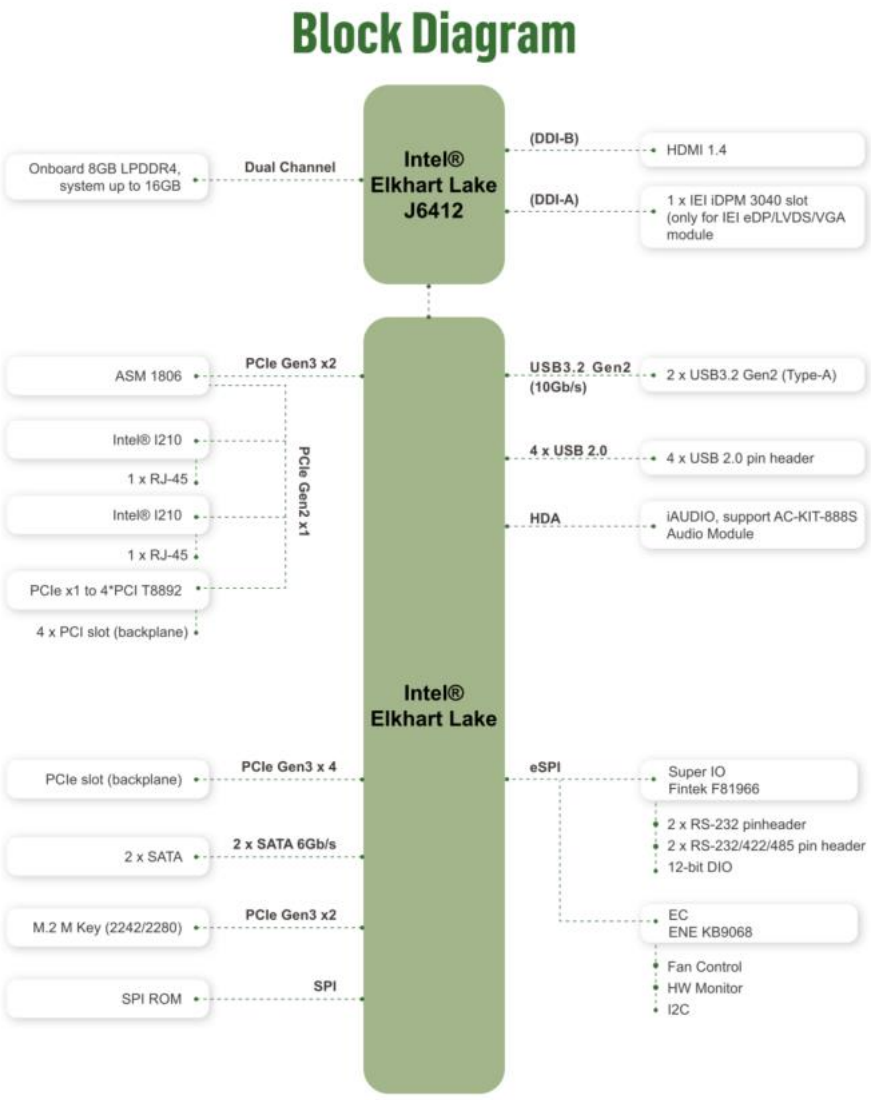


Figure 1-4: Data Flow Diagram

1.6 Technical Specifications

PICOe-EHL technical specifications are listed below.

Specification	PICOe-EHL
SoC	Intel® Elkhart Lake Processor Intel® Celeron® J6412 on-board SoC (up to 2.6GHz, quad-core, 1.5M Cache, TDP=10W)
BIOS	AMI UEFI BIOS
Memory	On-board LPDDR4x 3200 MHz 8GB, up to 16 GB
Graphics	Intel® UHD Graphics
Display Output	Double independent display 1 x HDMI 1.4 (up to 4096 x 2160@30Hz) 1 x IEI iDPM 3040 slot (only for IEI eDP/LVDS/VGA module)
Ethernet	LAN1: Intel® I210 controller LAN2: Intel® I210 controller
Digital I/O	12-bit digital I/O by 14-pin (2x7) header
Embedded Controller	ENE KB9068
Watchdog Timer	Software programmable support 1~255 sec. system reset
I/O Interface	
Audio Connector	1 x iAUDIO supports IEI AC-KIT-888S Audio Kit (2x5 pin)
Serial Ports	2 x RS-232/422/485 by 10-pin header (2x5 pin, P=2.0) 2 x RS-232 by 10-pin header (2x5 pin, P=2.0)
USB Ports	2 x USB 3.2 Gen 2 (10Gb/s) on rear I/O 4 x USB 2.0 by 8-pin (2x4 pin, P=2.0) header
Front Panel	1 x Front Panel (2 x 7 pin, Power LED, HDD LED, Speaker, Power Button, Reset Button)
Fan	1 x CPU fan connector (1x4 pin) 1 x System fan connector (1x4 pin)

Specification	PICOe-EHL
SMBus/I²C	1 x I²C connector by 4-pin (1x4) wafer 1 x SMBus connector by 4-pin (1x4) wafer
Storage	2 x SATA 6Gb/s with 5V SATA power connector
Expansions	1 x M.2 M Key (2242/2280, PCIe x2) NVMe support 1 x PCIe x4 (1 x PCIe x4 or 4 x PCIe x1) to the backplane 4 x PCI to the backplane
Environmental and Power Specifications	
Power Supply	12 V DC input only (AT/ATX support)
Power Connector	1 x Internal power connector by 4-pin (2x2) connector
Power Consumption	5V@ 6.39A, 5VSB@ 0.22A, 12V@ 0.96A (Intel® Celeron® J6412 CPU with 8 GB 3200 MHz LPDDR4x memory, max. loading, EuP mode enabled)
Operating Temperature	0°C ~ 60°C
Storage Temperature	-20°C ~ 70°C
Humidity	5% ~ 95%, non-condensing
Physical Specifications	
Dimensions	185 mm x 126 mm
Weight GW/NW	Weight GW:1000g / NW:420g

Table 1-1: Technical Specifications

Chapter

2

Unpacking

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the PICOe-EHL is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

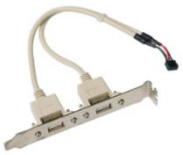
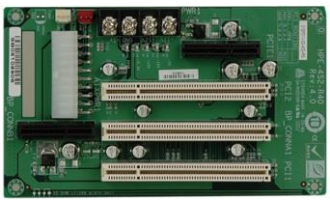
If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the PICOe-EHL was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The PICOe-EHL is shipped with the following components:

Quantity	Item and Part Number	Image
1	PICOe-EHL single board computer	
1	SATA with power cable kit	
1	Quick Installation Guide	

Table 2-1: Packing List

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual-port USB 2.0 cable, 210mm, P=2.0 (**P/N** : CB-USB02A-RS)	
RS-232 cable, 200 mm, p=2.0 (P/N : 32205-002700-200-RS)	
Audio kit, 7.1 Channel (P/N: AC-KIT-888S-R10)	
eDP to eDP DisplayPort converter board (for IEI iDPM connector) (P/N: iDPM-eDP-R10)	
eDP to LVDS DisplayPort converter board (for IEI iDPM connector) (P/N: iDPM-LVDS-R10)	
eDP to VGA Connetor converter board (For IEI Display Module) (P/N: iDPM-VGA-R10)	
PCI/PCI Express Backplane with 1 PCI, 1 PCIe x4 Slots (P/N: HPE-3S2-R41)	
PCI/PCI Express Backplane with 2 PCI, 1 PCIe x4 Slots (P/N: HPE-4S2-R41)	

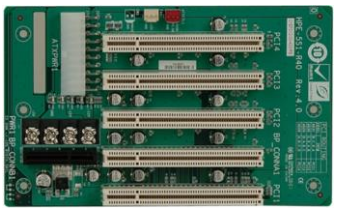
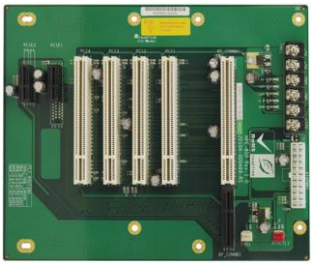
PCI/PCI Express Backplane with 4 PCI Slots,RoHS (P/N: HPE-5S1-R51)	
PCI/PCI Express Backplane with 4 PCI, 2 PCIe x1 Slots,RoHS (P/N: HPE-8S0-R41)	

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 PICOe-EHL Layout

The figures below show all the connectors and jumpers.

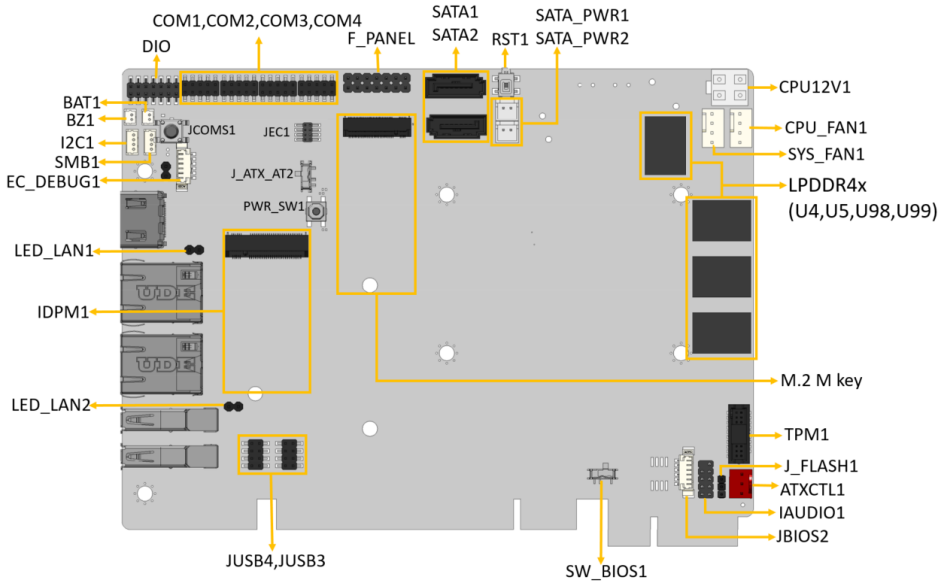


Figure 3-1: Connector and Jumper Locations

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
Clear CMOS button	Button	J_CMOS1
AT/ATX power mode setting	Switch	J_ATX_AT2
Flash descriptor override setting jumper	3-pin header	J_FLASH1
Audio connector for IEI AC-KIT-888S kit	10-pin header	AUDIO1
ATX 12V power connector	4-pin Molex	CPU12V1
Battery connector	2-pin wafer	BAT1
Buzzer connector	2-pin wafer	BZ1
Digital I/O connector	14-pin header	DIO1
CPU Fan connector	4-pin header	CPU_FAN1
System Fan connector	4-pin header	SYS_FAN1
Power LED & HDD LED connector	14-pin wafer	F_PANEL1
Power button connector	Button	PWR_SW1
Reset button	Switch	RST1
RS-232/422/485 serial port connectors	10-pin header	COM3, COM4
RS-232 serial port connectors	10-pin header	COM1, COM2
SATA 6Gb/s connectors	7-pin SATA connector	SATA1, SATA2
SATA power connector	2-pin wafer	SATA_PWR1 SATA_PWR2
I2C connector	4-pin wafer	I2C1
SMBus connector	4-pin wafer	SMB1

Flash SPI ROM connector	6-pin wafer	JBIOS2
Flash EC ROM connector	8-pin header	JEC1
EC debug connector	6-pin wafer	EC_DEBUG1
Internal USB 2.0 connector	8-pin header	JUSB3, JUSB4
M.2 M-key slot	M.2 M-key slot	M2_M1
IEI IDPM slot	IEI Defined Idpm slot	IDPM1
TPM Module connector	19-pin header	TPM1

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
External GbE RJ-45 connectors	RJ45	LAN1, LAN2
External USB 3.2 Gen 2 Type-A connectors	USB 3.2 Gen 2 Type-A	USB3_CON1, USB3_CON2
External HDMI connector	HDMI	HDMI1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the PICOe-EHL.

3.2.1 Clear CMOS Button

CN Label: **J_CMOS1**

CN Type: Button

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

To clear the CMOS Setup (for example if you have forgotten the password, you should clear the CMOS and then reset the password), you should disconnect the RTC battery and press the button for about 3 seconds. This will set back to normal operation mode.

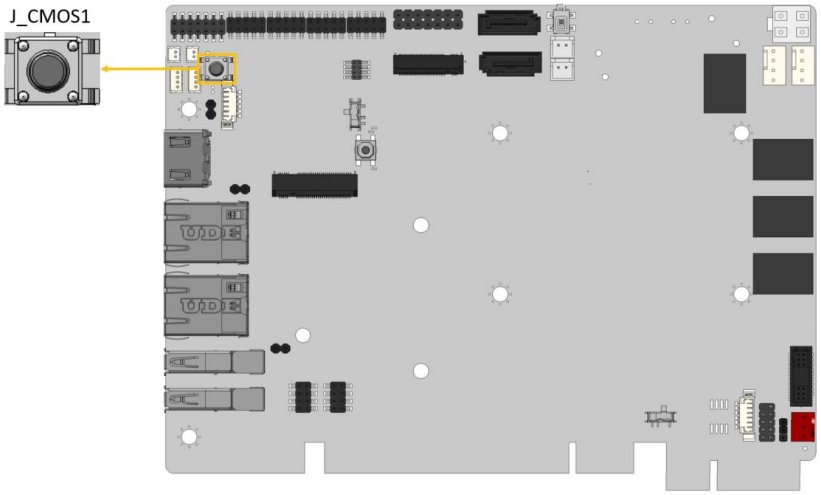


Figure 3-2: Clear CMOS Location

PIN NO.	DESCRIPTION
NC (default)	Keep CMOS Setup (Normal Operation)
Press button	Clear CMOS Setup

Table 3-3: Clear CMOS Pinouts

3.2.2 AT/ATX Power Mode Setting

CN Label: **J_ATX_AT2**

CN Type: Switch

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

The AT/ATX power mode selection is made through the AT/ATX power mode switch which is shown in Figure3-3.

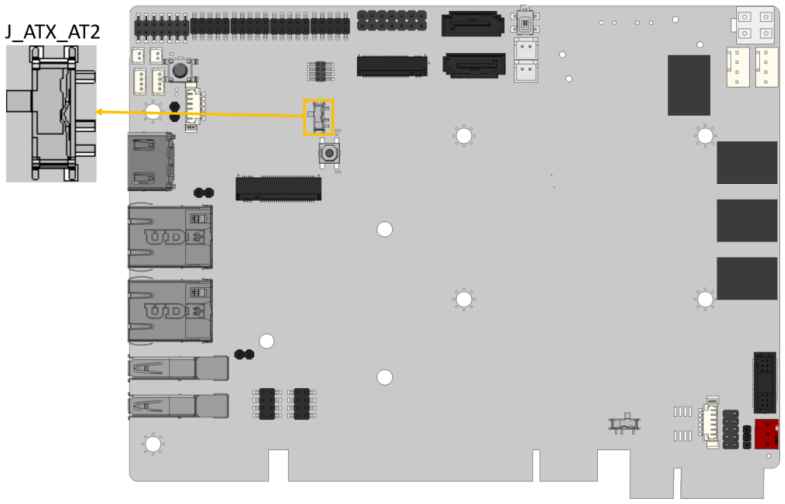


Figure 3-3: AT/ATX Power Mode Switch Location

Setting	Description
Short A-B	ATX power mode (default)
Short B-C	AT power mode

Table 3-4: AT/ATX Power Mode Switch Settings

3.2.3 BIOS1/BIOS2 Select Switch

CN Label:	**SW_BIOS1_1**
CN Type:	Switch
CN Location:	See **Figure 3-3**
CN Pinouts:	See **Table 3-4**

Use the switch to chose BIOS1 or BIOS2.

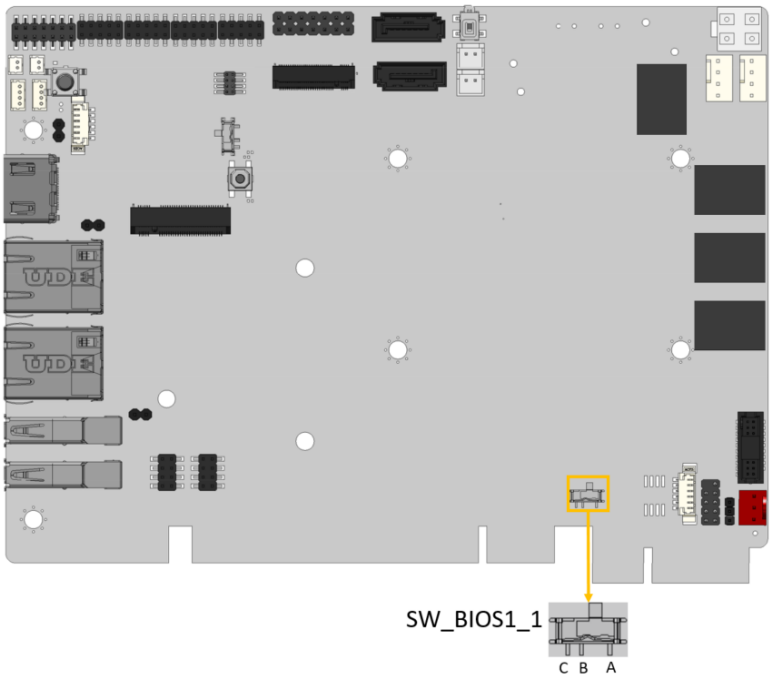


Figure 3-4: BIOS1/BIOS2 Select Switch Location

Setting	Description
Short A-B	BIOS1 (default)
Short B-C	BIOS2

Figure 3-5: BIOS1/BIOS2 Select Switch Settings

3.2.4 Flash Descriptor Override Setting Jumper

CN Label:	**J_FLASH1**
CN Type:	3-pin header,P=2.00mm
CN Location:	See **Figure 3-6**
CN Pinouts:	See **Table 3-5**

The J_FLASH1 connector is used for Flash Descriptor Security Overide .

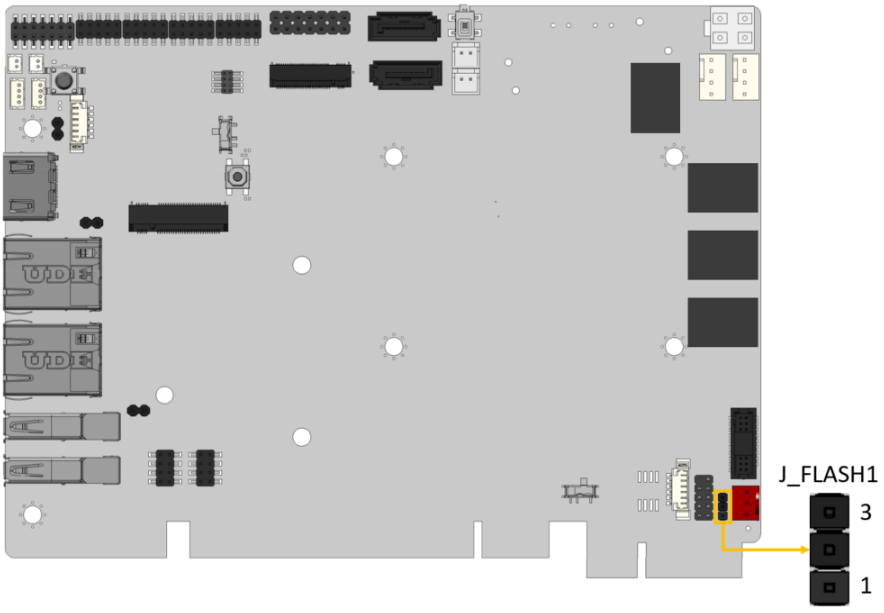


Figure 3-6: Flash Descriptor Override Setting Jumper Locations

PIN NO.	DESCRIPTION
Short 1 - 2	Disable (default)
Short 2 - 3	Enable

Table 3-5: Flash Descriptor Override Setting Jumper Pinouts

To update the ME firmware, please follow the steps below.

Step 1: Before turning on the system power, short the Flash Descriptor Security Override jumper.

Step 2: Update the BIOS and ME firmware, and then turn off the system power.

Step 3: Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting.

Step 4: Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

3.2.5 Internal Audio Connector

CN Label:	**IAUDIO1**
CN Type:	10-pin header, p=2.00 mm
CN Location:	See **Figure 3-7**
CN Pinouts:	See **Table 3-6**

The audio connector is connected to external audio devices (AC-KIT-888S-R10) including speakers and microphones for the input and output of audio signals to and from the system.

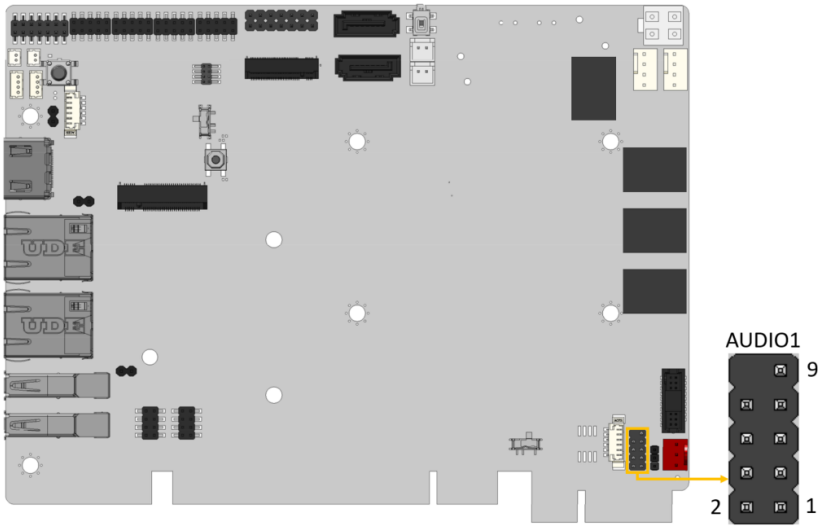


Figure 3-7: Audio Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	HDA_SYNC	2	HDA_CLK
3	HDA_SDOUT	4	HDA_SPKR
5	HDA_SDIN	6	HDA_RST#
7	+5V	8	GND
9	+12V	10	GND

Table 3-6:Audio Connector Pinouts

3.2.6 ATX 12V Power Connector

CN Label: **CPU12V1**

CN Type: 4-pin Molex, p=4.2 mm

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-7**

The connector supports the +12V power supply.

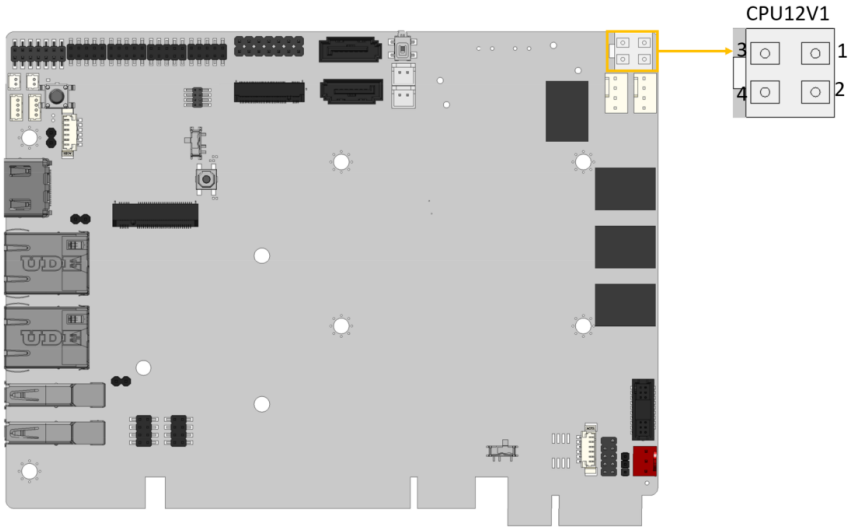


Figure 3-8: 12V Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	+12V	4	+12V

Table 3-7: 12V Power Connector Pinouts

3.2.7 RTC Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the PICOe-EHL is installed.

CN Label:	**BAT1**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-9**
CN Pinouts:	See **Table 3-8**

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

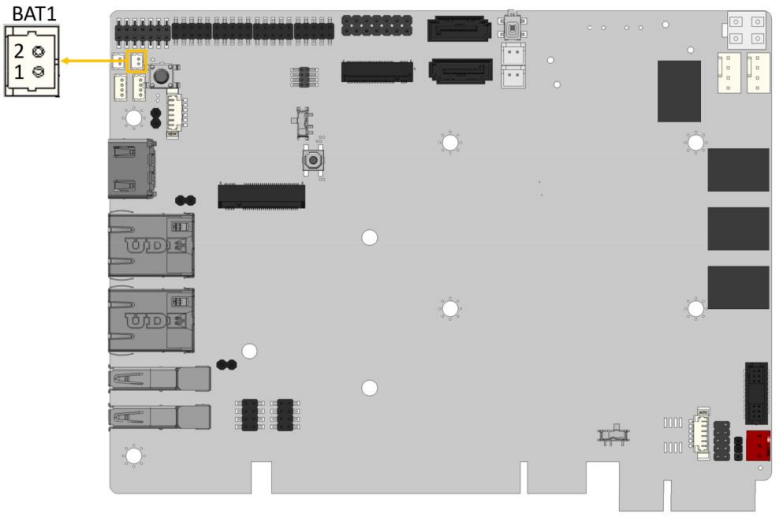


Figure 3-9: Battery Connector Location

Pin	Description
1	VBATT
2	GND

Table 3-8: Battery Connector Pinouts

3.2.8 Buzzer Connector

CN Label: **BZ1**

CN Type: 2-pin wafer, p=1.25 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-9**

The buzzer conector is connected with the buzzer to give a beep warning when the motherboard goes wrong.

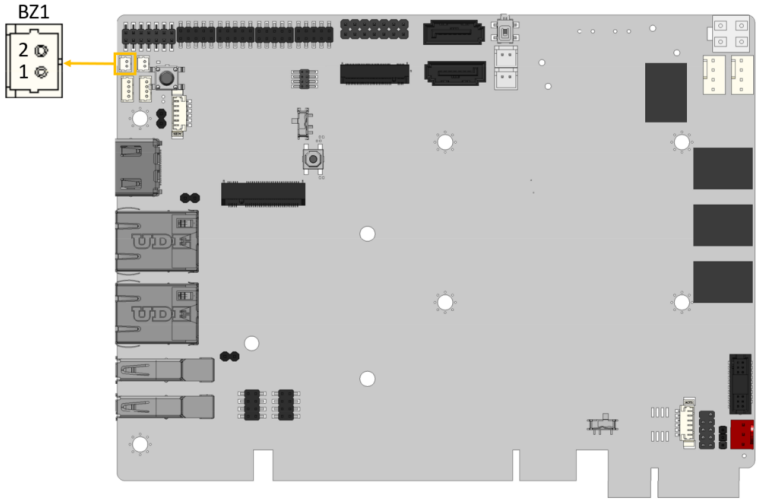


Figure 3-10: Buzzer Connector Location

Pin	Description
1	+5V
2	PC_BEEP

Table 3-9: Buzzer Connector Pinouts

3.2.9 Digital Input/Output Connector

CN Label: **DIO1**

CN Type: 14-pin header, p=2.0 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-10**

The 12-bit digital I/O connector provides programmable input and output for external devices.

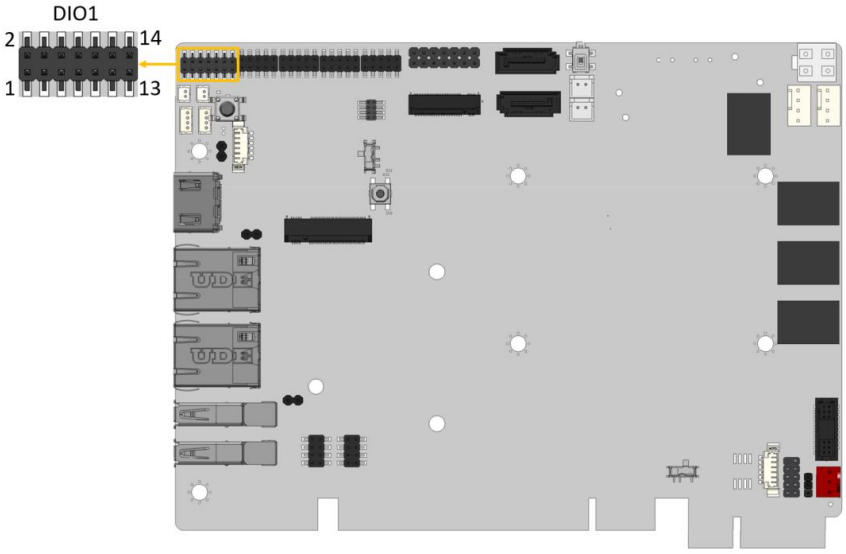


Figure 3-11: Digital I/O Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	VCC
3	DOUT5	4	DOUT4
5	DOUT3	6	DOUT2
7	DOUT1	8	DOUT0
9	DIN5	10	DIN4
11	DIN3	12	DIN2
13	DIN1	14	DIN0

Table 3-10: Digital I/O Connector Pinouts

3.2.10 CPU Fan Connector

CN Label: **CPU_FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-11**

The fan connector attaches to a smart cooling fan.

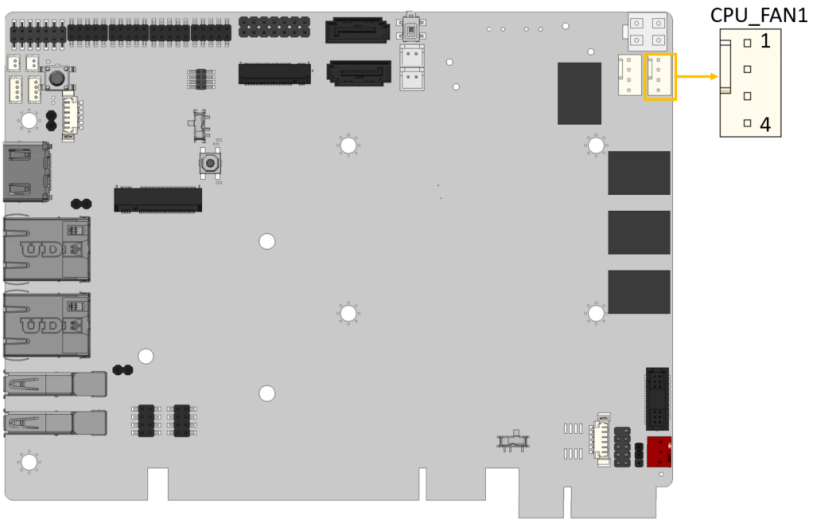


Figure 3-12: CPU Fan Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	3	FANIO
2	+12V	4	PWM

Table 3-11: CPU Fan Connector Pinouts

3.2.11 System Fan Connector

CN Label: **SYS_FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-12**

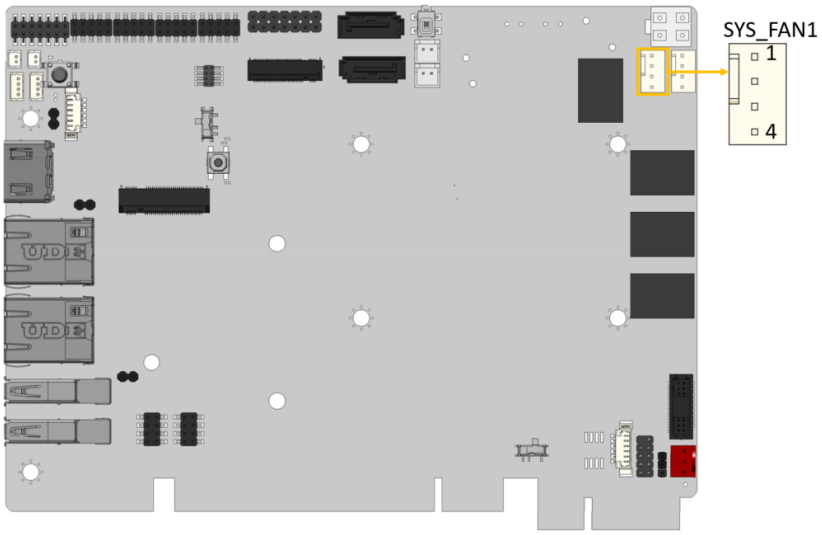


Figure 3-13: System Fan Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	3	FANIO
2	+12V	4	PWM

Table 3-12: System Fan Connector Pinouts

3.2.12 Power LED & HDD LED Connector

CN Label: **F_PANEL1**

CN Type: 14-pin header, p=2.00 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-13**

The front panel connector connects to the power LED indicator and HDD LED indicator on the system front panel.

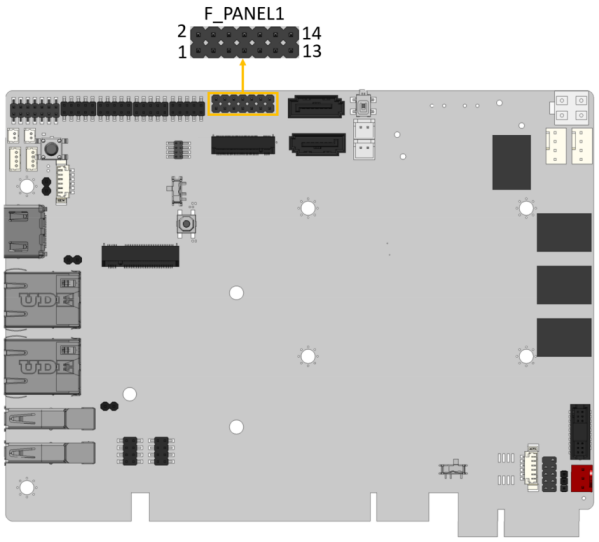


Figure 3-14: Power LED & HDD LED Connector Location

Pin	Description	Pin	Description
1	PWR_LED+	2	SPKR+
3	NC	4	NC
5	PWR_LED-	6	NC
7	PWR_BTN+	8	SPKR-
9	PWR_BTN-	10	NC
11	HDD_LED+	12	Reset+
13	HDD_LED-	14	Reset-

Table 3-13: Power LED & HDD LED Connector Pinouts

3.2.13 Power Button Connector

CN Label: **PWR_SW1**

CN Type: 2-pin wafer, p=2.00 mm

CN Location: See **Figure 3-15**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

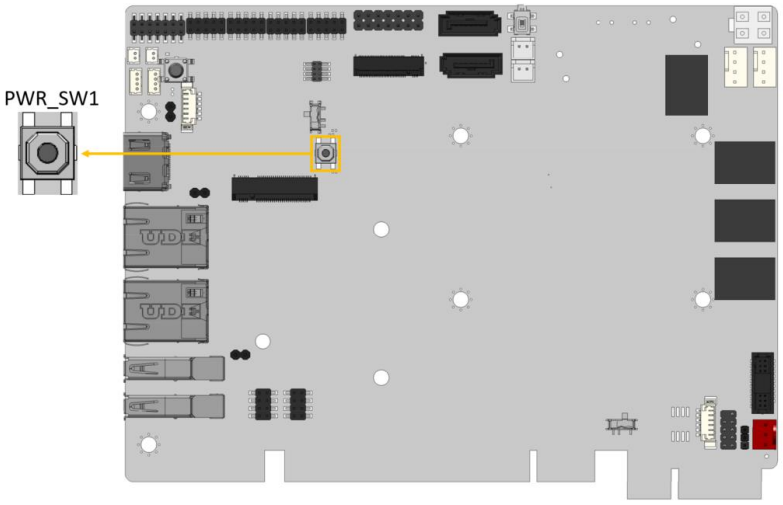


Figure 3-15: Power Button Connector Location

3.2.14 Reset Button

CN Label: **RST1**

CN Type: Button

CN Location: See **Figure 3-16**

The reset button allows users to reboot the system when the system is turned on.

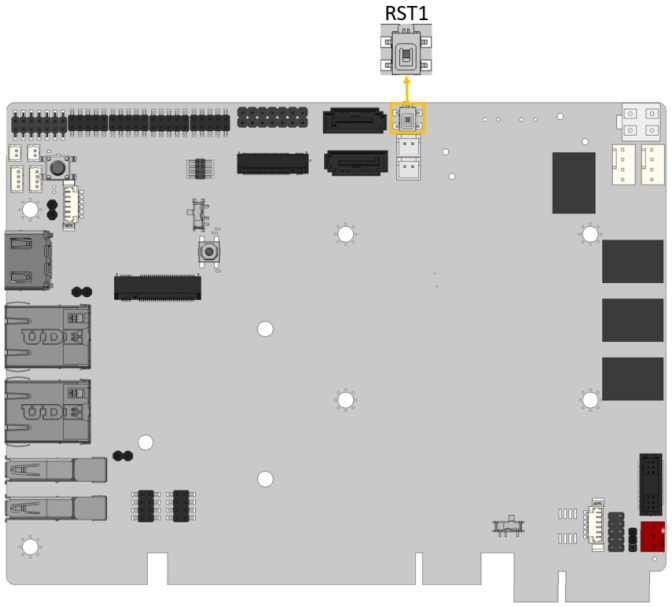


Figure 3-16: Reset Button Connector Location

3.2.15 RS-232/422/485 Serial Port Connector

CN Label:	**COM3, COM4**
CN Type:	10-pin header, p=2.0 mm
CN Location:	See **Figure 3-17**
CN Pinouts:	See **Table 3-14**

The serial connector provides RS-232/422/485 connection.

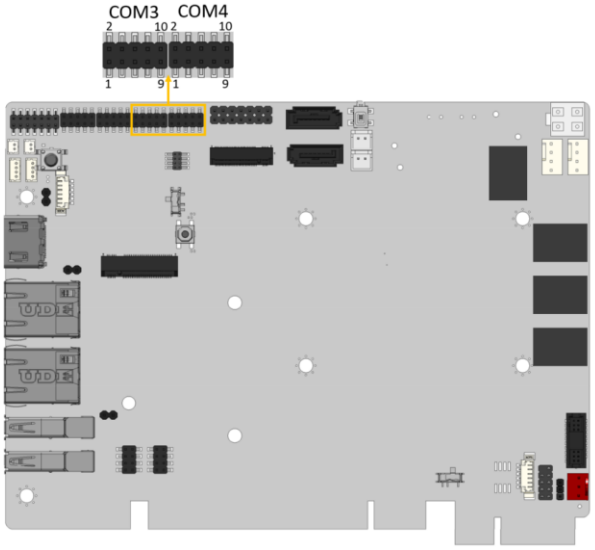
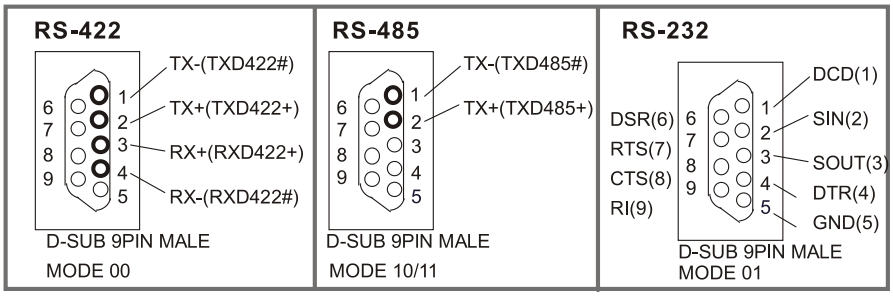


Figure 3-17: RS-232/422/485 Serial Port Connector Location



Pin	RS-232	RS-422	RS-485
1	DCD	TXD422-	TXD485-
2	RXD	TXD422+	TXD485+
3	TXD	RXD422+	
4	DTR	RXD422-	
5	GND		

Pin	RS-232	RS-422	RS-485
6	DSR		
7	RTS		
8	CTS		
9	RI		

Table 3-14: RS-232/422/485 Serial Port Connector Pinouts

3.2.16 RS-232 Serial Port Connector

CN Label: **COM1, COM2**

CN Type: 10-pin header, p=2.0 mm

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-15**

The serial connector provides RS-232 connection.

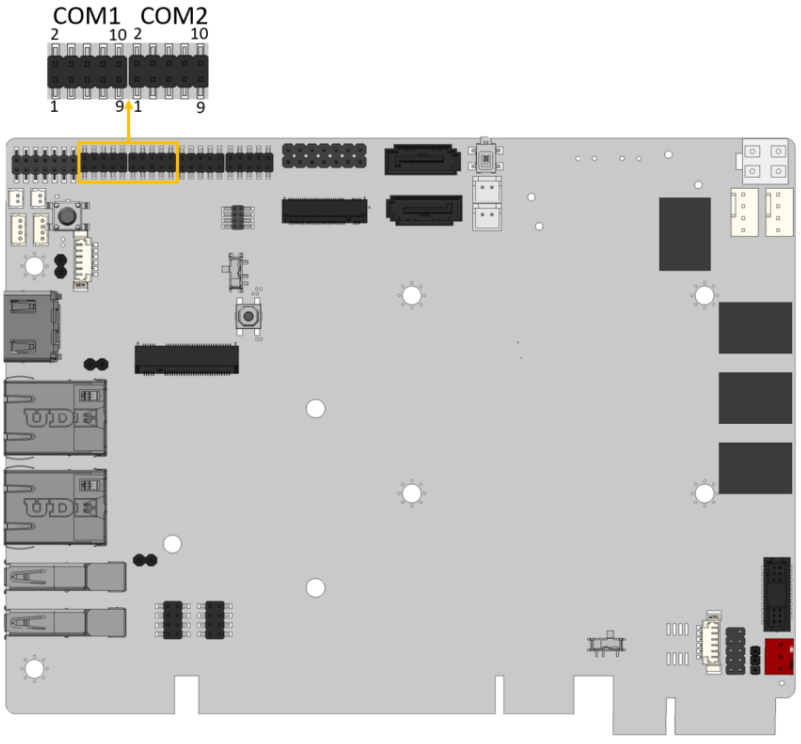


Figure 3-18: RS-232 Serial Port Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	GND

Table 3-15: RS-232 Serial Port Connector Pinouts

3.2.17 SATA 6Gb/s Drive Connector

CN Label: **SATA1, SATA2**

CN Type: 7-pin SATA connector

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-16**

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

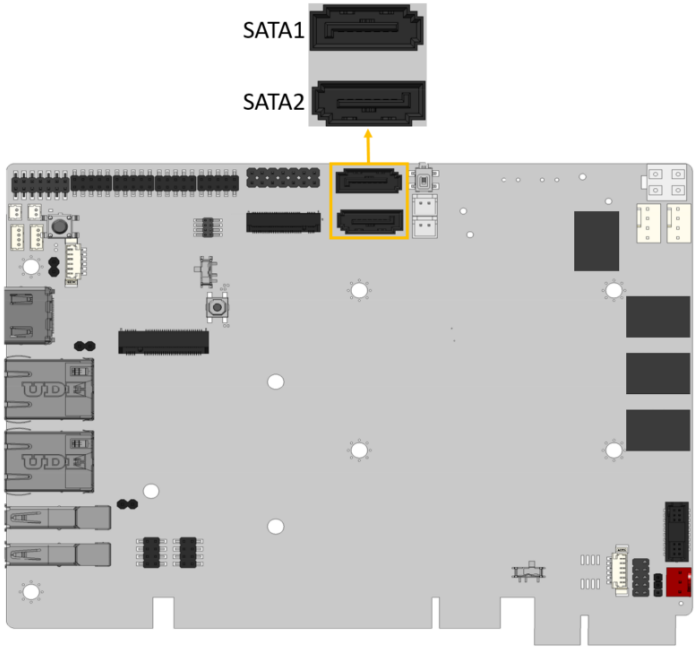


Figure 3-19: SATA 6Gb/s Drive Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	5	SATA_RX-
2	SATA_TX+	6	SATA RX+
3	SATA_TX-	7	GND
4	GND		

Table 3-16: SATA 6Gb/s Drive Connectors Pinouts

3.2.18 SATA Power Connector

CN Label: **SATA_PWR1,SATA_PWR2**

CN Type: 2-pin wafer, p=2.00 mm

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-17**

The SATA power connector provides +5 V power output to the SATA connector.

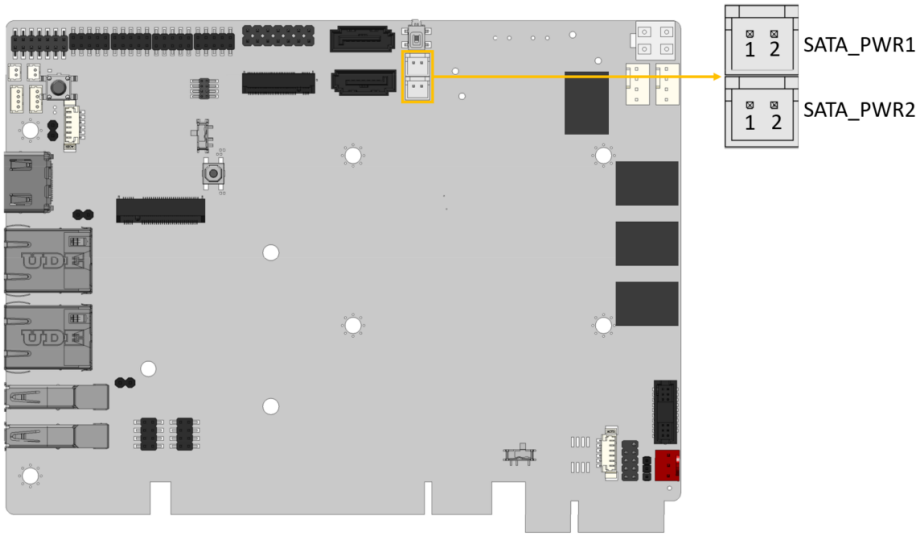


Figure 3-20: SATA Power Connector Location

Pin	Description
1	+5V
2	GND

Table 3-17: SATA Power Connector Pinouts

3.2.19 I²C Connector

CN Label:	**I2C1**
CN Type:	4-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-21**
CN Pinouts:	See **Table 3-18**

The I2C connector provides low-speed system management communications.

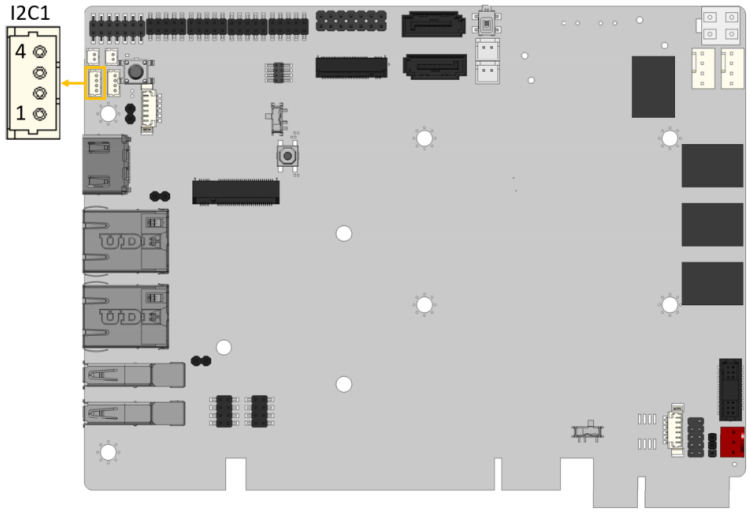


Figure 3-21: I²C Connector Location

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-18: I² C Connector Pinouts

3.2.20 SMBus Connector

CN Label: **SMB1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-19**

The SMBus is a two-wire bus used for communication with low bandwidth devices on a motherboard such as power related chips and temperature sensors.

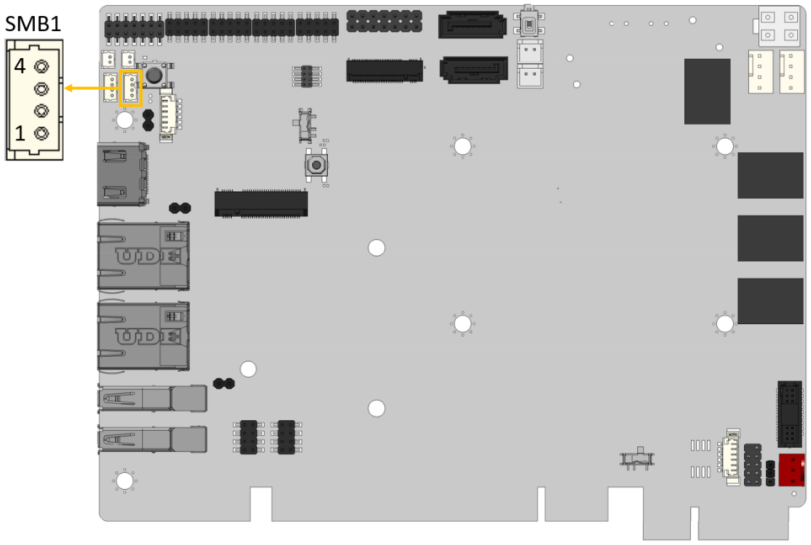


Figure 3-22: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-19: SMBus Connector Pinouts

3.2.21 Flash SPI ROM Connector

CN Label: **JBIOS2**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-20**

The 6-pin Flash SPI ROM connector is used to flash the BIOS.

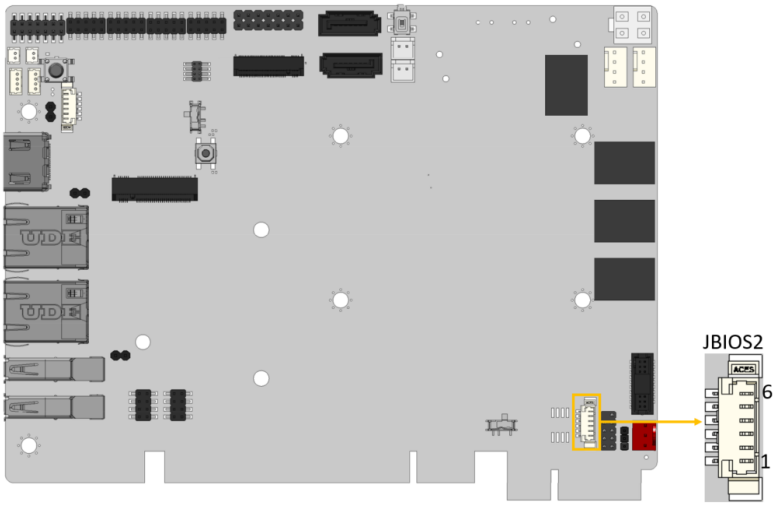


Figure 3-23: Flash SPI ROM Connector Location

Pin	Description
1	+3.3V
2	SPI_CS#
3	SPI SO
4	SPI CLK
5	SPI SI
6	GND

Table 3-20: Flash SPI ROM Connector Pinouts

3.2.22 Flash EC ROM Connector

CN Label:	**JEC1**
CN Type:	8-pin header, p=1.27 mm
CN Location:	See **Figure 3-24**
CN Pinouts:	See **Table 3-21**

The 6-pin Flash EC ROM connector is used to flash the EC internal ROM.

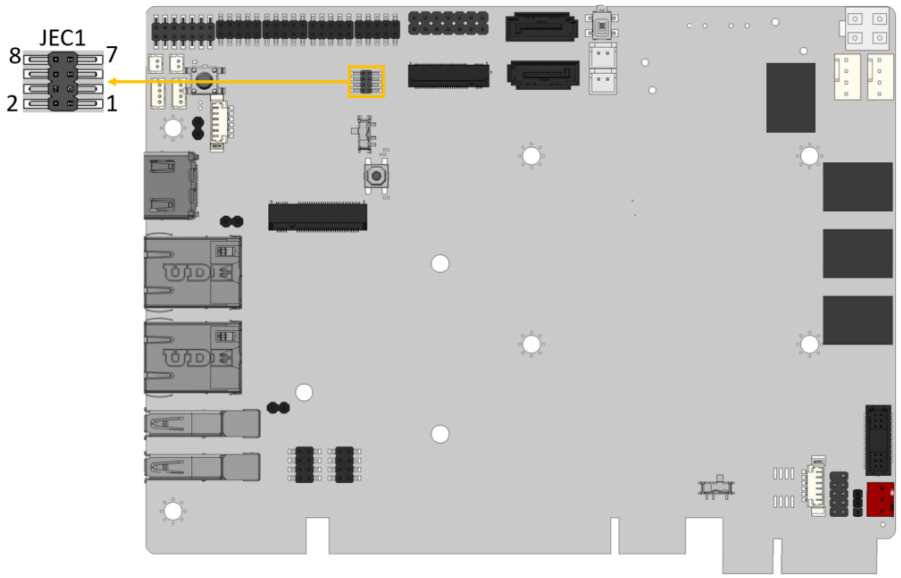


Figure 3-24: Flash EC ROM Connector Location

Pin	Description	Pin	Description
1	CS#_EC	2	+3.3V
3	SO_EC	4	HOLD#_EC
5	EC_DET_FLASH	6	SCK_EC
7	GND	8	SIO_EC

Table 3-21: Flash EC ROM Connector Pinouts

3.2.23 EC Debug Connector

CN Label: **EC_DEBUG1**

CN Type: 6-pin header, p=1.25 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-22**

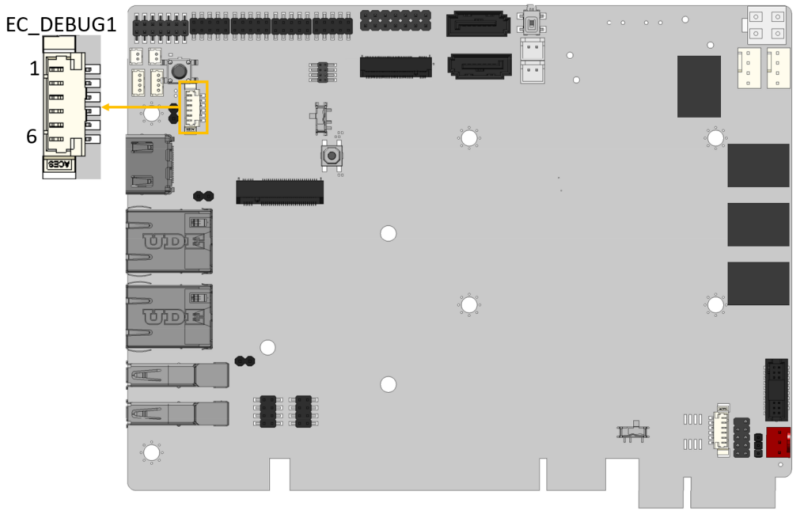


Figure 3-25: EC Debug Connector Location

Pin	Description	Pin	Description
1	NC	2	EDICLK
3	EDICS	4	EDIDI
5	EDIDO	6	GND

Table 3-22:EC Debug Connector Pinouts

3.2.24 Internal USB 2.0 Connectors

CN Label: **JUSB3, JUSB4**

CN Type: 8-pin header, p=2.00 mm

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-23**

Each USB connector provides two USB 2.0 ports by dual-port USB cable.

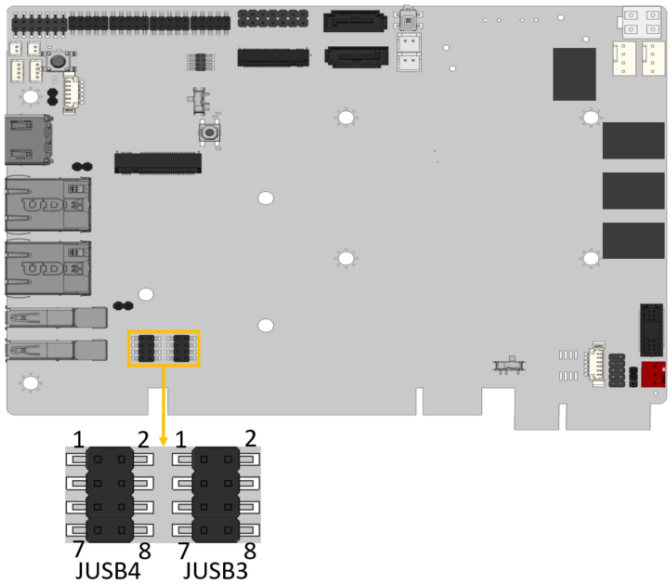


Figure 3-26: Internal USB 2.0 Connectors Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	USB DATA-	4	USB DATA+
5	USB DATA+	6	USB DATA-
7	GND	8	VCC

Table 3-23: Internal USB 2.0 Connectors Pinouts

3.2.25 M.2 M-key Slot

CN Label: **M2_M1**

CN Type: M.2 B-key slot

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-24**

The M.2 M key (2242/2280) slot with PCIe Gen3 x2 signal supports NVMe storage.

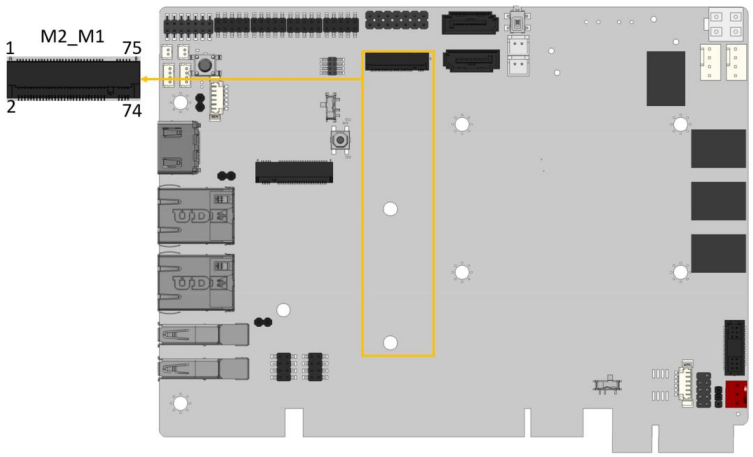


Figure 3-27: M.2 M-key Slot Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+V3.3
3	GND	4	+V3.3
5	NC	6	NC
7	NC	8	NC
9	GND	10	NC
11	NC	12	+V3.3
13	NC	14	+V3.3
15	GND	16	+V3.3
17	NC	18	+V3.3
19	NC	20	NC
21	GND	22	NC
23	NC	24	NC
25	NC	26	NC
27	GND	28	NC
29	PCIE_1_RX_DN	30	NC
31	PCIE_1_RX_DP	32	NC
33	GND	34	NC
35	PCIE_1_TX_DN	36	NC
37	PCIE_1_TX_DP	38	MKEY_SSD_SLP
39	GND	40	M2_I2C_CLK2
41	PCIE_0_RX_DN	42	M2_I2C_DAT2
43	PCIE_0_RX_DP	44	NC

45	GND	46	NC
47	PCIE_0_TX_DN	48	NC
49	PCIE_0_TX_DP	50	SLOT_RST
51	GND	52	NC
53	PCIE_CLK_DN	54	NC
55	PCIE_CLK_DP	56	NC
57	GND	58	NC
59	Module Key	60	Module Key
61	Module Key	62	Module Key
63	Module Key	64	Module Key
65	Module Key	66	Module Key
67	NC	68	NC
69	M2_IFDET2_N	70	+V3.3
71	GND	72	+V3.3
73	GND	74	+V3.3
75	GND		

Table 3-24: M. 2 M-key Slot Pinouts

3.2.26 iDPM Slot

CN Label: **IDPM**

CN Type: iDPM slot

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-25**

The iDPM slot is only for IEI eDP/LVDS/VGA module

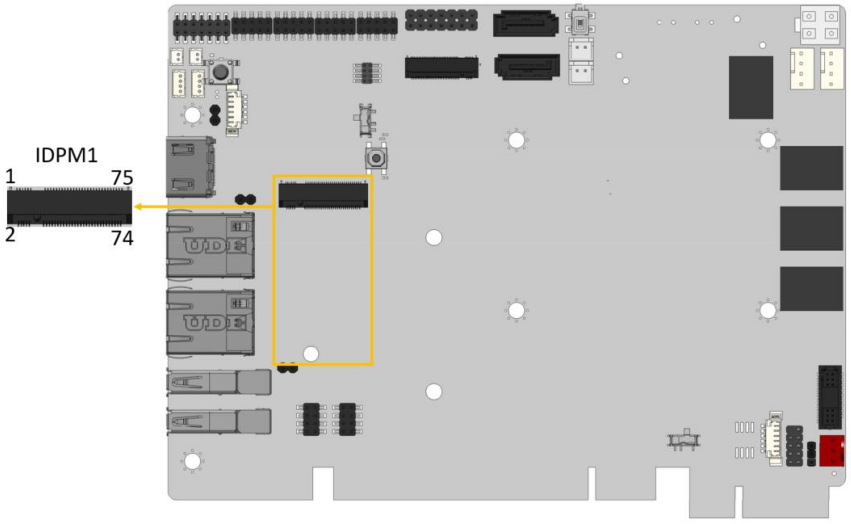


Figure 3-28: IDPM Slot Location

Pin	Description	Pin	Description
1	GND	2	+3.3V
3	GND	4	+3.3V
5	GND	6	+3.3V
7	GND	8	+3.3V
9	GND	10	+3.3V
11	+5V	12	Module Key
13	Module Key	14	Module Key
15	Module Key	16	Module Key
17	Module Key	18	Module Key
19	Module Key	20	+3.3VS
21	DISPLAY_DETECT_PIN21	22	+3.3VS

Pin	Description	Pin	Description
23	DISPLAY_DETECT_PIN23	24	+3.3VS
25	GND	26	+3.3VS
27	GND	28	GND
29	EDP_TX3_DN	30	+12VS
31	EDP_TX3_DP	32	+12VS
33	GND	34	+12VS
35	EDP_TX2_DN	36	+12VS
37	EDP_TX2_DP	38	GND
39	GND	40	SMB_CLK
41	EDP_TX1_DN	42	SMB_DATA
43	EDP_TX1_DP	44	GND
45	GND	46	EC_BKLT_CTRL
47	EDP_TX0_DN	48	EDP1_BKLT_CTRL
49	EDP_TX0_DP	50	EDP1_BKLT_EN
51	GND	52	EDP1_VDD_EN #
53	EDP_AUX_DN	54	EDP_HPD_R
55	EDP_AUX_DP	56	BUF_PLT_RST#
57	GND	58	LVDS_EN
59	GND	60	+V5S
61	GND	62	+V5S
63	GND	64	+V5S
65	GND	66	+V5S
67	GND	68	+12VA
69	GND	70	+12VA
71	GND	72	+12VA
73	GND	74	+12VA
75	GND		

Table 3-25: iDPM Connector Pinouts

3.2.27 TPM Module Connector

CN Label: **TPM1**

CN Type: 19-pin header, p=1.27 mm

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-26**

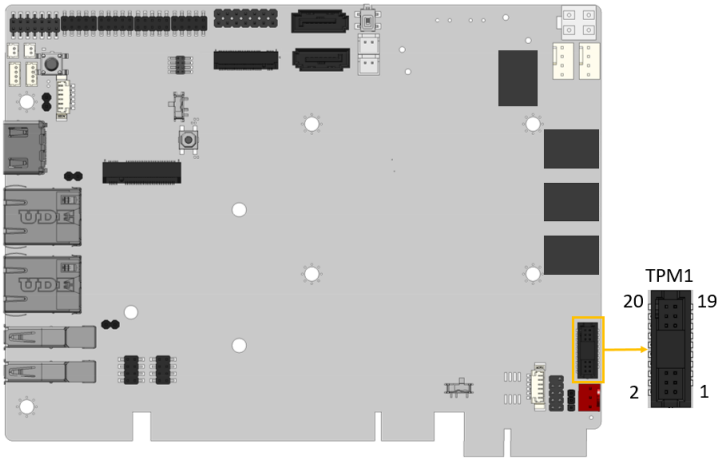


Figure 3-29: TPM Connector Location

Pin	Description	Pin	Description
1	NC	2	TPM_SPI_CS0_N
3	DEDI_PROG_RST_N	4	TPM_SPI_CS1_N
5	GND	6	+V3P3A
7	SPI_CLK_TPM	8	SPI_TPM_DQ2
9	TPM_SPI_DQ3	10	TPM_SPI_MISO
11	SPI_TPM_HOLD_R_N	12	TPM_SPI_MOSI
13	SPI_TPM_CS2_R	14	GND
15	TPM_WP#	16	NC
17	SPI_TPM_INT_N	18	+V3.3A_1.8A_SPI_CON
19	PLT_RST_N	20	+V3.3A_1.8A_SPI_CON

Table 3-26: TPM Connector Pinouts

3.3 External Peripheral Interface Connector Panel

Figure 3-30 shows the PICOe-EHL external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 1 x HDMI connector
- 2 x GbE RJ-45 connector
- 2 x USB 3.2 Gen 2 connector

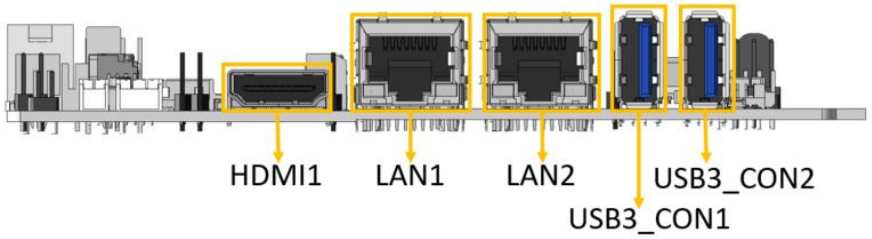


Figure 3-30: External Peripheral Interface Connector

3.3.1 External GbE RJ-45 Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-30**

CN Pinouts: See **Table 3-27**

The LAN connector connects to a local network.

Pin	Description	Pin	Description
1	MDI0P	5	MDI2P
2	MDI0N	6	MDI2N
3	MDI1P	7	MDI3P
4	MDI1N	8	MDI3N

Table 3-27: External GbE RJ-45 Connectors Pinouts

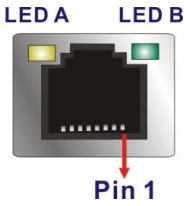


Figure 3-31: LAN LED Location

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received	B	off: 10 Mb/s orange: 100 Mb/s green: 1000 Mb/s

Table 3-28: LAN LED Pinouts

3.3.2 External HDMI Connector

CN Label: **HDMI1**

CN Type: HDMI connector

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-29**

The HDMI connectors can connect to HDMI devices.

Pin	Description	Pin	Description
1	HDMI2_DATA2	2	GND
3	HDMI2_DATA2#	4	HDMI2_DATA1
5	GND	6	HDMI2_DATA1#
7	HDMI2_DATA0	8	GND
9	HDMI2_DATA0#	10	HDMI2_CLK
11	GND	12	HDMI2_CLK#
13	N/C	14	N/C
15	HDMI2_SCL	16	HDM2I_SDA
17	GND	18	+5V
19	HDMI2_HPD		

Table 3-29: External HDMI Connector Pinouts

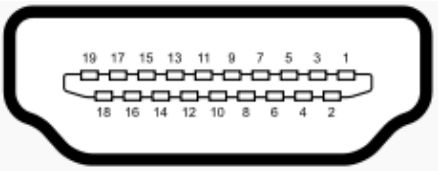


Figure 3-32: External HDMI Connector Location

3.3.3 External USB 3.2 Gen 2 Connectors

CN Label:	**USB3_CON1, USB3_CON2**
CN Type:	USB 3.2 Gen 2 port Type-A
CN Location:	See **Figure 3-33**
CN Pinouts:	See **Table 3-30**

The PICOe-EHL has two external USB 3.2 Gen 2 ports. The USB connector can be connected to a USB 2.0 or USB 3.2 device. The pinouts of USB 3.2 Gen 2 connectors are shown below.

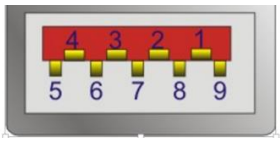


Figure 3-33: External USB 3.2 Gen 2 Connectors Location

Pin	Description	Pin	Description
1	VCC	2	USB_DATA0-
3	USB_DATA0+	4	GND
5	USB3_RX0-	6	USB3_RX0+
7	GND	8	USB3_TX0-
9	USB3_TX0+		

Table 3-30: External USB 3.2 Gen 2 Connectors Pinouts

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the PICOe-EHL may result in permanent damage to the PICOe-EHL and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the PICOe-EHL. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the PICOe-EHL or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding*** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the PICOe-EHL, place it on an anti-static pad. This reduces the possibility of ESD damaging the PICOe-EHL.
- ***Only handle the edges of the PCB***: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the PICOe-EHL, PICOe-EHL components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the PICOe-EHL installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the PICOe-EHL on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the PICOe-EHL off:
  - When working with the PICOe-EHL, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

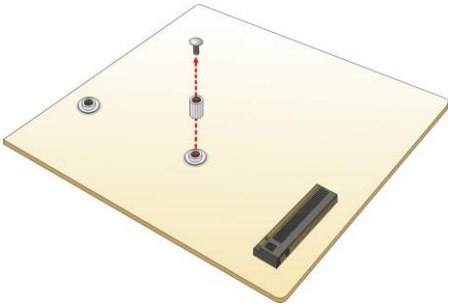
Before and during the installation of the PICOe-EHL **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 M.2 Module Installation

CAUTION:

The standoff and screw pre-installed for the M.2 2242 module must be removed before installing an M.2 2280 module. Failing to do so may cause short circuit or other damges to the motherboard.



To install an M.2 module, please follow the steps below.

Step 1: Locate the M.2 module slot. See **Chapter 3**.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º (**Figure 4-1)**.

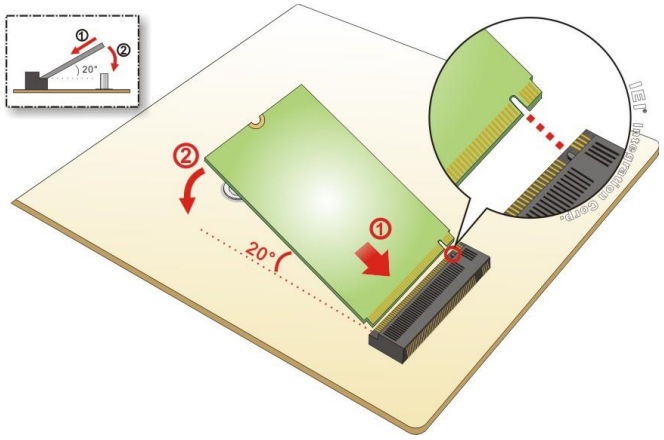


Figure 4-1: Inserting The M.2 Module Into The Slot At An Angle

Step 4: Secure the M.2 module with the previously removed retention screw (**Figure 4-2**).

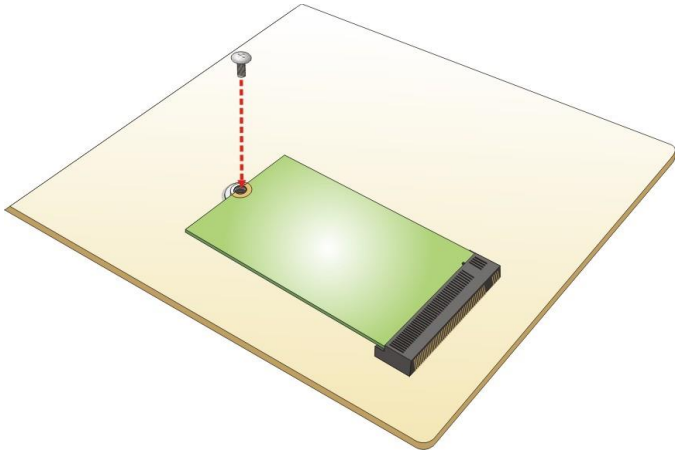


Figure 4-2: Securing The M.2 Module

4.4 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

4.4.1 AT Power Connection

Follow the instructions below to connect the PICOe-EHL to an AT power supply.

WARNING:

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the PICOe-EHL.

Step 1: **Locate the power cable**. The power cable is shown in the packing list in **Chapter 2**.

Step 2: **Connect the power cable to the motherboard**. Connect the 4-pin (2x2) Molex type power cable connector to the power connector on the motherboard. See **Figure 4-3**

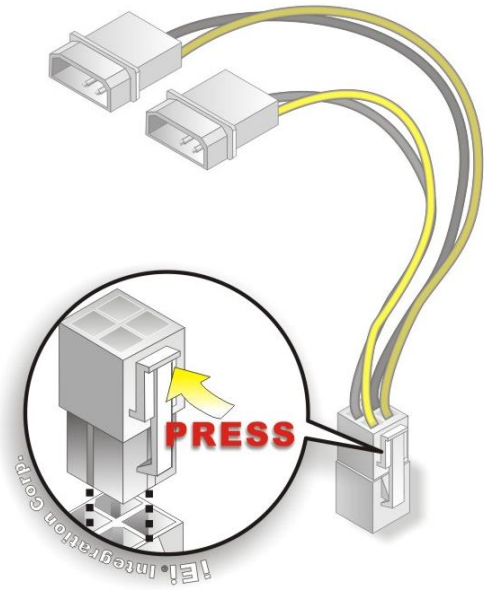


Figure 4-3: Power Cable to Motherboard Connection

Step 3: **Connect power cable to power supply**. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT power supply. See **Figure 4-4**

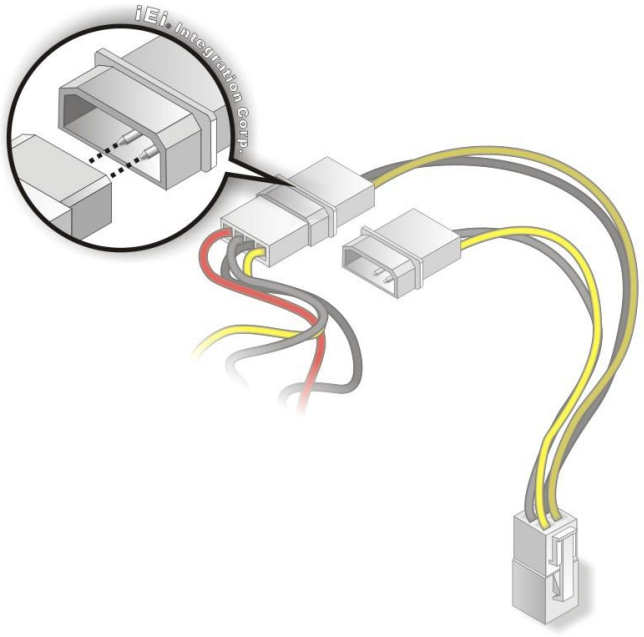


Figure 4-4: Connect Power Cable to Power Supply

4.4.2 7.1 Channel Audio Kit Installation

NOTE:

This item must be ordered separately, and connects to the audio connector. For further information please contact the nearest distributor, reseller or vendor or contact an IEI sales representative directly.

The audio kit attaches to the audio connector. The audio kit provides 7.1 channel audio. To install the audio kit, please refer to the steps below:

Step 1: **Connect the cable to the audio kit.** Connect the included cable to the audio kit. Make sure pin 1 aligns with the marked pin.

Step 2: **Conect the cable to the board**. Connect the other end of the cable to the board. Make sure to line up the marked pin 1.

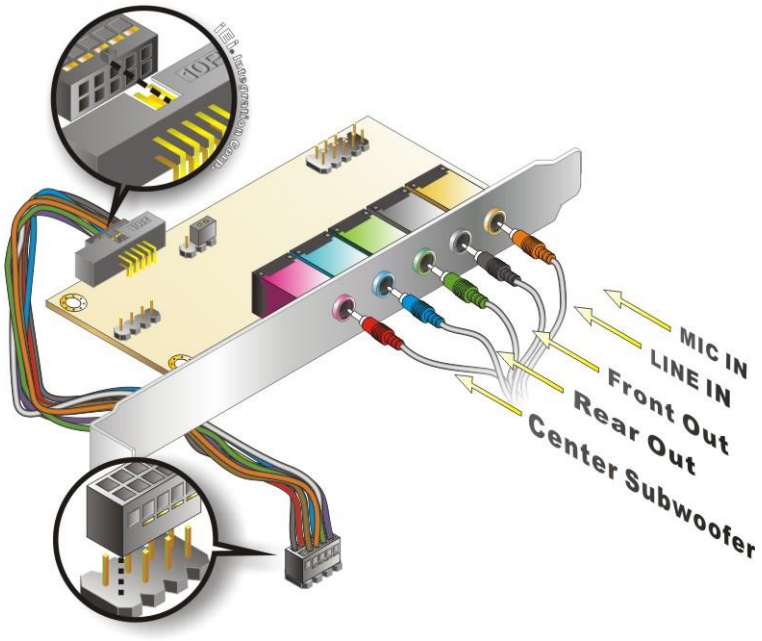


Figure 4-5: 7.1 Channel Audio Kit

Step 3: **Mount the audio kit onto the chassis**. Once the audio kit is connected to the board, secure the audio kit bracket to the system chassis.

Step 4: **Connect the audio devices**. Connect speakers and external audio sources to the audio jacks on the audio kit.

Step 5: **Install the driver**. Install the 7.1 channel audio driver included with the board.

4.4.3 SATA Drive Connection

The PICOe-EHL is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

Step 1: **Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-6**.

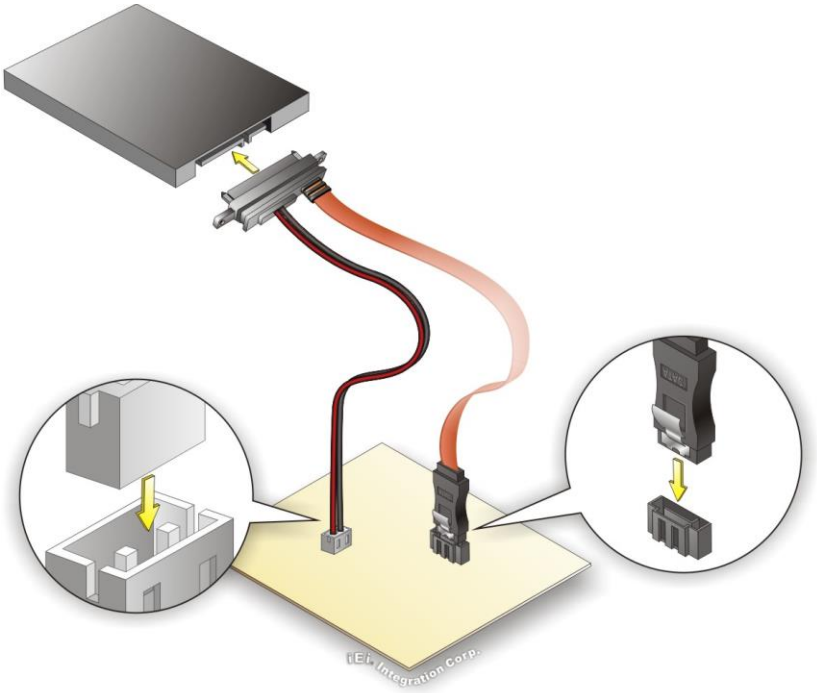


Figure 4-6: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive.

Step 4: To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

4.5 Software Drivers

4.5.1 Available Drivers

All the drivers for the PICOe-EHL are available on IEI Resource Download Center (https://download.ieiworld.com). Type PICOe-EHL and press Enter to find all the relevant software, utilities, and documentation.

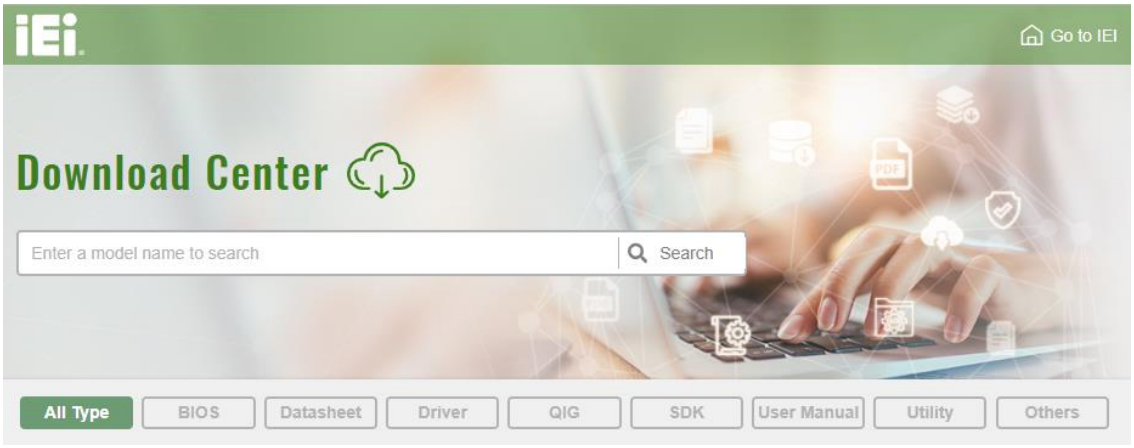
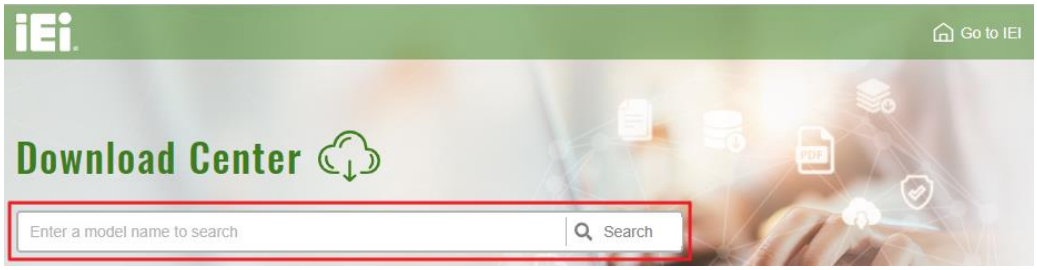


Figure 4-7: IEI Resource Download Center

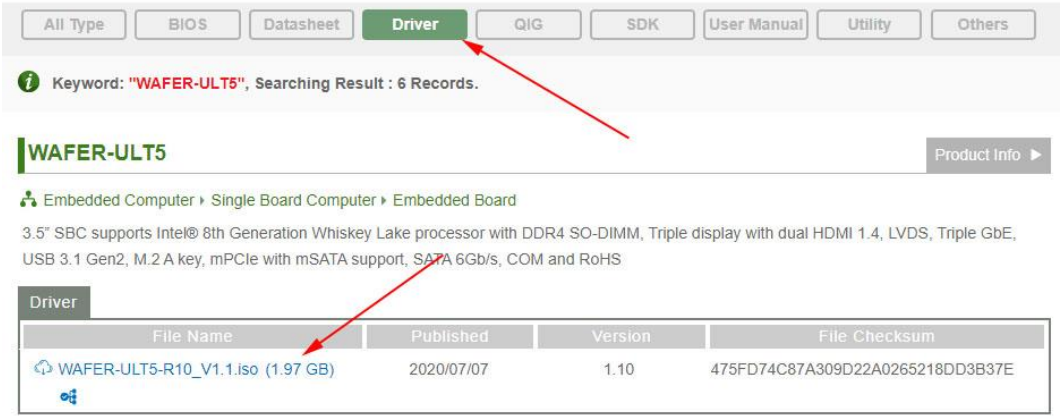
4.5.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

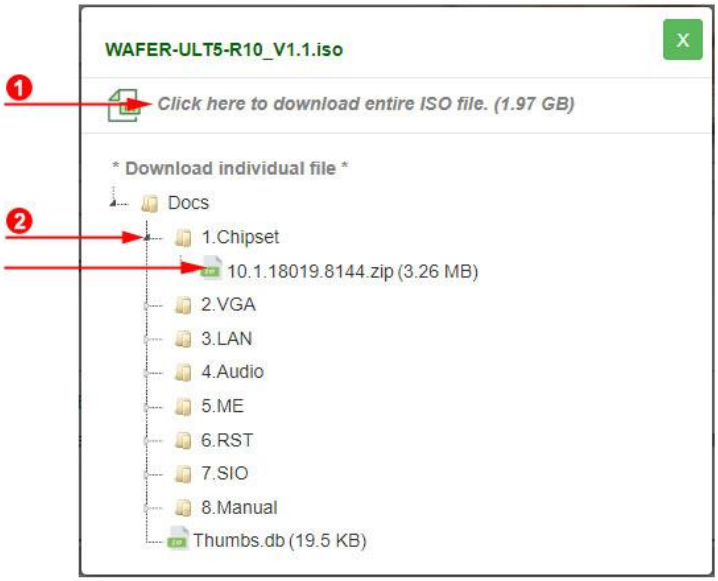
Step 1: Go to https://download.ieiworld.com. Type PICOe-EHL and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard**: Press the **DEL** or **F7** as soon as the system is turned on.
2. **Using touchscreen**: Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL or F7** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

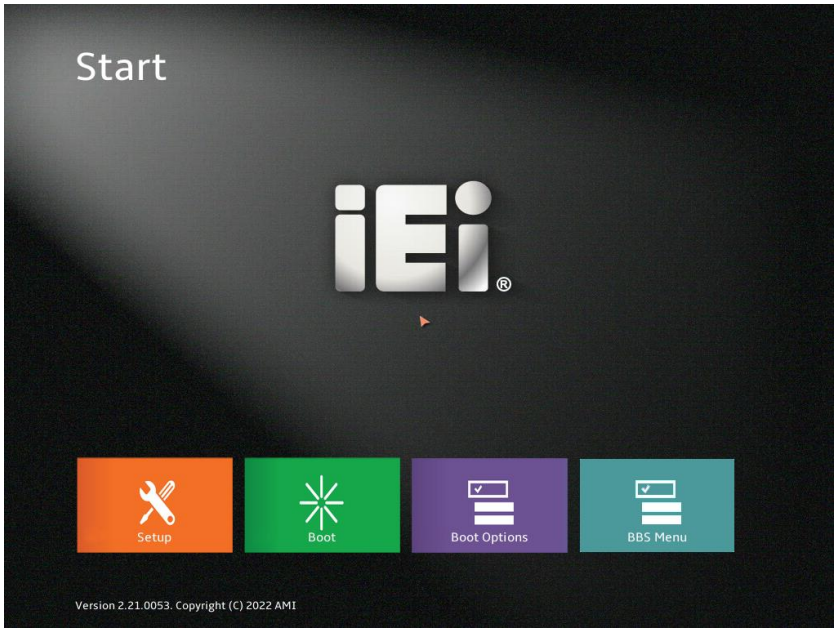


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

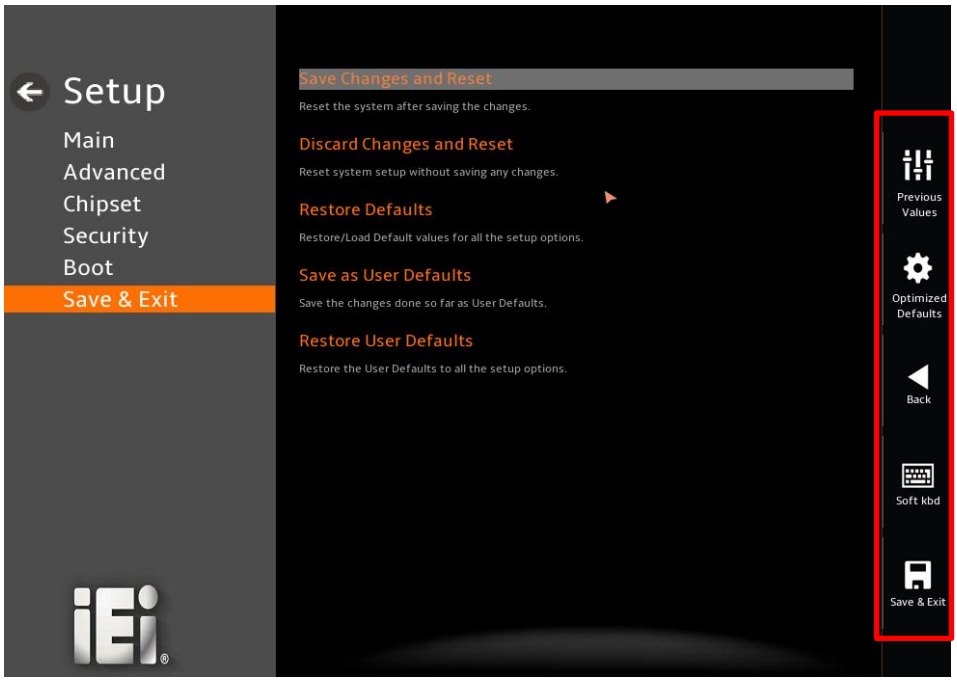
For keyboard navigation, use the navigation keys shown in **Table 5-1**.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

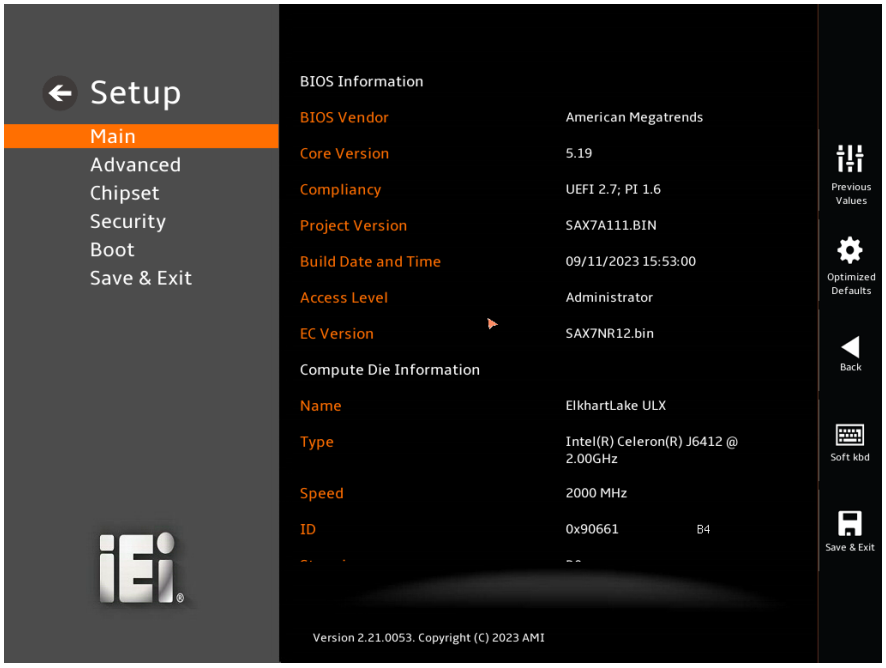
The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1 & BIOS Menu 2**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/2)

BIOS Menu 2: Main (2/2)

➔ **BIOS Information**

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliancy:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **EC Version:** Current EC version
- BIOS Information

➔ **Compute Die Information**

The **Compute Die Information** lists a brief summary of the Processor. The fields in **Compute Die Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the Processor Details
- **Type:** Displays the Processor Type
- **Speed:** Displays the Processor Speed
- **ID:** Displays the Processor ID
- **Stepping:** Displays the Processor Stepping
- **Number of Processors:** Displays number of CPU cores
- **Microcode Revision:** CPU Microcode Revision
- **Total Memory:** Total Memory in the System
- **Memory Data Rate:** Displays the Data Rate of Memory

➔ **PCH Information**

The **PCH Information** lists a brief summary of the PCH. The fields in **PCH Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the PCH Name
- **Stepping:** Displays the PCH Stepping
- **ME FW Version:** Displays the ME Firmware Version
- **ME Firmware SKU:** Displays the ME Firmware SKU

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 3**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

BIOS Menu 3: Advanced

5.3.1 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 4 & BIOS Menu 5 & BIOS Menu 6**) to view detailed CPU specifications or enable the Intel Virtualization Technology.

BIOS Menu 4: CPU Configuration (1/3)

BIOS Menu 5: CPU Configuration (2/3)

BIOS Menu 6: CPU Configuration (3/3)

➔ **Intel (VMX) Virtualization Technology [Enabled]**

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

➔	**Disabled**		Disables Intel Virtualization Technology.
➔	**Enabled**	**DEFAULT**	Enables Intel Virtualization Technology.

➔ **Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

➔	**All**	**DEFAULT**	Enable all cores in the processor package.
➔	**1**		Enable one core in the processor package.
➔	**2**		Enable two cores in the processor package.
➔	**3**		Enable three cores in the processor package.

➔ **EIST [Enable]**

Use the **EIST** option to enable more than two frequency ranges to be supported.

➔	**Disabled**		Disables more than two frequency ranges
➔	**Enabled**	**DEFAULT**	Enables more than two frequency ranges

➔ **C states [Disabled]**

Use the **C states** option to enable or disable the CPU Power Management.

➔	**Disabled**	**DEFAULT**	Disables CPU to go to C states when it's not 100% utilized.
➔	**Enabled**		Enables CPU to go to C states when it's not 100% utilized.

➔ **Tcc Activation Offset [0]**

Use the **Tcc Activation** option to set Tcc activation temprature at which the Thermal Control Circuit must be activated.Tcc will be activated at: Tcc Activation Temp-Tcc Activation Offset. Tcc Activation Offset range is 0 to 63.

➔ **Power Limit 1**

Use the **Power Limit 1** to set Power Limit in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power limit and TDP Limit. If value is 0, BIOS will program TDP value.

➔ **Power Limit 1 Time Window**

Power Limit 1 Time Window value in second. The value may vary from 0 to 128.0, 0 = default value (28 sec for mobile and 8 sec for desktop). Defines time window which TDP value should be maintained.

➔ **Power Limit 2**

Use the **Power Limit 2** to set Power Limit in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

➔ **Turbo Mode [Enabled]**

Use the **Turbo Mode** option to enable or disable Turbo Mode which requires Intel Speed Step or Intel Speed Shift to be available and enabled.

➔	**Disabled**		Disables Turbo Mode Technology
➔	**Enabled**	**DEFAULT**	Enables Turbo Mode Technology

5.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 7**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).

BIOS Menu 7: Trusted Computing

➔ **TPM Support [Enable]**

Use the **TPM Support** option to configure support for the TPM.

- ➔ **Disable** — TPM support is disabled.
- ➔ **Enable** **DEFAULT** — TPM support is enabled.

➔ **TPM Device Selection [PTT]**

Use the **TPM Device Selection** option to chose dPTM or PTT.

- ➔ **dPTM** — Chose to use IEI TPM module.
- ➔ **PTT** **DEFAULT** — Chose Intel® PTT (TPM 2.0).

➔ **Pending Operation [None]**

Use the **Pending Operation** option to schedule an operation for the security device.

➔ **None**	**DEFAULT**	TPM information is same as previous
➔ **TPM Clear**		TPM information is cleared

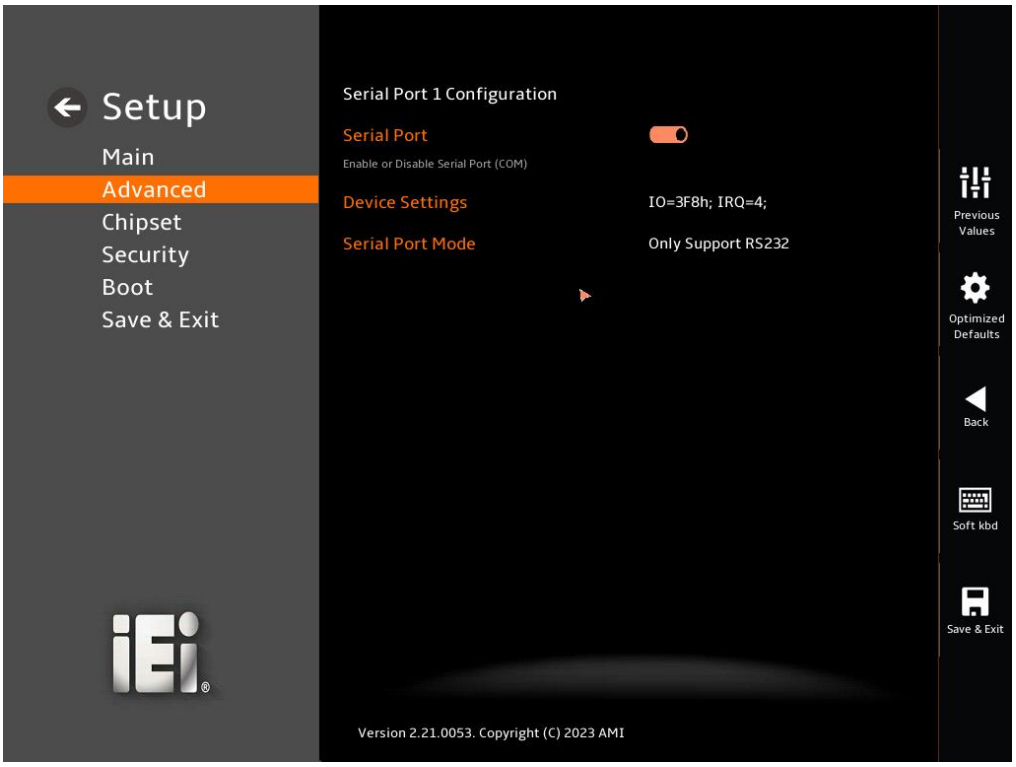
5.3.3 F81966 Super IO Configuration

Use the **F81966 Super IO Configuration** menu (**BIOS Menu 8**) to set or change the configurations for the serial ports.

BIOS Menu 8: F81966 Super IO Configuration

5.3.3.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 9**) to configure the serial port.



BIOS Menu 9: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

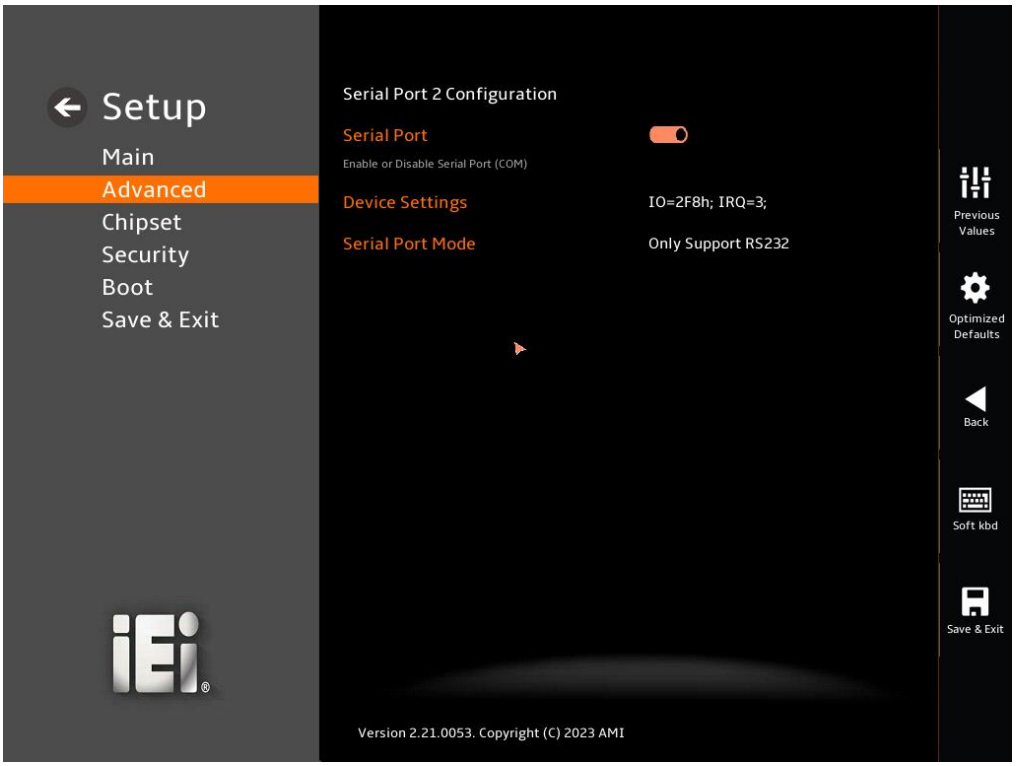
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=3F8h; IRQ=4**	Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

5.3.3.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (**BIOS Menu 10**) to configure the serial port.



BIOS Menu 10: Serial Port 2 Configuration Menu

➔ **Serial Port [Enabled**

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

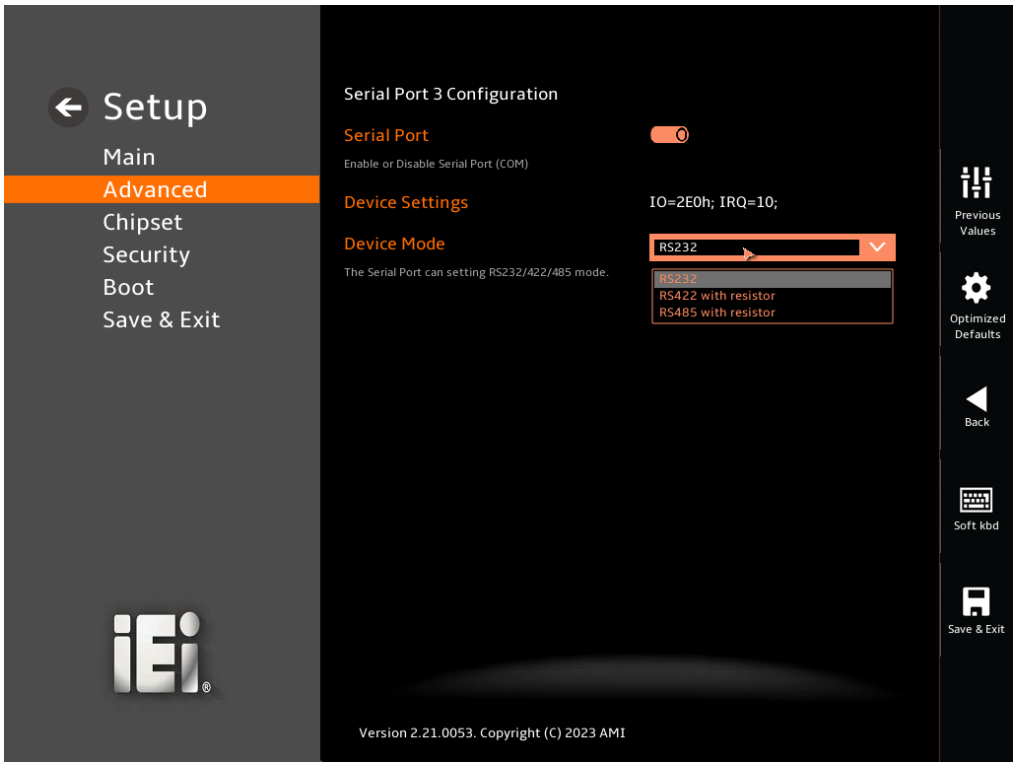
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔	**IO=2F8h; IRQ=3**	Serial Port I/O port address is 2F8h and the interrupt address is IRQ3

5.3.3.3 Serial Port 3 Configuration

Use the **Serial Port 3 Configuration** menu (**BIOS Menu 11**) to configure the serial port.



BIOS Menu 11: Serial Port 3 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E0h; IRQ=10**	Serial Port I/O port address is 2E0h and the interrupt address is IRQ10

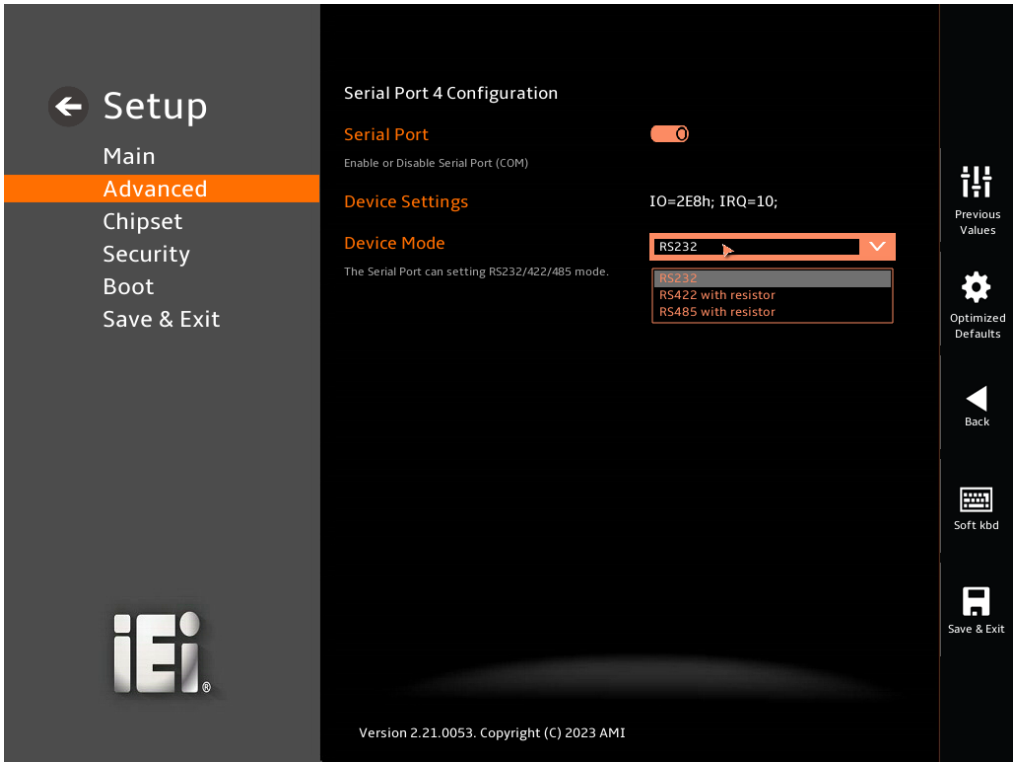
➔ **Device Mode**

Use the **Device Mode** option to change the serial port mode.

➔	**RS232**	The serial port mode is RS-232
	RS422 with Register	The serial port mode is RS-422
	RS485 with Register	The serial port mode is RS-485

5.3.3.4 Serial Port 4 Configuration

Use the **Serial Port 4 Configuration** menu (**BIOS Menu 12**) to configure the serial port.



BIOS Menu 12: Serial Port 4 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔	**Disabled**		Disable the serial port
➔	**Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E8h; IRQ=10**	Serial Port I/O port address is 2E8h and the interrupt address is IRQ10

➔ **Device Mode**

Use the **Device Mode** option to change the serial port mode.

➔ **RS232**	The serial port mode is RS-232
RS422 with Register	The serial port mode is RS-422
RS485 with Register	The serial port mode is RS-485

5.3.4 ENE KB9068 Monitor

The ENE KB9068 Monitor menu (**BIOS Menu 13**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.

BIOS Menu 13: ENE KB9068 Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - System Temperature
- Fan Speeds:
  - Fan1 Speed
- Voltages:
  - CPU_CORE

- +12V
- DDR
- +5VSB
- +3.3VSB

5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 14**) to configure the CPU/system fan start/off temperature and control mode.

BIOS Menu 14: Smart Fan Mode Configuration

➔ **CPU_FAN1 Smart Fan Control [Manual Mode]**

Use the **Smart Fan Control** option to configure the CPU Smart Fan.

➔ **Manual Mode** **DEFAULT** The fan spins at the speed set in Manual Mode settings.

➔ **Auto Mode** The fan adjusts its speed using Auto Mode settings.

➔ **Manual Mode PWM**

Use the **Manual Mode PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **Smart Fan Control** option to configure the CPU Smart Fan.

- ➔ **Manual Mode** **DEFAULT** The fan spins at the speed set in Manual Mode settings.
- ➔ **Auto Mode** The fan adjusts its speed using Auto Mode settings.

➔ **Hysteresis Temp.High**

Use the **Hysteresis Temp.High** option to set when the fan speeds up. If current temperature is higher than this setting, fan will increase the speed. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **Hysteresis Temp.Low**

Use the **Hysteresis Temp.Low** option to set when the fan speeds down. If current temperature is less than this setting, fan will decrease the speed. But fan speed never less than [Normal Duty] setting. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **Normal Duty**

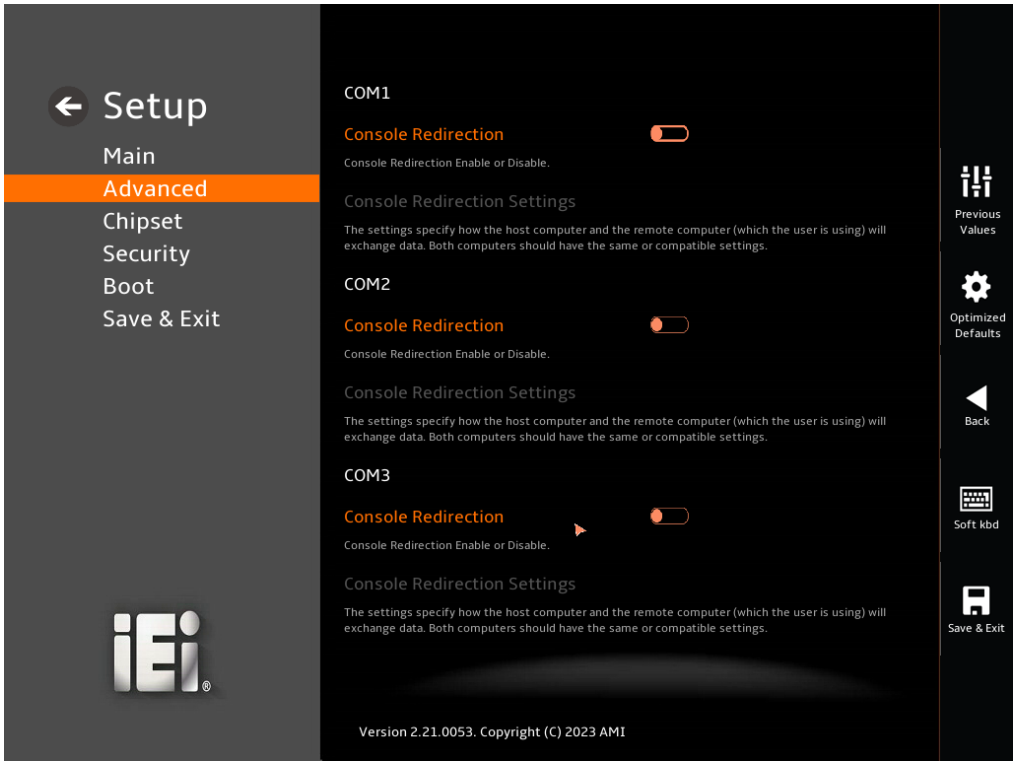
Use the **Normal Duty** option to set system power on speed and minimum fan speed percentage. Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **SYS_FAN1 FAN Slope [1]**

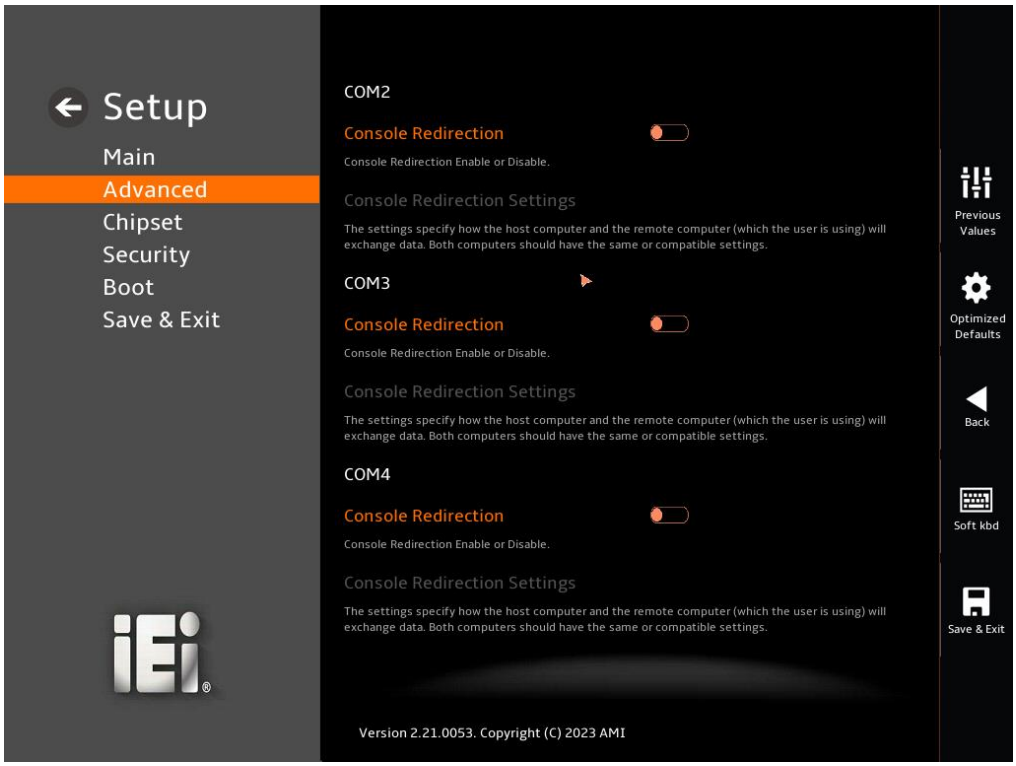
Use the **SYS_FAN1 FAN Slope** option to set the auto mode fan slope PWM from 1 to 8.

5.3.5 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 16**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 15: Serial Port Console Redirection



BIOS Menu 16: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

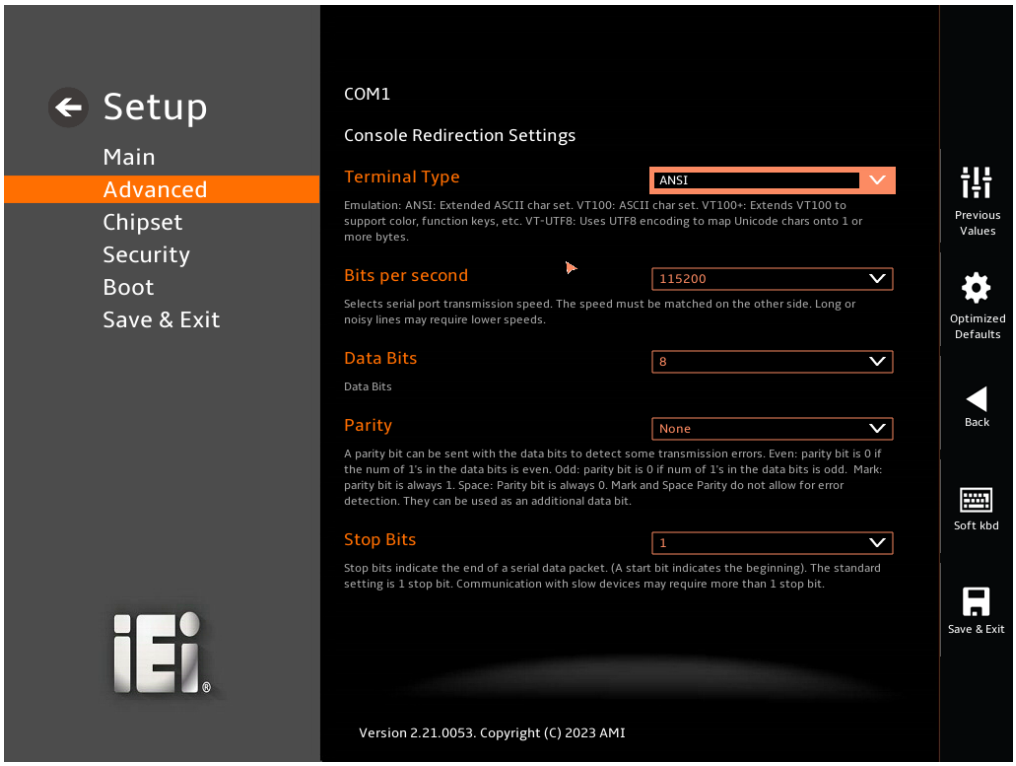
Use **Console Redirection** option to enable or disable the console redirection function.

➔	**Disabled**	**DEFAULT**	Disabled the console redirection function
➔	**Enabled**		Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.5.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 17**) when the **COM Console Redirection** (for COM1 to COM6) option is enabled.



BIOS Menu 17: COM Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100**		The target terminal type is VT100
➔ **VT100+**		The target terminal type is VT100+
➔ **VT-UTF8**		The target terminal type is VT-UTF8
➔ **ANSI**	**DEFAULT**	The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

➔ **9600**	Sets the serial port transmission speed at 9600.
➔ **19200**	Sets the serial port transmission speed at 19200.

- ➔ **38400** Sets the serial port transmission speed at 38400.
- ➔ **57600** Sets the serial port transmission speed at 57600.
- ➔ **115200** **DEFAULT** Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

- ➔ **7** Sets the data bits at 7.
- ➔ **8** **DEFAULT** Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- ➔ **None** **DEFAULT** No parity bit is sent with the data bits.
- ➔ **Even** The parity bit is 0 if the number of ones in the data bits is even.
- ➔ **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- ➔ **Mark** The parity bit is always 1. This option does not allow for error detection.
- ➔ **Space** The parity bit is always 0. T This option does not allow for error detection.

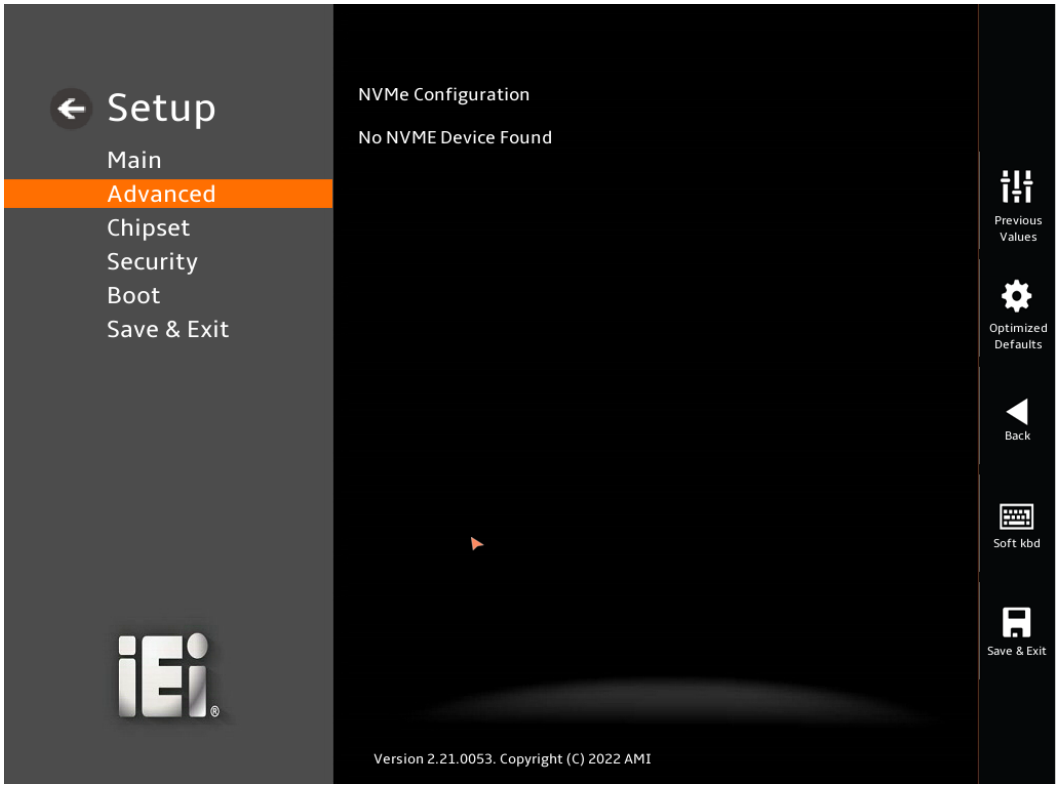
➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- ➔ **1** **DEFAULT** Sets the number of stop bits at 1.
- ➔ **2** Sets the number of stop bits at 2.

5.3.6 NVMe Configuration

Use the **NVMe Configuration** (**BIOS Menu 18**) menu to display the NVMe controller and device information.



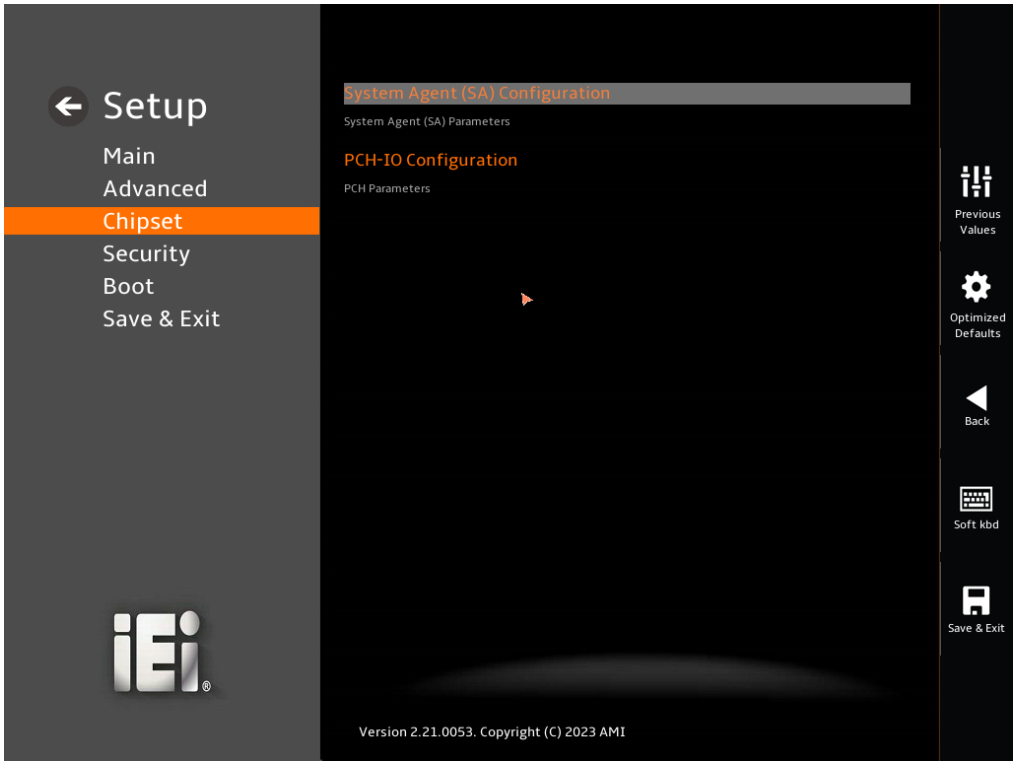
BIOS Menu 18: NVMe Configuration

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 19**) to access the PCH IO and System Agent (SA) configuration menus.

WARNING!

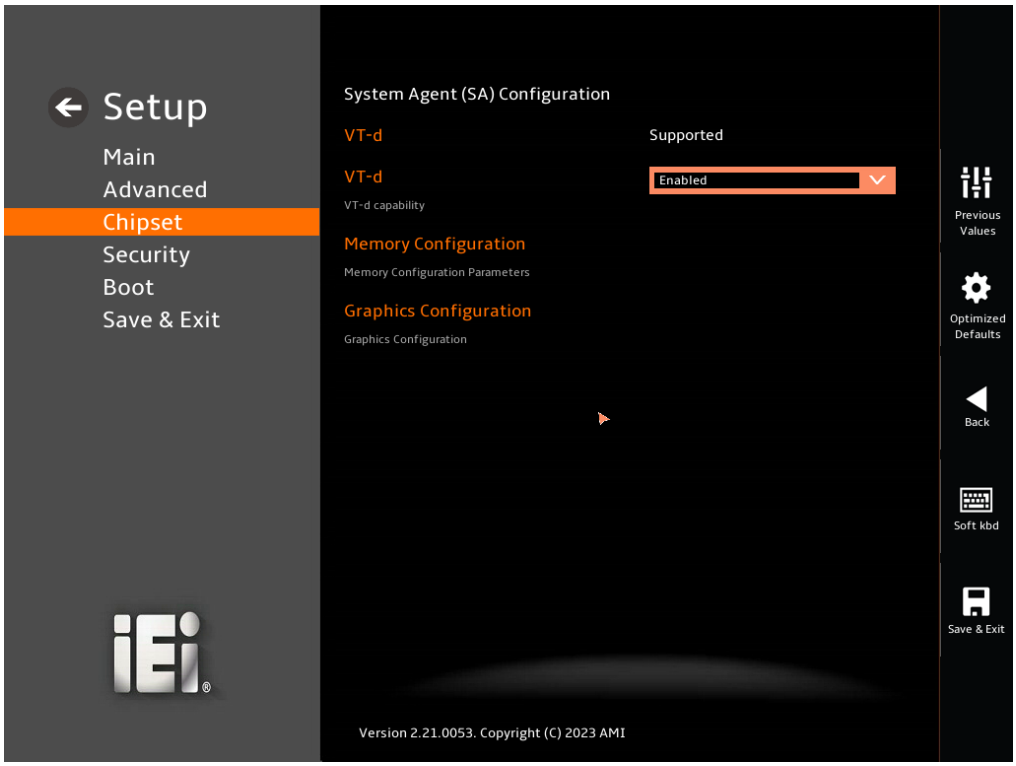
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 19: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 20**) to configure the System Agent (SA) parameters.



BIOS Menu 20: System Agent (SA) Configuration

➔ **VT-d [Enabled]**

Use the **VT-d** option to enable or disable the VT-d capability.

➔	**Disabled**		Disable the VT-d capability
➔	**Enabled**	**DEFAULT**	Enable the VT-d capability

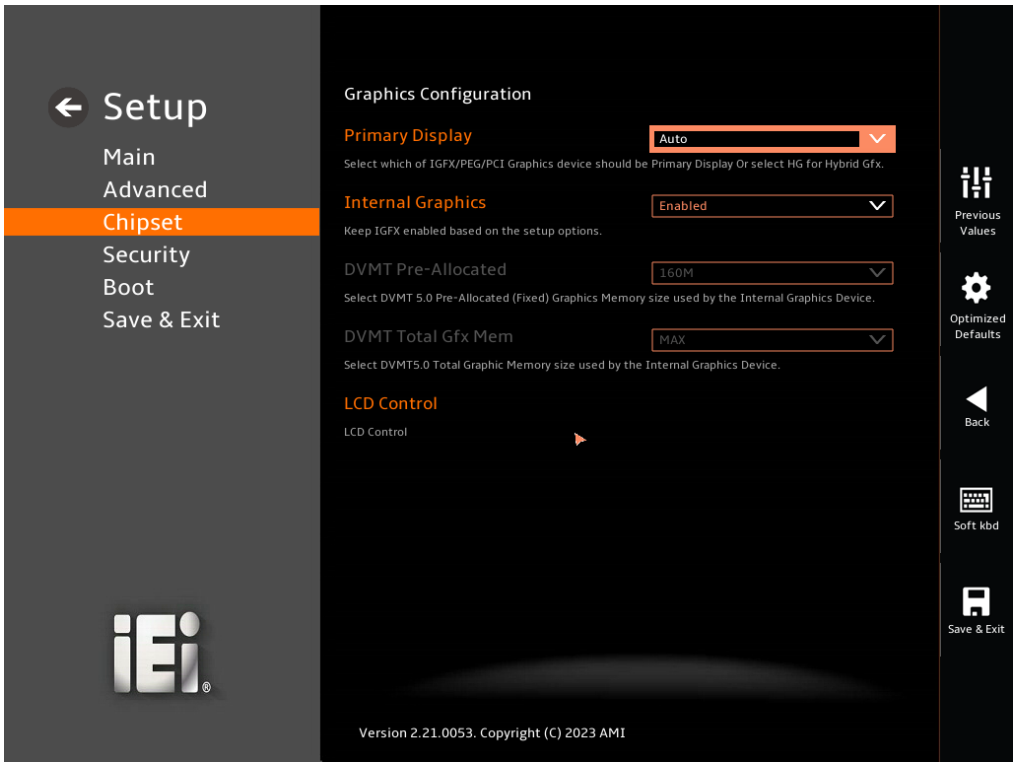
5.4.1.1 Memory Configuration

Use the **Memory Configuration** submenu (**BIOS Menu 21**) to view memory information.

BIOS Menu 21: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 22**) menu to configure the video device connected to the system.



BIOS Menu 22: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG
- PCI

➔ **Internal Graphics [Enabled]**

Use the **Internal Graphics** option to configure whether to keep IGFX enabled. If user wants to support dual display by internal graphics and external graphics, this Internal Graphics

option should be set to Enabled and the above Primary Display option should be set to IGFX.

➔	**Auto**		Auto mode
➔	**Disabled**		Disables IGFX.
➔	**Enabled**	**Default**	Enables IGFX.

➔ **DVMT Pre-Allocated [160M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

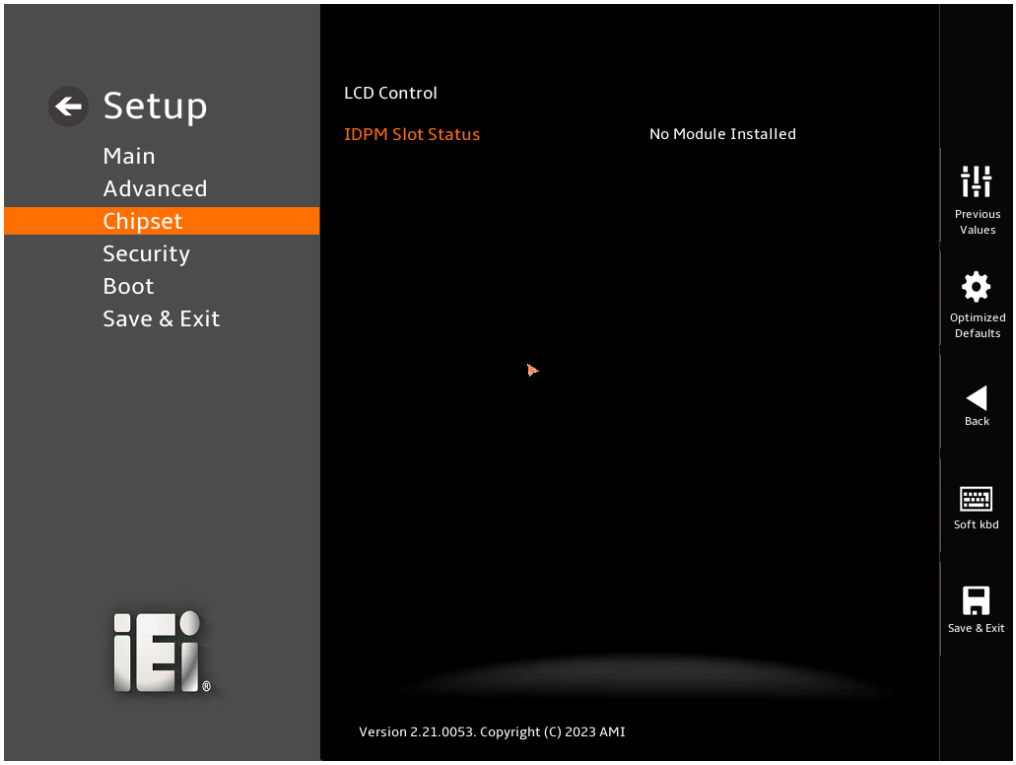
- 80M
- 160M **Default**

➔ **DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT5.0 total graphic memory size used by the internal graphic device. The following options are available:

- 128M
- 256M
- MAX **Default**

➔ **LCD Control**



BIOS Menu 23: LCD Control

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 24**) to configure the PCH parameters.

BIOS Menu 24: PCH-IO Configuration

➔ **Auto Power Button Function [Enabled(AT)]**

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

➔ **Enabled (AT)**	The system power mode is AT.
➔ **Disabled (ATX)**	The system power mode is ATX.

➔ **Power Saving Function(EUP) [Disabled]**

Use the **Power Saving Function(EUP)** BIOS option to enable or disable the power saving function.

➔ **Disabled**	**DEFAULT**	Power saving function is disabled.

➔ **Enabled** Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **USB3CON12 SW1 [+5V DUAL]**

Use the **USB Power SW1** BIOS option to configure the USB power source for the corresponding USB connectors (**Figure 5-2**).

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

➔ **+5V** Sets the USB power source to +5V

➔ **USB2_JUSB3 SW2 [+5V DUAL]**

Use the **USB Power SW2** BIOS option to configure the USB power source for the corresponding USB connectors (**Figure 5-2**).

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

➔ **+5V** Sets the USB power source to +5V

➔ **USB2_JUSB4 SW3 [+5V DUAL]**

Use the **USB Power SW3** BIOS option to configure the USB power source for the corresponding USB connectors (**Figure 5-2**).

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

➔ **+5V** Sets the USB power source to +5V

BIOS Options	Configured USB Ports
USB Power SW1	USB3_CON1, USB3_CON2 (external USB 3.2 Gen 2 ports)
USB Power SW2	JUSB3 (internal USB 2.0 ports)
USB Power SW3	JUSB4 (internal USB 2.0 ports)

Figure 5-2: BIOS Options and Configured USB Ports

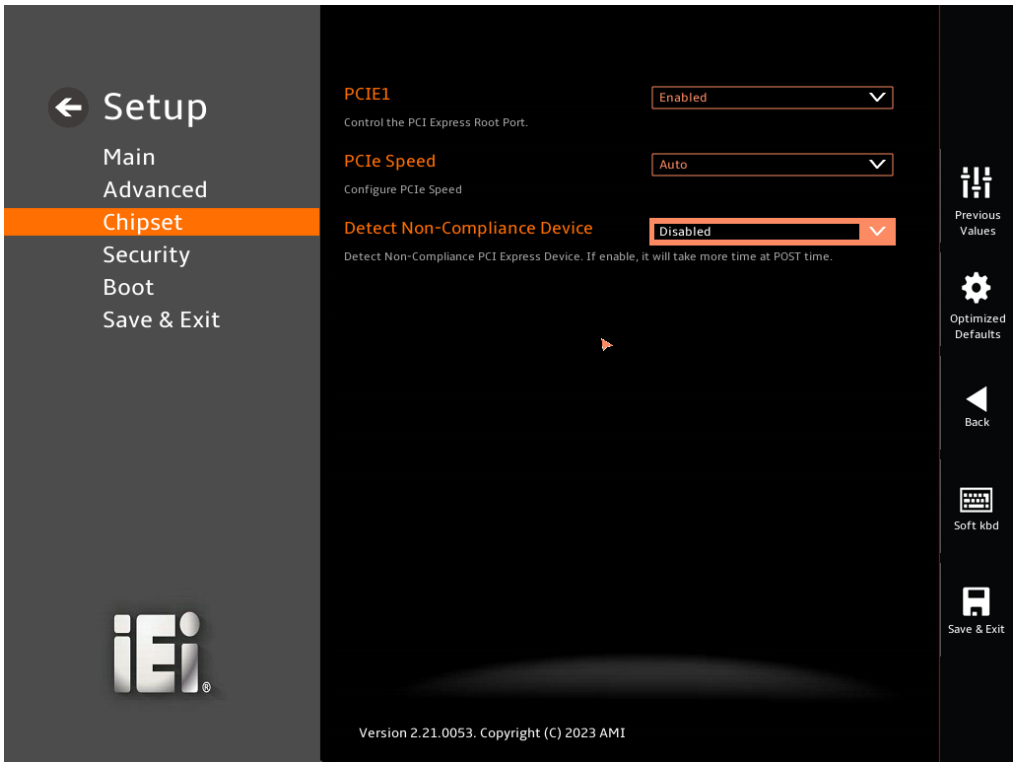
5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 25**) to configure the PCI Express slots and M.2 slots.

BIOS Menu 25: PCI Express Configuration

5.4.2.1.1 PCIe Root Port Setting

Use the **PCIE1** submenu (**BIOS Menu 26**) to configure the PCIe root port setting.



BIOS Menu 26: PCIe Slot Configuration Submenu

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.

➔ **Detect Non-Compliance Device [Disabled]**

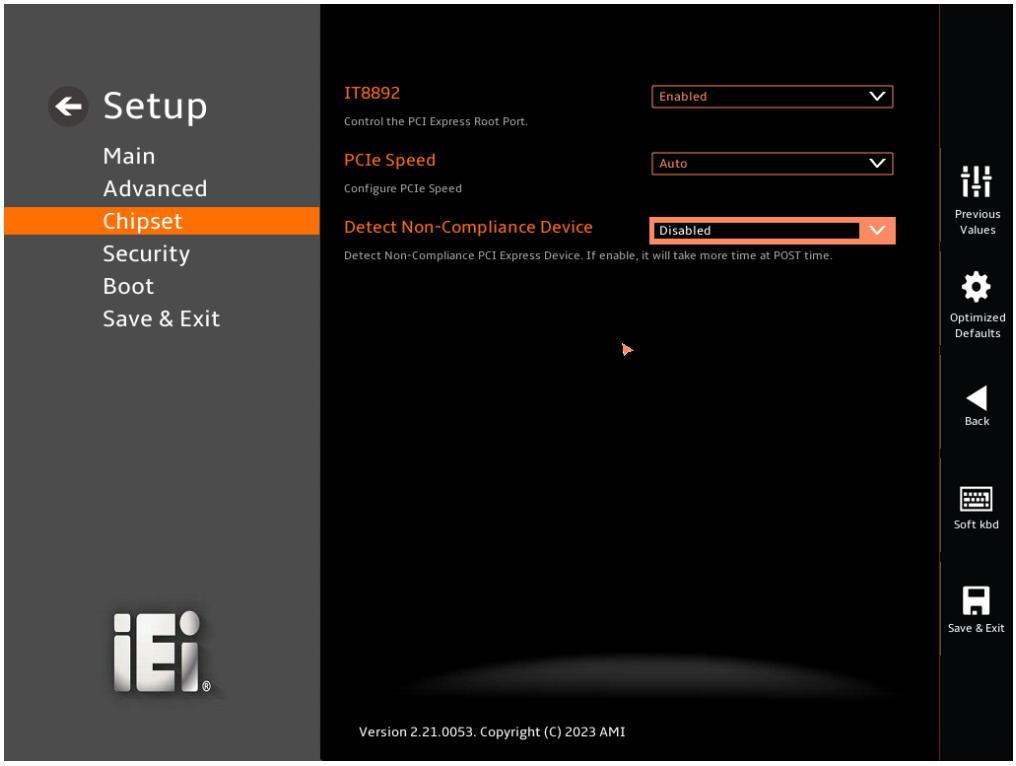
Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.1.2 IT8892

Use the **IT8892** menu (**BIOS Menu 27**) to configure the PCIe root port setting (PCIe x1 to four PCI).



BIOS Menu 27: IT8892

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.

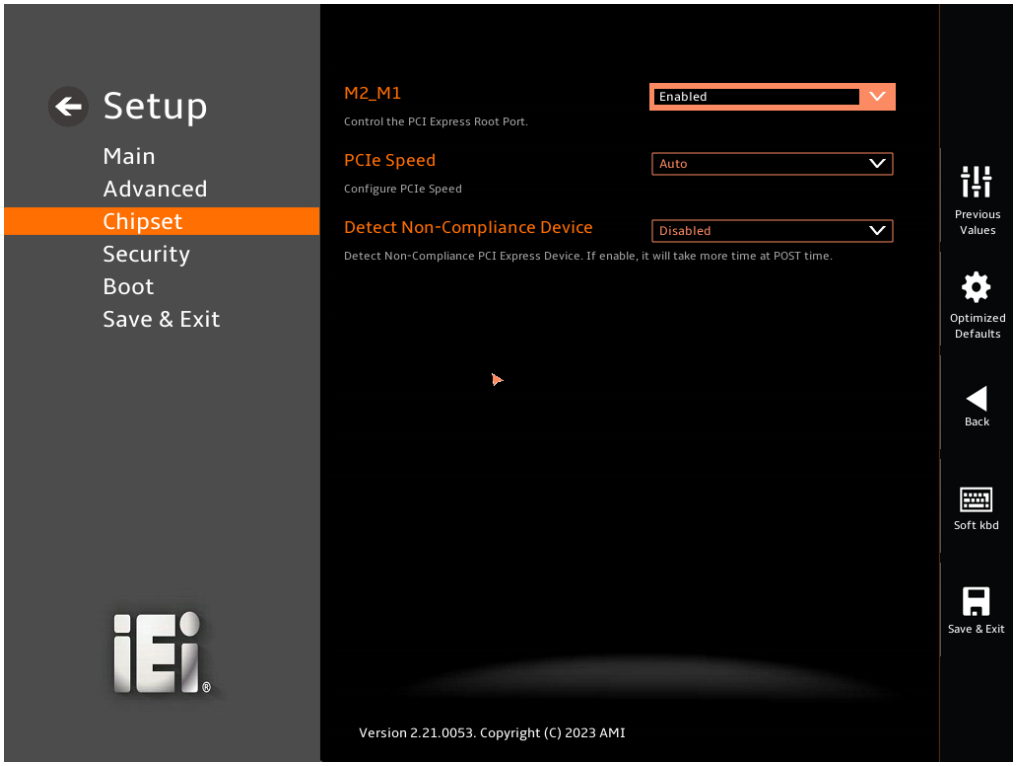
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.1.3 M2_M1 Slot

Use the **M2_M1** menu (**BIOS Menu 28**) to configure the M.2 M key slot.



BIOS Menu 28: M2_M1

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.

- ➔ **Gen1** Configure PCIe Speed to Gen1.
- ➔ **Gen2** Configure PCIe Speed to Gen2.
- ➔ **Gen3** Configure PCIe Speed to Gen3.

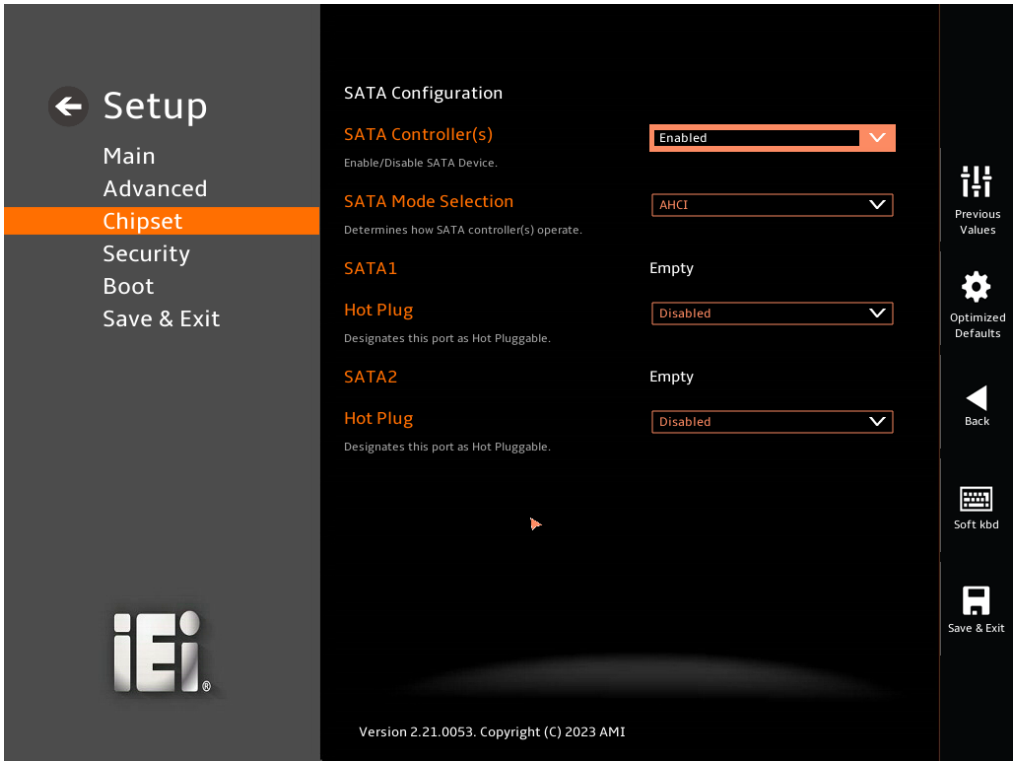
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

- ➔ **Disabled** **DEFAULT** Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
- ➔ **Enabled** Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 29**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 29: SATA Configuration

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to configure the SATA controller(s).

➔ **Enabled**	**DEFAULT**	Enables the on-board SATA controller(s).
➔ **Disabled**		Disables the on-board SATA controller(s).

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

➔ **AHCI**	**DEFAULT**	Configures SATA devices as AHCI device.

➔ **Intel RST Premium With Intel Optane System Acceleration**		Configures SATA devices to the Intel RST Premium With Intel Optane System Acceleration mode.

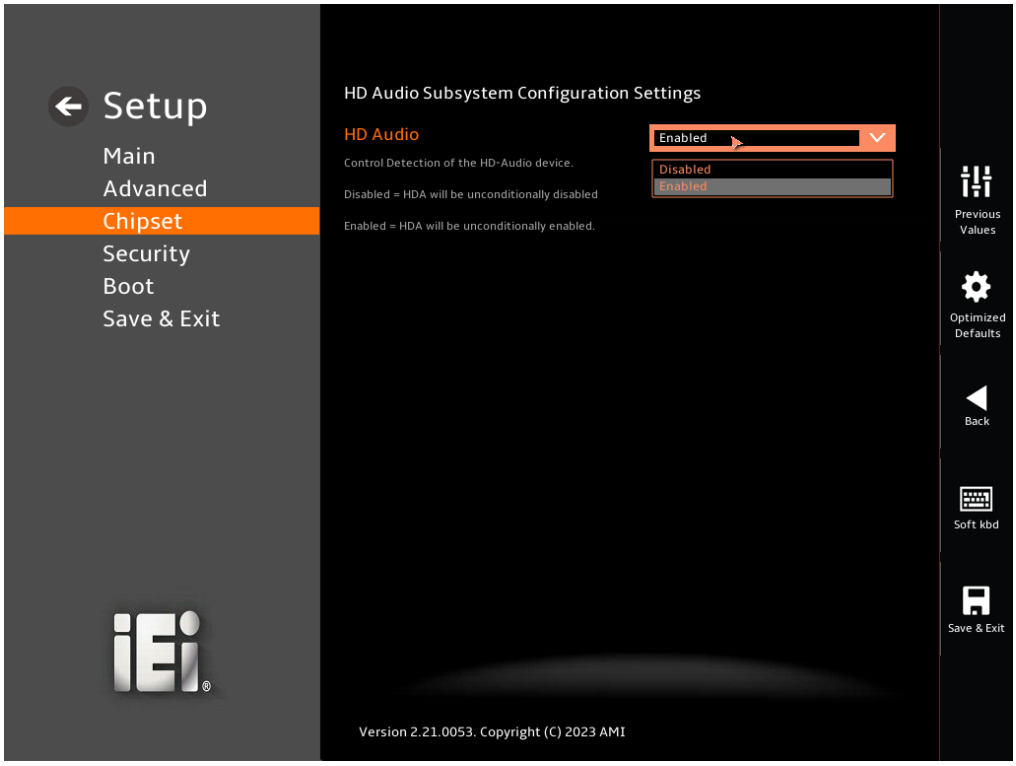
➔ **Hot Plug [Disabled]**

Use the **Hot Plug** option (for SATA1 to SATA2) to designate the correspondent port as hot-pluggable.

➔ **Disabled**	**DEFAULT**	Disables the hot-pluggable function of the SATA port.
➔ **Enabled**		Designates the SATA port as hot-pluggable.

5.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 30**) to configure the PCH Azalia settings.



BIOS Menu 30: HD Audio Configuration

➔ **HD Audio [Enabled]**

Use the **HD Audio** option to enable or disable the High Definition Audio controller.

- ➔ **Disabled** The onboard High Definition Audio controller is disabled.
- ➔ **Enabled** **DEFAULT** The onboard High Definition Audio controller is enabled.

5.5 Security

Use the **Security** menu (**BIOS Menu 31**) to set system and user passwords.

BIOS Menu 31: Security

➔ **Administrator Password**

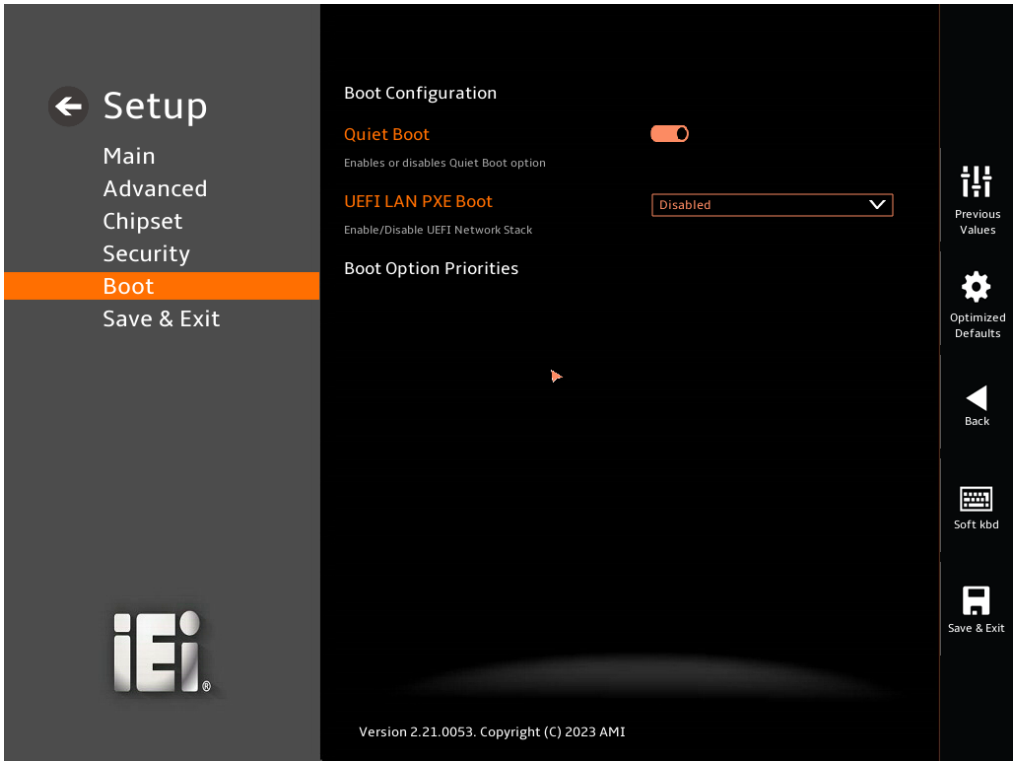
Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 32**) to configure system boot options.



BIOS Menu 32: Boot

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔	**Disabled**		Normal POST messages displayed
➔	**Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

➔ **UEFI LAN PXE Boot [Disabled]**

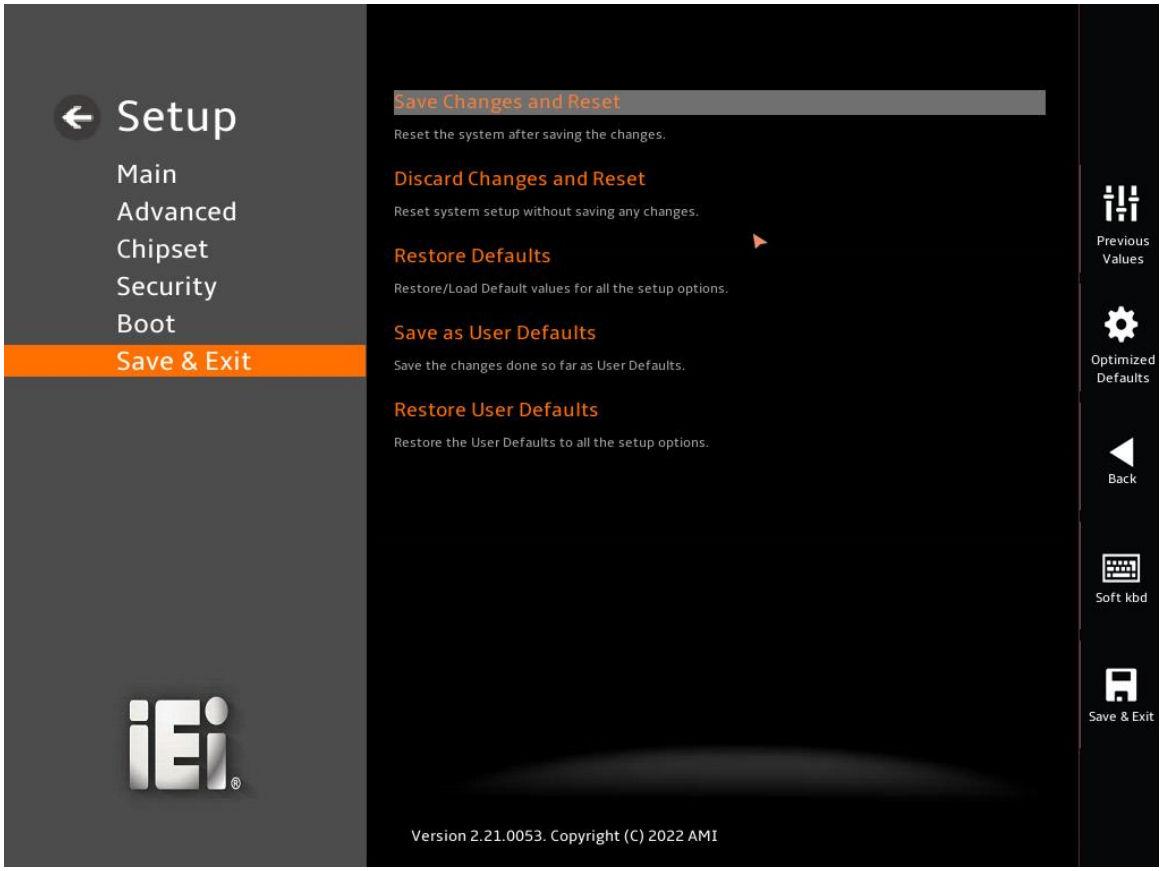
Use the **UEFI LAN PXE Boot** option to enable or disable boot option for legacy network devices.

➔	**Disabled**	**DEFAULT**	Disabled the lan pxe

➔ **Enabled** Enable the lan pxe

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 33**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 33: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

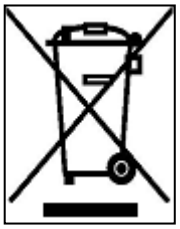
Product Disposal

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

E

Error Beep Code

E.1 PEI Beep Codes

Number of Beeps	Description
4	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

NOTE:

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybromina ted Biphenyls	Polybromina ted Diphenyl Ethers	Bis(2-ethylhexyl) phthalate	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。