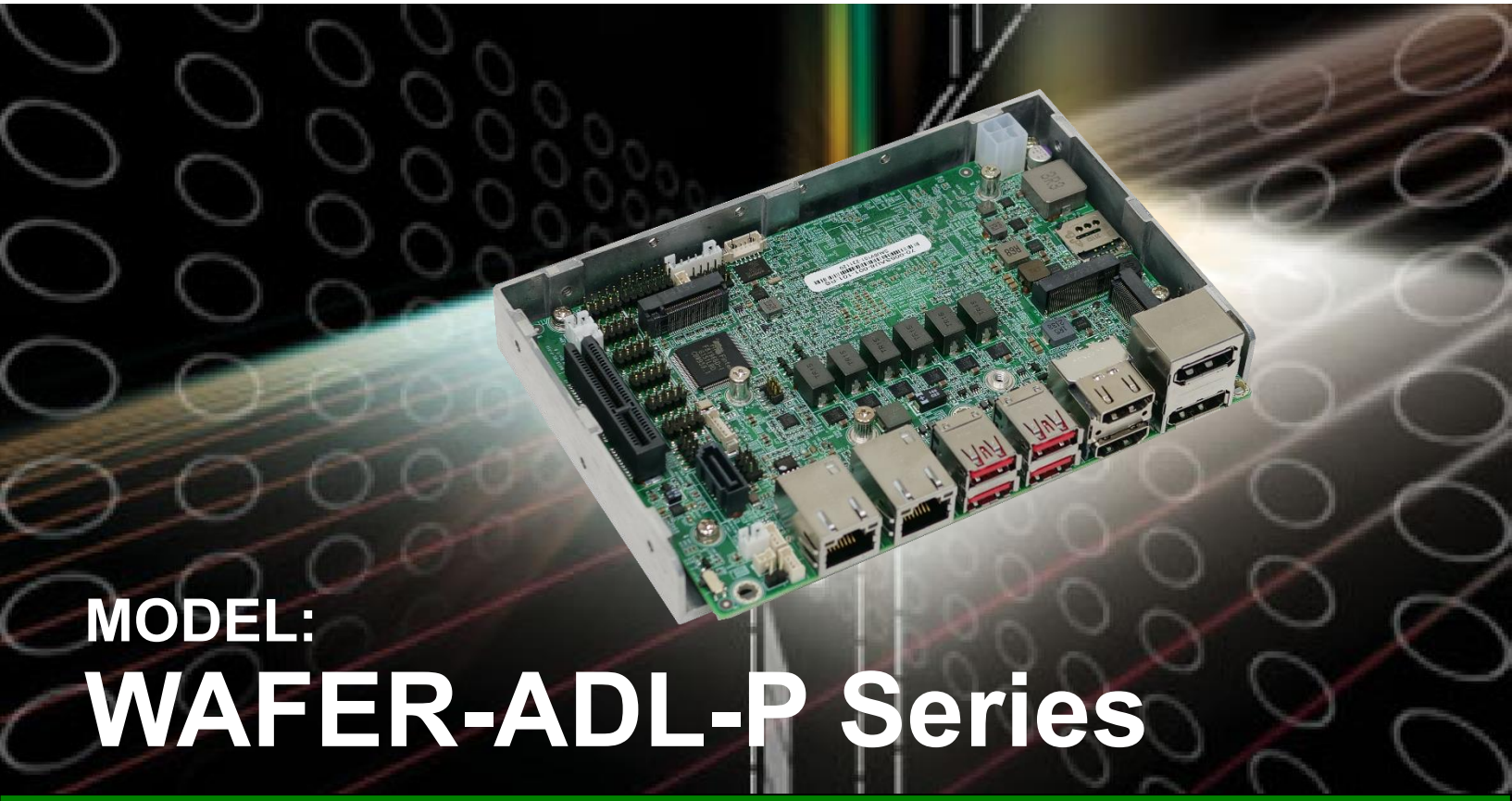
IEI Integration Corp.



MODEL:

WAFER-ADL-P Series

3.5" SBC Supports Intel® Alder Lake-P Processor, Dual HDMI, Dual DP, Dual 2.5GbE, M.2 A Key + B Key + M Key, USB 3.2 Gen 2, SATA 6Gb/s, COM, PCIe x4 for Riser Card and RoHS

User Manual

Rev. 1.00 - July 4, 2023

RoHS Lead Free

Revision

Date	Version	Changes
July 4, 2023	1.00	Initial release

Copyright

COPYRIGHT NOTICE

TRADEMARKS

Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

Table of Contents

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Chapter

1

Introduction

1.1 Introduction

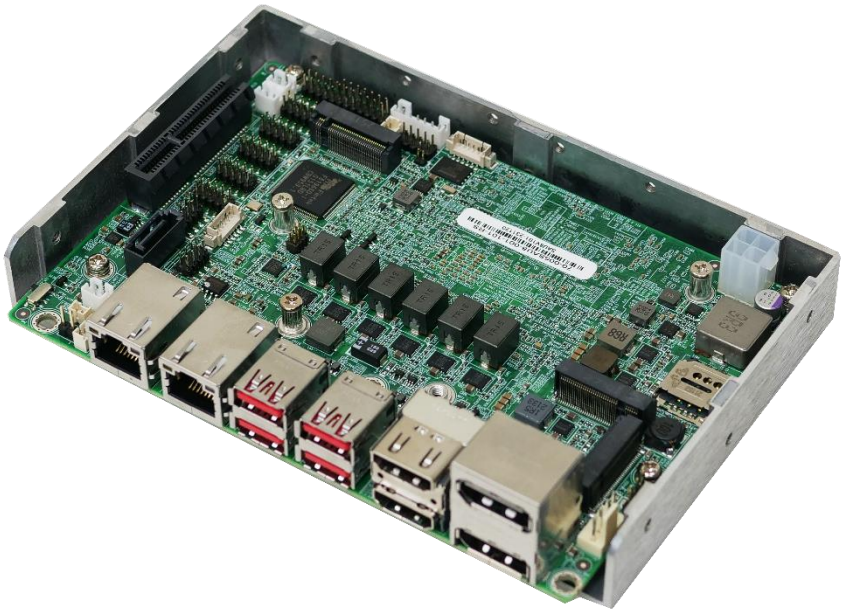


Figure 1-1: WAFER-ADL-P

The WAFER-ADL-P is a 3.5" industrial motherboard equipped with an Intel® Alder Lake-P Core™ i7/i5/i3 and Celeron® processor, and supports onboard LPDDR4x 3200MHz with 8GB memory, up to 16GB.

The WAFER-ADL-P includes two HDMI1.4 (up to 4096 x 2160 @30Hz) connectors, two DP1.4 (up to 4096 x 2160 @60Hz) connectors for quadruple independent display.

Expansion and I/O include one M.2 2230 A-key slot for Wi-Fi & Bluetooth expansion, one M.2 3042 B-key slot with SIM holder for 5G module or NVMe storage expansions, one M.2 2242/2280 M-key slot and one PCIe x4 slot. There are also four USB 3.2 Gen 2 connectors on the rear panel, four USB 2.0 connectors by pin header and one SATA 6Gb/s connector. Serial device connectivity is provided by two internal RS-232/422/485 connectors and four internal RS-232 connectors. Two RJ-45 GbE connectors provide the system with smooth connections to an external LAN.

1.2 Features

Some of the WAFER-ADL-P motherboard features are listed below:

- 12th Gen. Intel® Alder Lake-P Core™ i7/i5/i3 and Celeron® processor on board SoC
- Two Intel® I225V 2.5GbE ports (Colay with I225-LM)
- Four USB 3.2 Gen 2 (Type-A), four USB 2.0 pin header, two RS-232/422/485 pin header, four RS-232 pin header
- M.2 A key, M.2 B key, M.2 M key and PCIe x4 slot (PCIe x4 signal, x4 & x2+x2) expansions
- Support quadruple independent display via two HDMI 1.4 (up to 4096 x 2160 @ 30Hz) and two DP 1.4 (up to 4096 x 2160 @ 60Hz)

1.3 Connectors

The connectors on the WAFER-ADL-P are shown in the figure below.

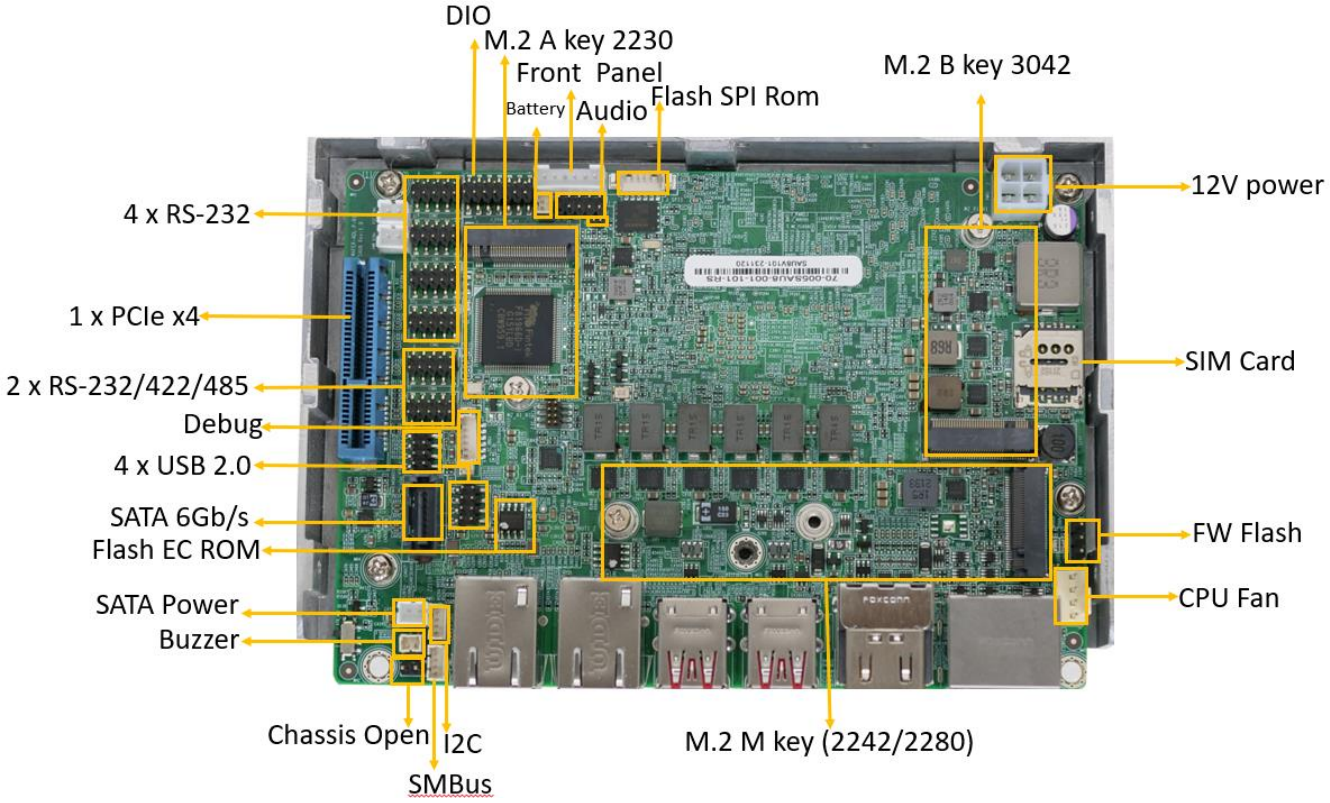


Figure 1-2: Connectors

1.4 Dimensions

The dimensions of the board are listed below:

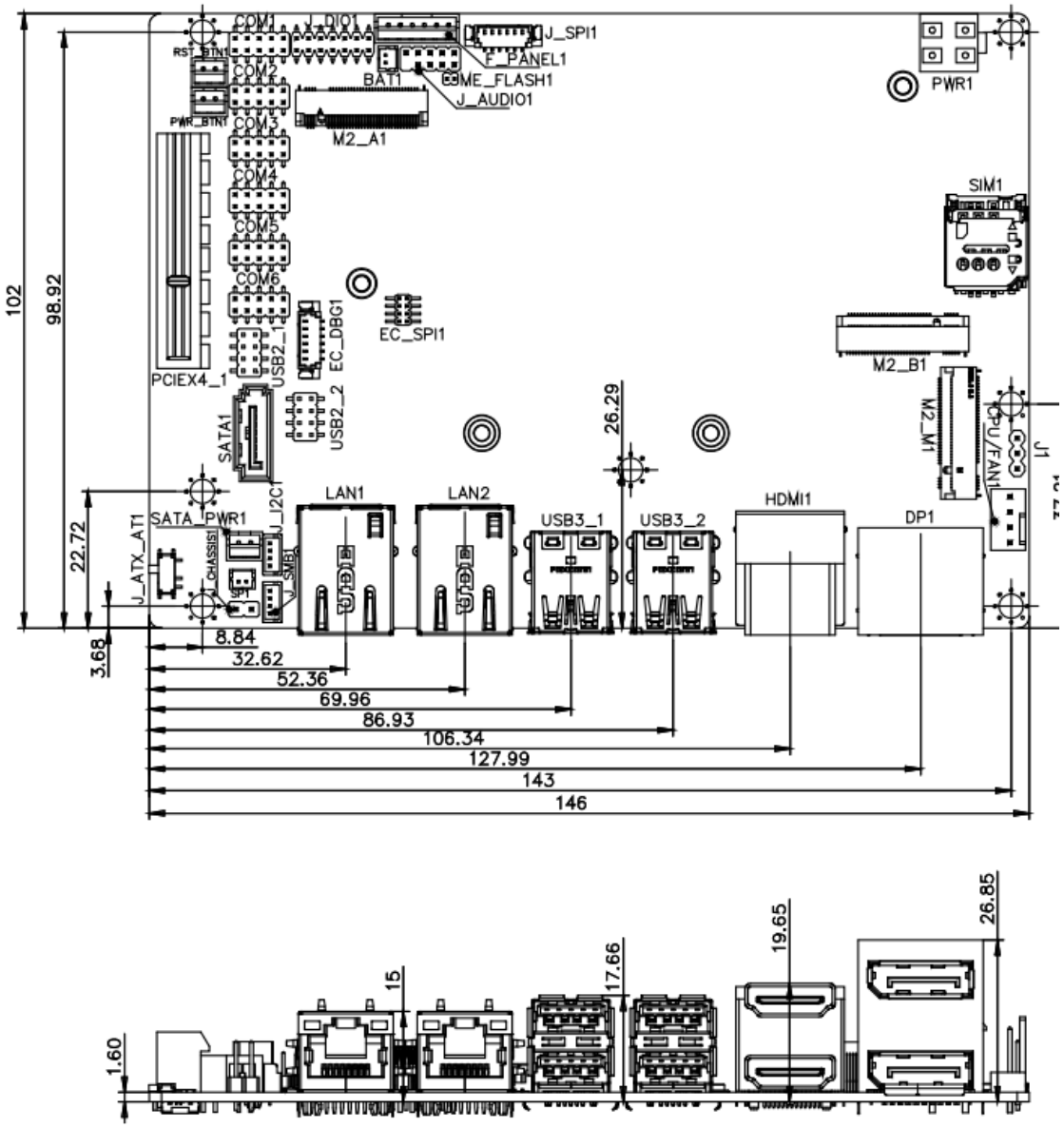


Figure 1-3: Dimensions (mm)

1.5 Data Flow

Shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

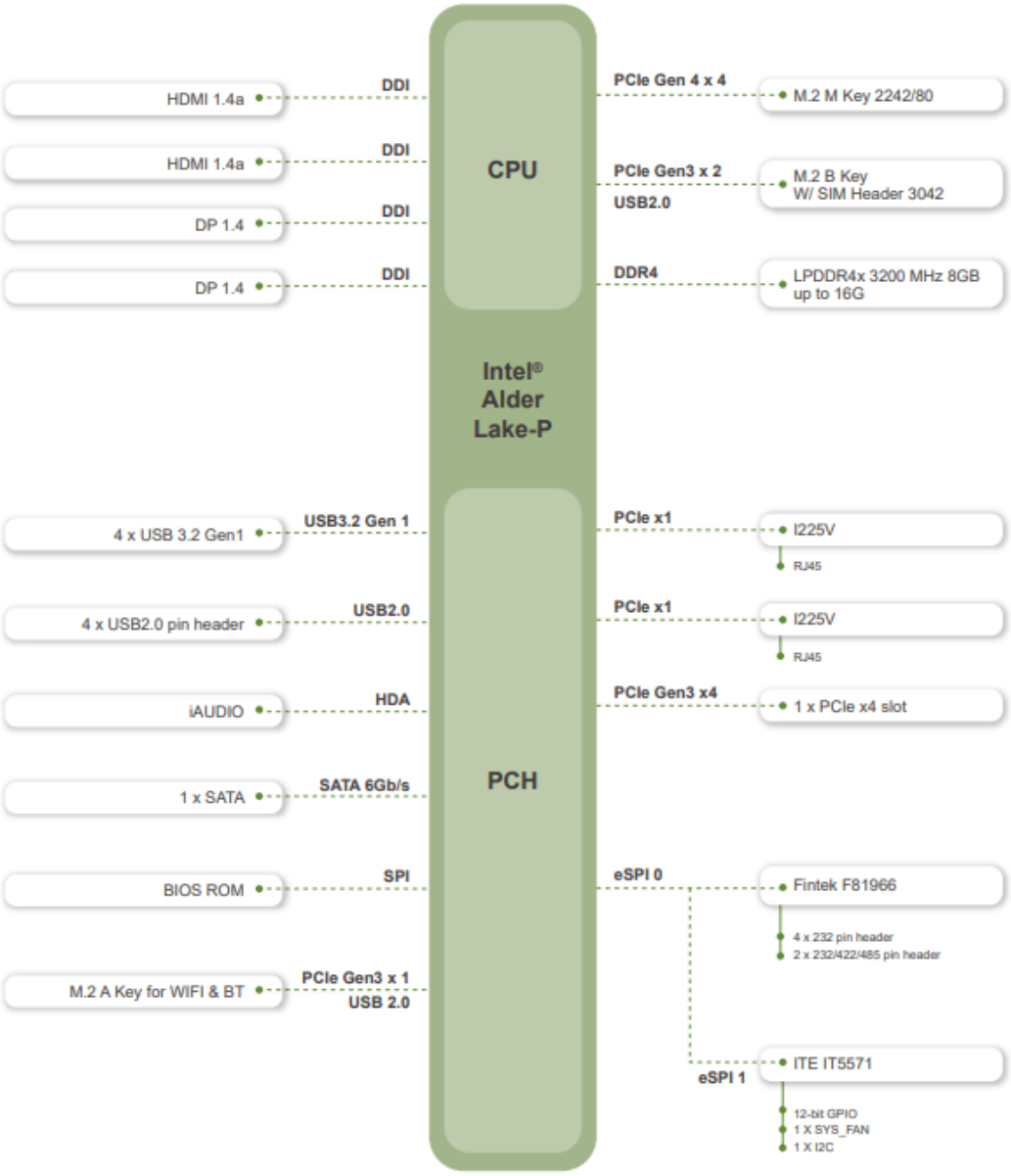


Figure 1-4: Data Flow Diagram

1.6 Technical Specifications

The technical specifications of the WAFER-ADL-P are listed below.

Specification	WAFER-ADL-P
SoC	12th Gen. Intel® Alder Lake-P Core™ i7/i5/i3 and Celeron® processor onboard SoC
BIOS	AMI UEFI BIOS
Memory	On-board LPDDR4x 3200 MHz 8GB, up to 16 GB
Graphics	Intel® UHD Graphics for Celeron® 7305 and Core™ i3-1215U Intel® Xe Graphics architecture for Core™ i5-1235U and Core™ i7-1255U
Display Output	Quadruple independent display 2 x HDMI 1.4a (up to 4096 x 2160@30Hz) 2 x DP 1.4a (up to 4096 x 2160 @60Hz)
Ethernet	LAN1: Intel® I225V 2.5GbE (Colay with I225-LM) LAN2: Intel® I225V 2.5GbE (Colay with I225-LM)
Digital I/O	1 x 12-bit Digital I/O (2x7 pin) header
Watchdog Timer	Software programmable support 1~255 sec. system reset
I/O Interface	
Audio Connector	1 x Analog audio (2x5 pin, p=2.0) supports 7.1 channel HD audio by IEI AC-KIT-888S audio kit
Serial Ports	2 x RS-232/422/485 (2x5 pin, P=2.0) wafer 4 x RS-232 (2x5 pin, P=2.0) wafer
USB Ports	4 x USB 3.2 Gen 2 (Type-A) (10Gb/s) 4 x USB 2.0 by 8-pin (2x4 pin, P=2.0) header
Front Panel	1 x Front panel (1x6 pin, p=2.0; power LED, HDD LED 1 x Power button connector (1x2 pin, p=2.0) 1 x Reset button connector (1x2 pin, p=2.0)
Fan	1 x System Smart fan connector by 4-pin (1x4) wafer

Specification	WAFER-ADL-P
SMBus/I²C	1 x I²C connector by 4-pin (1x4 pin, p=1.25) wafer 1 x SMBus connector by 4-pin (1x4 pin, p=1.25) wafer
Storage	1 x SATA 6Gb/s with 5 V SATA power connectors
Expansions	1 x M.2 2230 A key for Wi-Fi & BT (PCIe Gen3 x1 & USB 2.0) 1 x M.2 3042 B key with SIM slot (PCIe x2 & USB 2.0) 1 x M.2 2242/2280 M key (PCIe x4) 1 x PCIe x4 slot (PCIe x4 signal, x4 & x2+x2)
Environmental and Power Specifications	
Power Supply	12V DC power supply Support AT/ATX mode
Power Consumption	12V@2.83A (12th Gen Intel® Core™ i7-1265UE CPU with 8GB 3200 MHz LPDDR4x memory, max. loading, EuP mode enabled)
Operating Temperature	0°C ~ 60°C
Storage Temperature	-30°C ~ 70°C
Humidity	5% ~ 95%, non-condensing
Physical Specifications	
Dimensions	146mm x 102mm
Weight GW/NW	850g / 350g

Table 1-1：Technical Specifications

Chapter

2

Unpacking

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the WAFER-ADL-P is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the WAFER-ADL-P was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The WAFER-ADL-P is shipped with the following components:

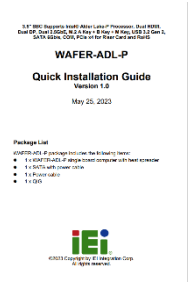
Quantity	Item and Part Number	Image
1	WAFER-ADL-P single board computer	
1	Power cable	
1	SATA with power cable kit	
1	Quick Installation Guide	 WAFER-ADL-P Quick Installation Guide Version 1.0 May 25, 2023 Package List

Table 2-1: Packing List

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual-port USB 2.0 cable, 300mm, P=2.0 (**P/N** : CB-USB02A-RS)	
SATA power cable, MOLEX 5264-4P to SATA15P (**P/N**: 32102-000100-200-RS)	
RS-232/422/485, 200mm, P=2.0 (**P/N:** 32205-002700-200-RS)	
RS-232 cable, 250 mm, p=1.25 (**P/N**: 32005-003500-200-RS)	
Audio kit, 7.1 Channel (**P/N**: AC-KIT-888S-R10)	
Cooler module, 157 mm x 100 mm x 20 mm, with pad and fan (**P/N**: CM-WAFER-WF-R10)	
Heatsink module, 157 mm x 100 mm x 20 mm, with pad (**P/N**: CM-WAFER-WOF-R10)	

PCIe x4 to two PCIe x2 riser card for WAFER on the left side (**P/N**: NWR2-L2S-R10)	
PCIe x4 to two PCIe x2 riser card for WAFER on the right side (**P/N**: NWR2-R2S-R10)	
PCIe x4 to four PCIe x1 riser card for WAFER on the left side **(P/N:** NWR2-L4S-R10)	
PCIe x4 to four PCIe x1 riser card for WAFER on the right side (**P/N**: NWR2-R4S-R10)	

Table 2-2: Optional Items

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 WAFER-ADL-P Layout

The figures below show all the connectors and jumpers.

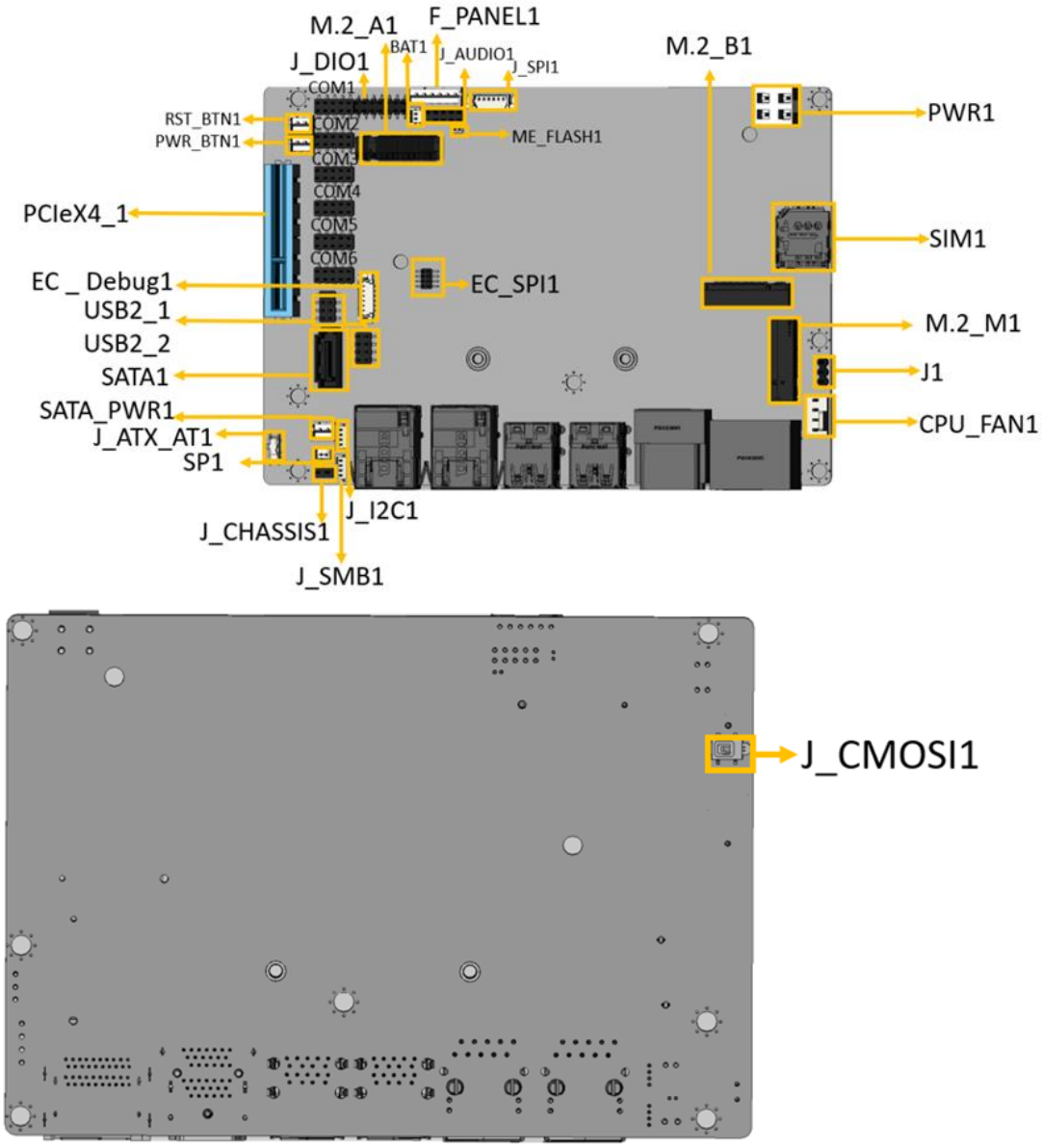


Figure 3-1: Connector And Jumper Locations

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
Clear CMOS button	4-pin switch	J_CMOS1
AT/ATX power mode setting	3-pin switch	J_ATX_AT1
Flash descriptor security override jumper	2-pin header	ME_FLASH1
Audio connector for IEI AC-KIT-888S kit	10-pin header	J_AUDIO1
12V power input connector	4-pin Molex	PWR1
RTC battery connector	2-pin wafer	BAT1
Buzzer connector	2-pin wafer	SP1
Chassis intrusion connector	2-pin header	J_CHASSIS1
Digital I/O connector	14-pin header	J_DIO1
EC debug connector	6-pin wafer	EC_DBG1
Fan connector	4-pin wafer	CPU/FAN1
Front panel connector	6-pin wafer	F_PANEL1
Power button connector	2-pin wafer	PWR_BTN1
Reset button connector	2-pin wafer	RST_BTN1
RS-232 serial port connectors	10-pin header	COM1, COM2, COM3, COM4
RS-232/422/485 serial port connectors	10-pin header	COM5, COM6
SATA 6Gb/s connector	7-pin SATA connector	SATA1
SATA power connector	2-pin wafer	SATA_PWR1
I2C connector	4-pin wafer	J_I2C1
SMBus connector	4-pin wafer	J_SMB1
Flash SPI ROM connector	6-pin wafer	J_SPI1
Flash EC ROM connector	8-pin header	EC_SPI1

Internal USB 2.0 connectors	8-pin header	USB2_1, USB2_2
M.2 2230 A key slot	M.2 A-key slot	M2_A1
M.2 3042 B key slot	M.2 B-key slot	M2_B1
M.2 2242/2280 M key slot	M.2 M-key slot	M2_M1
PCIe x4 slot	PCIe slot for riser card	PCIEX4_1
SIM card slot	6-pin SIM holder	SIM1

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
External 2.5GbE RJ-45 connectors	RJ45	LAN1, LAN2
External dual USB 3.2 Gen 2 connectors	USB 3.2 Gen 2 Type-A	USB3_1, USB3_2
External dual DP connector	DP	DP1
External dual HDMI connector	HDMI	HDMI1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the WAFER-ADL-P.

3.2.1 Clear CMOS Button

CN Label: **J_CMOS1**

CN Type: Button

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

To clear the CMOS Setup (for example if you have forgotten the password, you should clear the CMOS and then reset the password), you should disconnect the RTC battery and press the button for about 3 seconds. This will set back to normal operation mode.

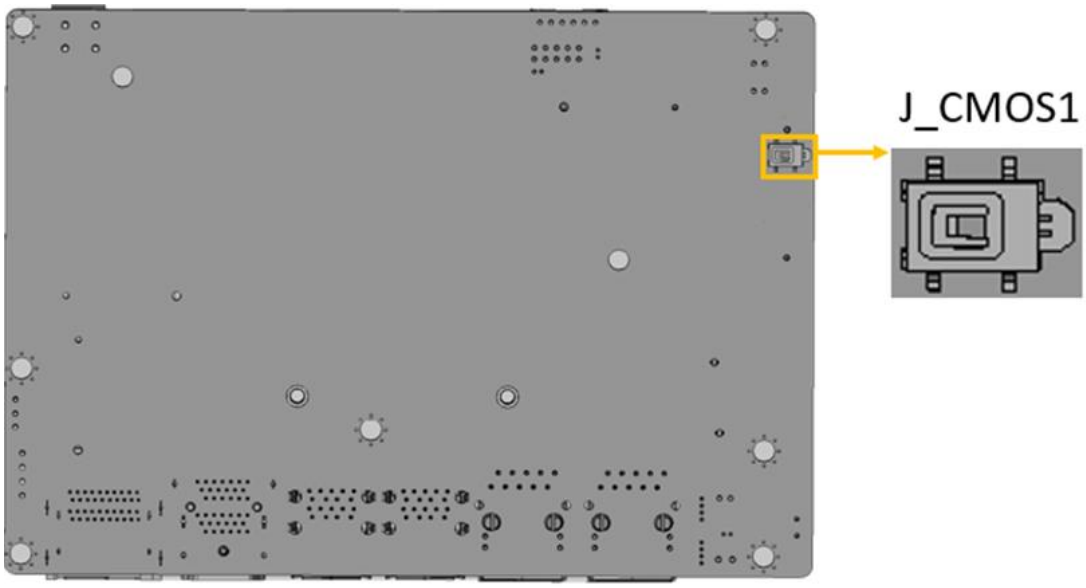


Figure 3-2: Clear CMOS Location

Status	DESCRIPTION
NC	Keep CMOS Setup (Normal Operation)
Press	Clear CMOS Setup

Table 3-3: Clear CMOS Pinouts

3.2.2 AT/ATX Power Mode Setting

CN Label: **J_ATX_AT1**

CN Type: Slide Switch

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

The AT/ATX power mode selection is made through the AT/ATX power mode switch which is shown in Figure3-3.

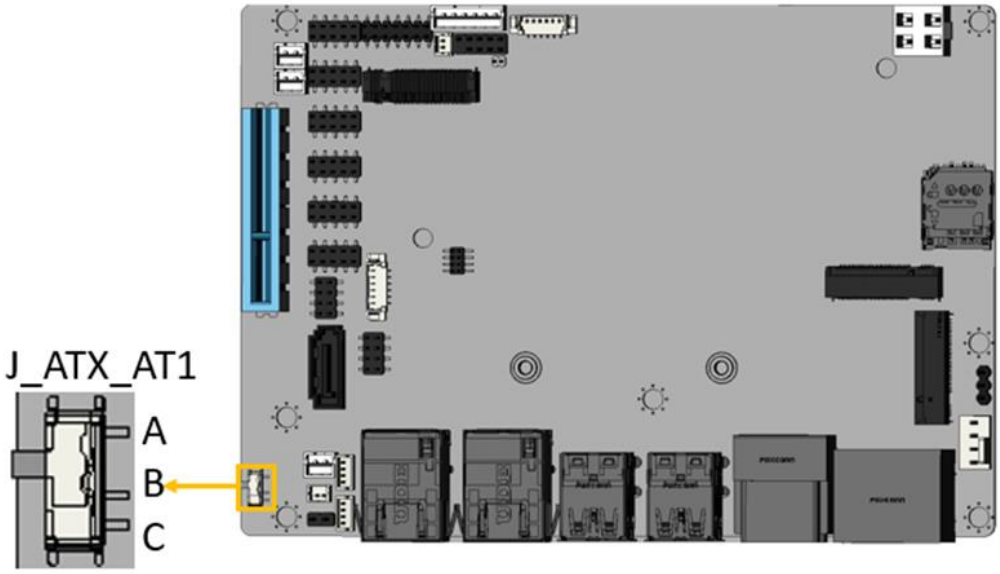


Figure 3-3: AT/ATX Power Mode Switch Locations

PIN NO.	DESCRIPTION
Short A - B	ATX Power Mode (default)
Short B - C	AT Power Mode

Table 3-4: AT/ATX Power Mode Switch Pinouts

3.2.3 Chassis Intrusion Connector

CN Label: **J_CHASSIS1**

CN Type: 2-pin header, P=2.54mm

CN Location: See **Figure 3-4**

CN Pinouts: See **Table 3-5**

The Chassis Intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

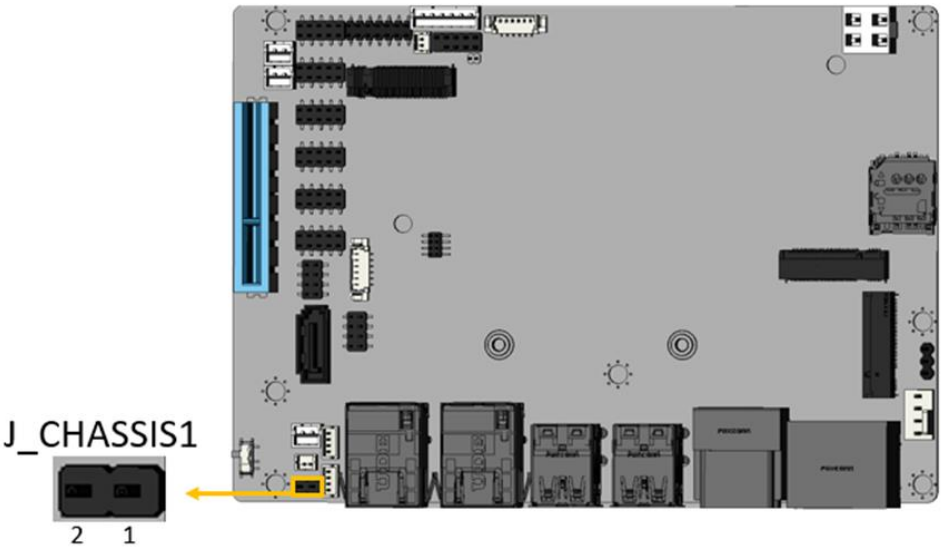


Figure 3-4: Chassis Intrusion Location

PIN NO.	DESCRIPTION
1	CASEOPEN_N
2	GND

Table 3-5: Chassis Intrusion Pinouts

3.2.4 Flash Descriptor Security Override Jumper

CN Label: **ME_FLASH1**

CN Type: 2-pin header, P=1.27mm

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The ME_FLASH1 connector is used for Flash Descriptor Security Override.

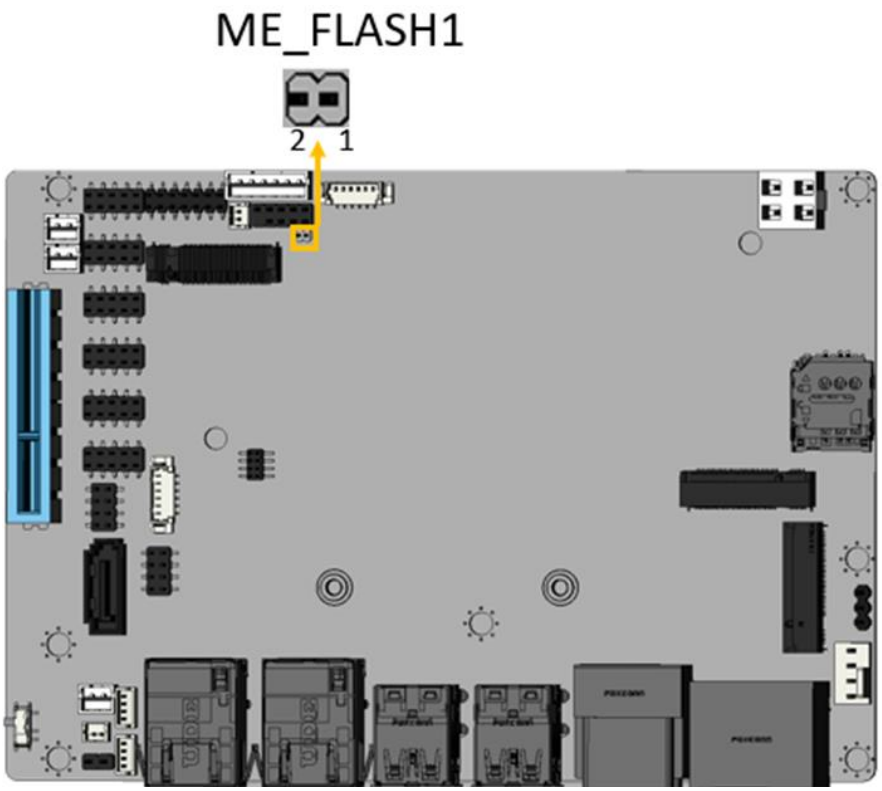


Figure 3-5: Flash Descriptor Security Override Jumper Location

PIN NO.	DESCRIPTION
Open	Disable (default)
Short	Enable

Table 3-6: Flash Descriptor Security Override Jumper Pinouts

To update the ME firmware, please follow the steps below.

Step 1: Before turning on the system power, short the Flash Descriptor Security Override jumper.

Step 2: Update the BIOS and ME firmware, and then turn off the system power.

Step 3: Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting.

Step 4: Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

3.2.5 Audio Connector For IEI AC-KIT-888S kit

CN Label: **J_AUDIO1**

CN Type: 10-pin header, p=2.00 mm

CN Location: See **Figure 3-6**

CN Pinouts: See **Table 3-7**

The audio connector is connected to external audio devices (AC-KIT-888S-R10) including speakers and microphones for the input and output of audio signals to and from the system.

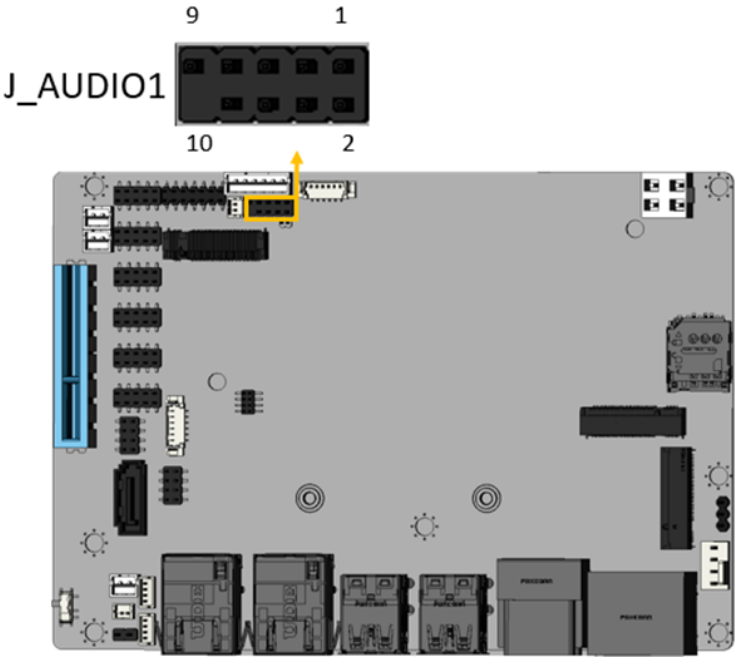


Figure 3-6: Audio Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	HDA_SYNC_R	2	HDA_BCLK_R
3	HDA_SDO_R	4	HDA_PCBEEPC
5	HDA_SDI_0_R	6	HDA_RST_R
7	+5V	8	GND
9	+12V	10	GND

Table 3-7:Audio Connector Pinouts

3.2.6 12V Power Input Connector

CN Label: **PWR1**

CN Type: 4-pin Molex, p=4.2 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-8**

The connector supports the +12V power supply.

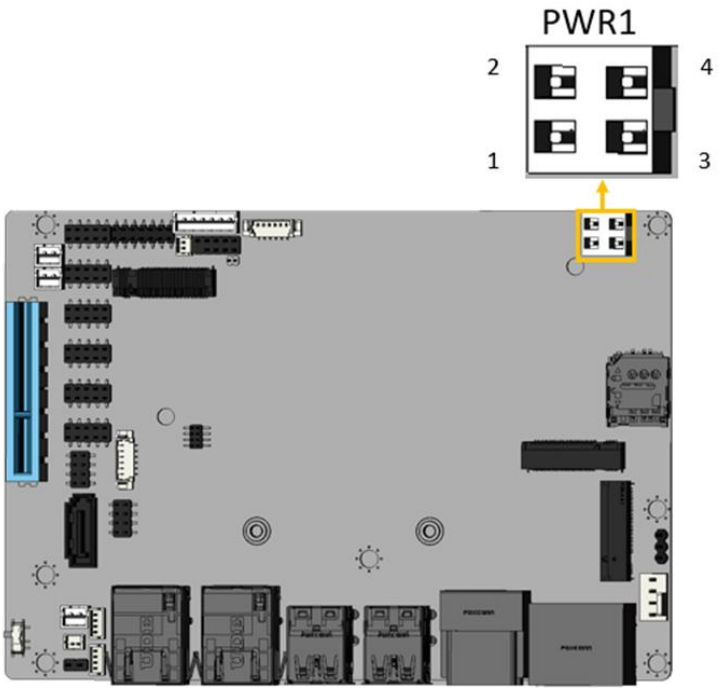


Figure 3-7: ATX 12V Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	+12V	4	+12V

Table 3-8: ATX 12V Power Connector Pinouts

3.2.7 RTC Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

NOTE:

It is recommended to attach the RTC battery onto the system chassis in which the WAFER-ADL-P is installed.

CN Label:	**BAT1**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-8**
CN Pinouts:	See **Table 3-9**

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

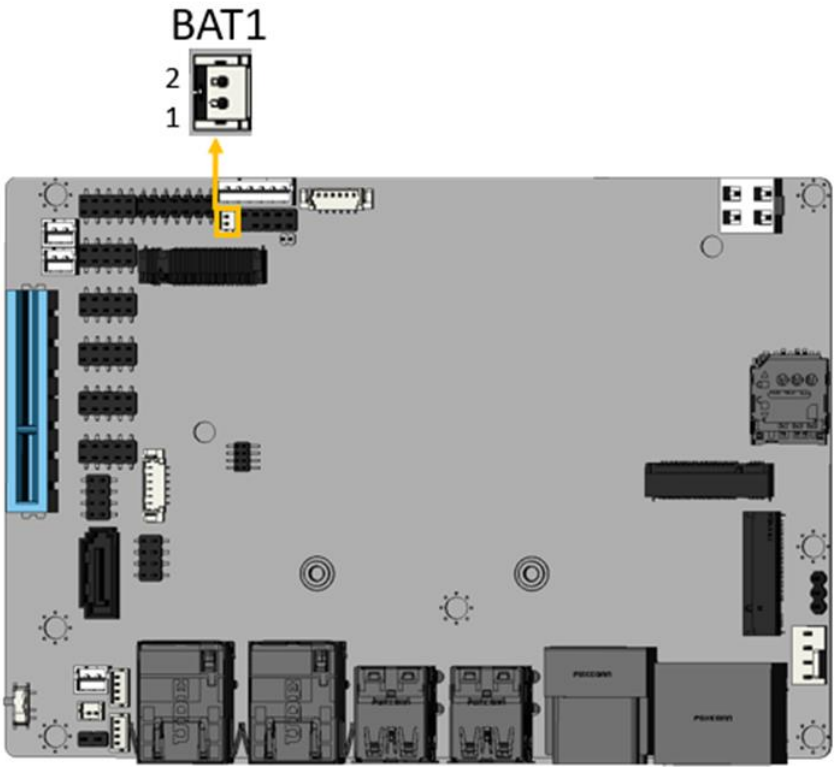


Figure 3-8: Battery Connector Location

PIN NO.	Description
1	VBATT
2	GND

Table 3-9: Battery Connector Pinouts

3.2.8 Buzzer Connector

CN Label: **SP1**

CN Type: 2-pin wafer, p=1.25 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-10**

The buzzer conector is connected with the buzzer to give a beep warning when the motherboard goes wrong.

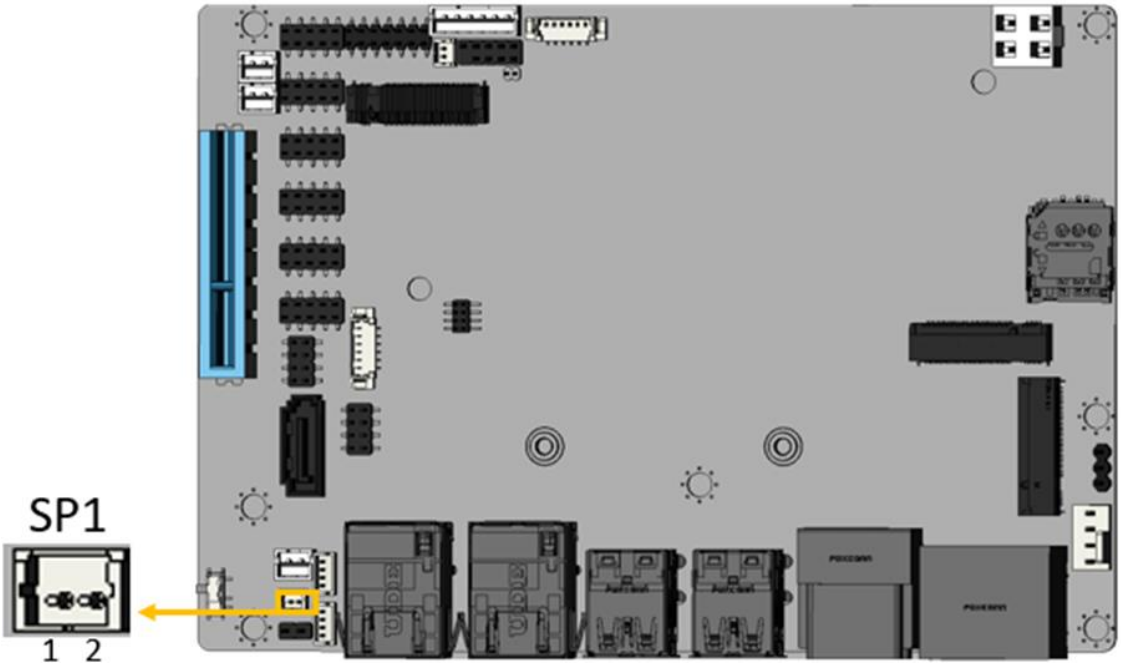


Figure 3-9: Buzzer Connector Location

PIN NO.	Description
1	+5V
2	PC_BEEP_N

Table 3-10: Buzzer Connector Pinouts

3.2.9 Digital Input /Output Connector

CN Label: **J_DIO1**

CN Type: 14-pin header, p=2.0 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-11**

The 12-bit digital I/O connector provides programmable input and output for external devices.

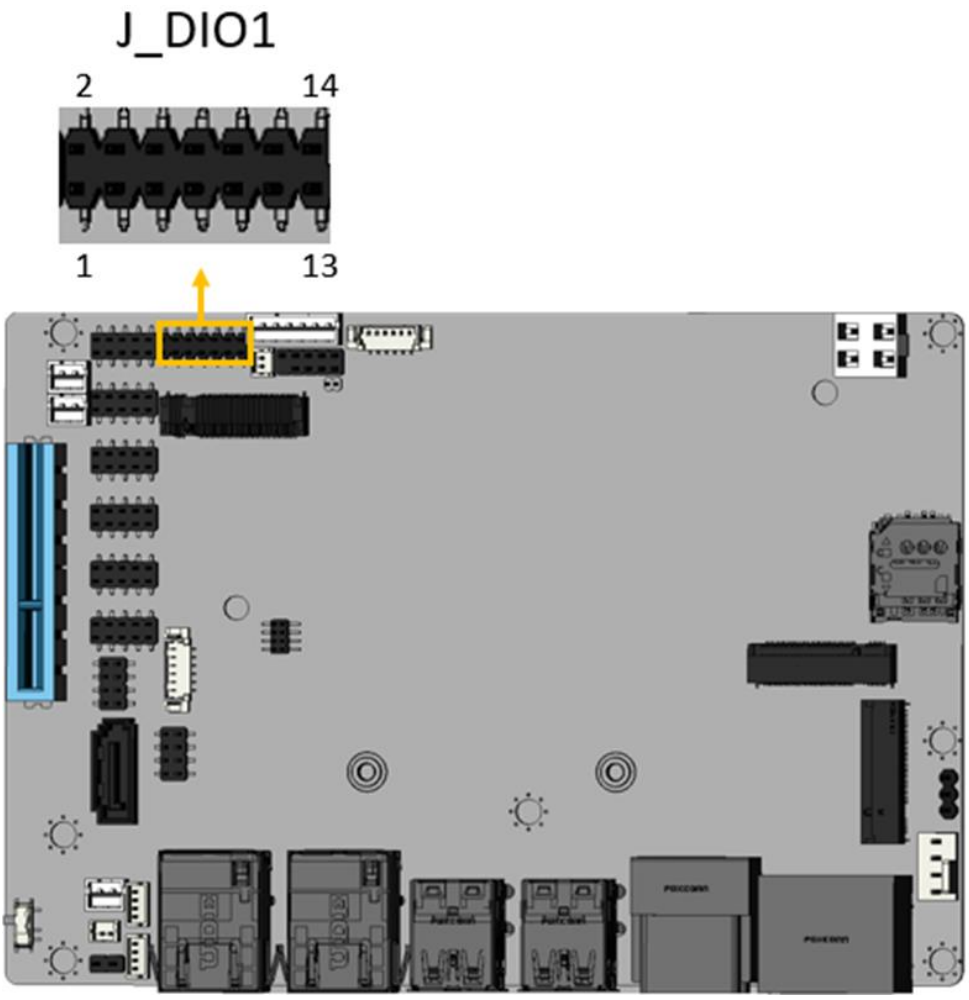


Figure 3-10: Digital I/O Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	VCC
3	Output 5	4	Output 4
5	Output 3	6	Output 2
7	Output 1	8	Output 0
9	Input 5	10	Input 4
11	Input 3	12	Input 2
13	Input 1	14	Input 0

Table 3-11: Digital I/O Connector Pinouts

3.2.10 CPU Fan Connector

CN Label: **CPU/FAN1**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-12**

The fan connector attaches to a smart cooling fan.

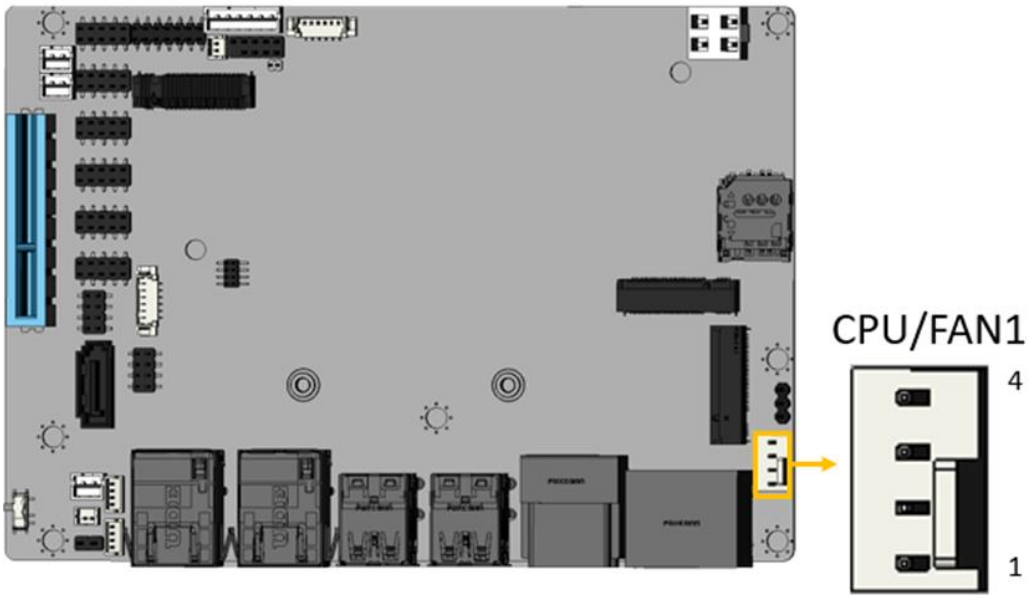


Figure 3-11: CPU Fan Connector Location

PIN NO.	Description	PIN NO.	Description
1	GND	2	+12V
3	FANIO	4	PWM (+5V)

Table 3-12: CPU Fan Connector Pinouts

3.2.11 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 6-pin wafer, p=2.00 mm

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-13**

The front panel connector connects to the power LED indicator and HDD LED indicator on the system front panel.

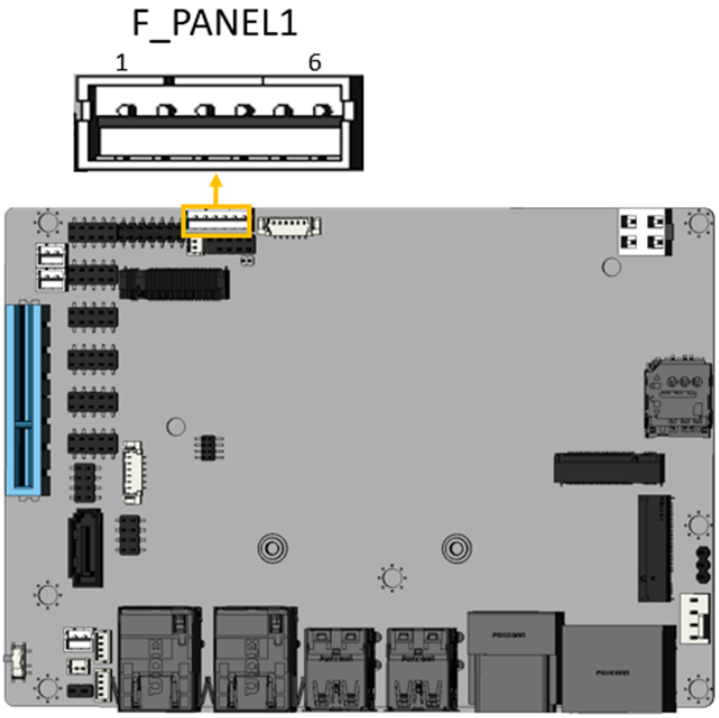


Figure 3-12: Front Panel Connector Location

PIN NO.	Description	PIN NO.	Description
1	VCC	2	GND
3	PWR_LED+	4	PWR_LED-
5	HDD_LED+	6	HDD_LED-

Table 3-13: Front Panel Connector Pinouts

3.2.12 Power Button Connector

CN Label: **PWR_BTN1**

CN Type: 2-pin wafer, p=2.00 mm

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-14**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

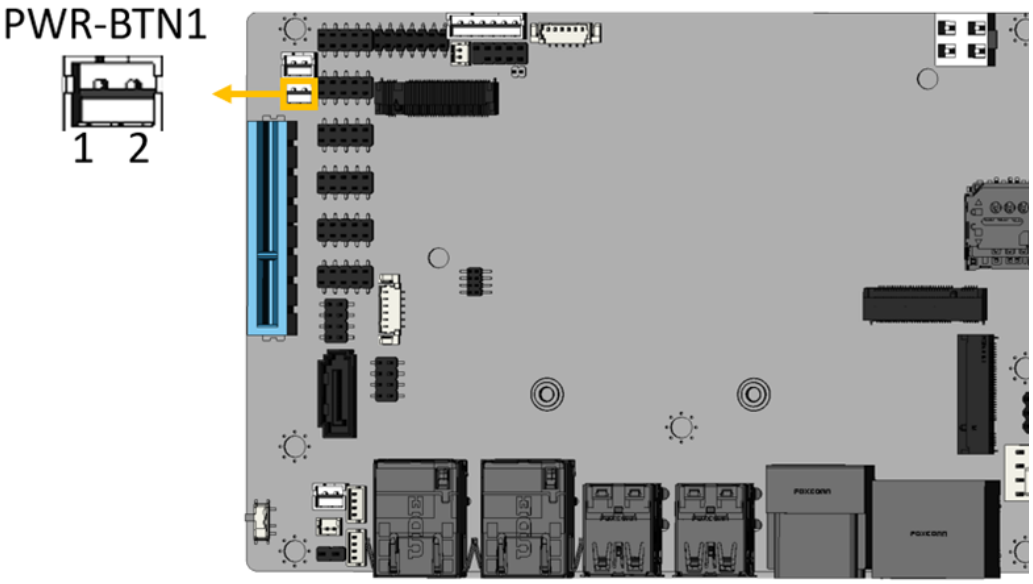


Figure 3-13: Power Button Connector Location

PIN	DESCRIPTION
1	PWRBTN_SW#
2	GND

Table 3-14: Power Button Connector Pinouts

3.2.13 Reset Button Connector

CN Label: **RST_BTN1**

CN Type: 2-pin wafer, p=2.00 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-15**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

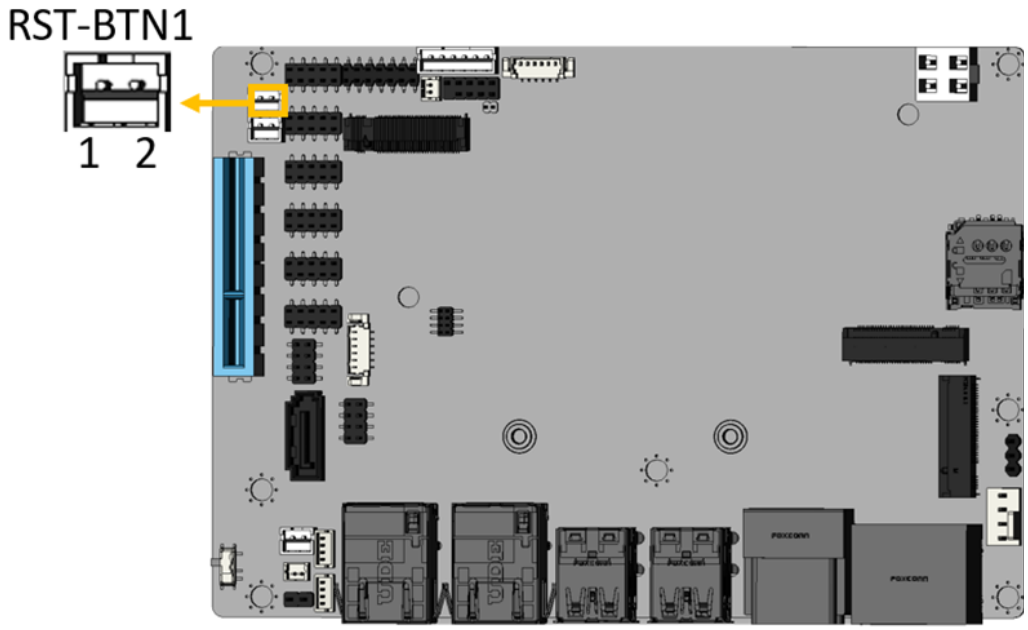


Figure 3-14: Reset Button Connector Location

PIN	DESCRIPTION
1	EXTRST-
2	GND

Table 3-15: Reset Button Connector Pinouts

3.2.14 RS-232 Serial Port Connectors

CN Label: **COM1, COM2, COM3, COM4**

CN Type: 10-pin wafer, p=2.00 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-16**

The serial connector provides RS-232 connection.

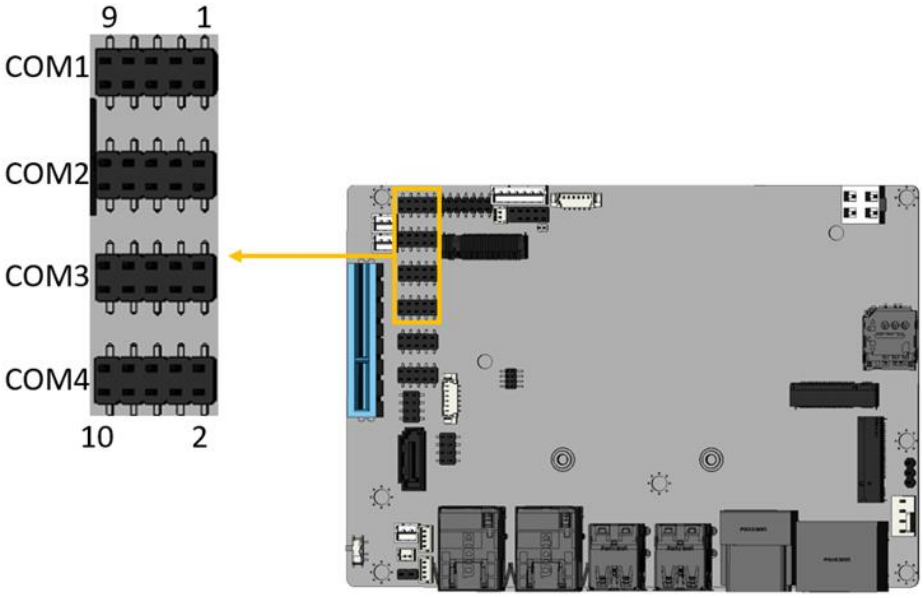


Figure 3-15: RS-232 Serial Port Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	GND

Table 3-16: RS-232 Serial Port Connectors Pinouts

3.2.15 RS-232/422/485 Serial Port Connectors

CN Label: **COM5, COM6**

CN Type: 10-pin wafer, p=2.00 mm

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-17**

The serial connector provides RS-232/422/485 connection.

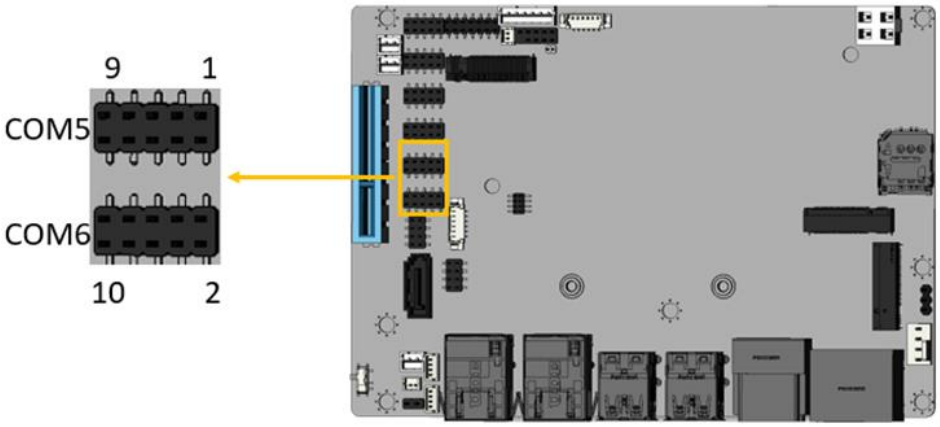


Figure 3-16: RS-232/422/485 Serial Port Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	GND

Table 3-17: RS-232/422/485 Serial Port Connectors Pinouts

3.2.16 SATA 6Gb/s Connector

CN Label: **SATA1**

CN Type: 7-pin SATA connector, p=1.27 mm

CN Location: See **Figure 3-17**

CN Pinouts: See **Table 3-18**

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

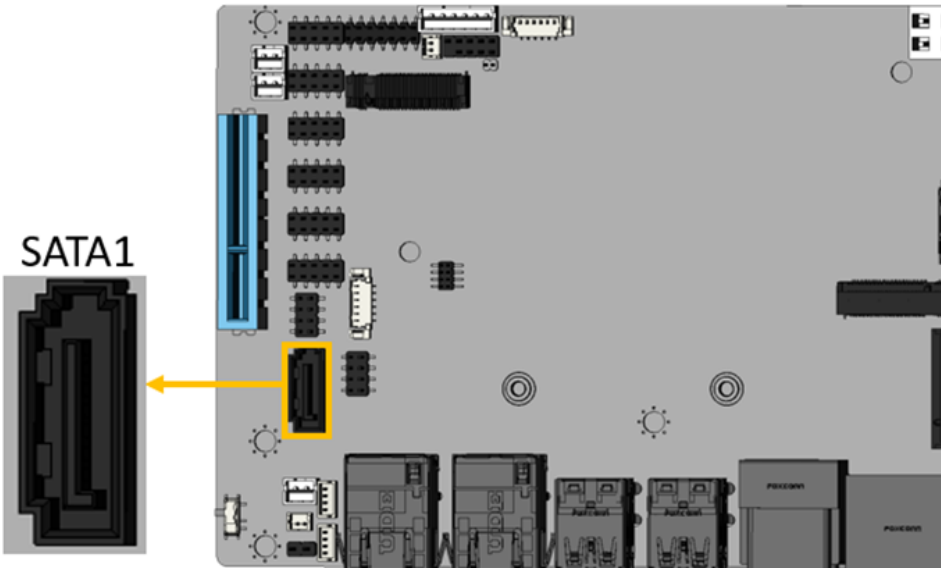


Figure 3-17: SATA 6Gb/s Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	5	SATA_RX-
2	SATA_TX+	6	SATA RX+
3	SATA_TX-	7	GND
4	GND		

Table 3-18: SATA 6Gb/s Connector Pinouts

3.2.17 SATA Power Connector

CN Label: **SATA_PWR1**

CN Type: 2-pin wafer, p=2.00 mm

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-19**

The SATA power connector provides +5 V power output to the SATA connector.

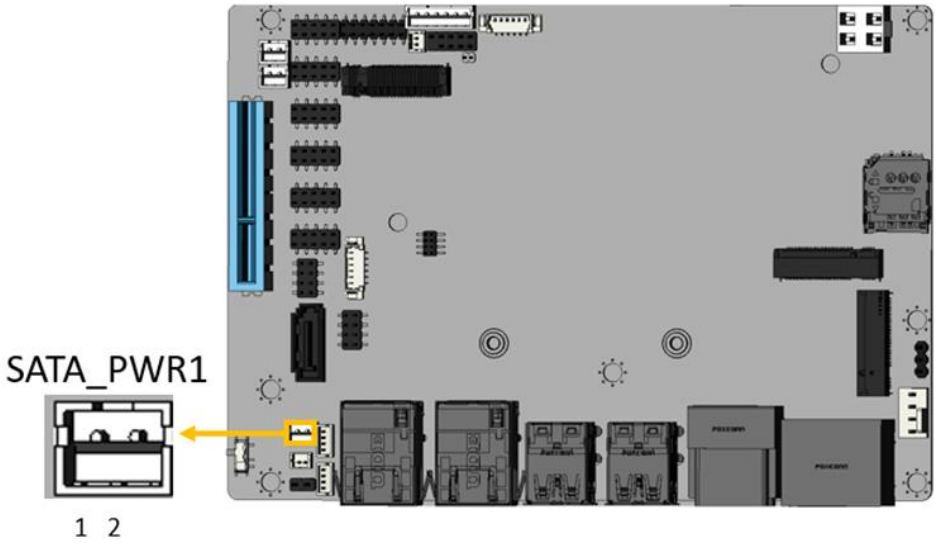


Figure 3-18: SATA Power Connector Location

PIN NO.	DESCRIPTION
1	VCC5V
2	GND

Table 3-19: SATA Power Connector Pinouts

3.2.18 I²C Connector

CN Label: **J_I2C1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-20**

The SMBus (System Management Bus) connector provides low-speed system management communications.

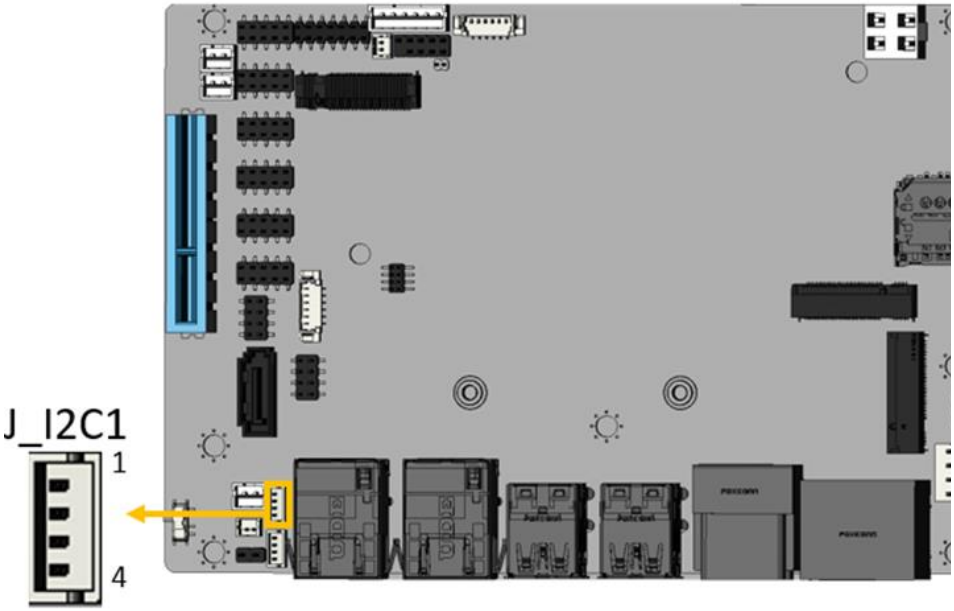


Figure 3-19: I²C Connector Location

PIN NO.	DESCRIPTION
1	GND
2	SMB_DATA_EC
3	SMB_CLK_EC
4	+5V

Table 3-20: I² C Connector Pinouts

3.2.19 SMBus Connector

CN Label: **J_SMB1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-21**

The SMBus is a two-wire bus used for communication with low bandwidth devices on a motherboard such as power related chips and temperature sensors.

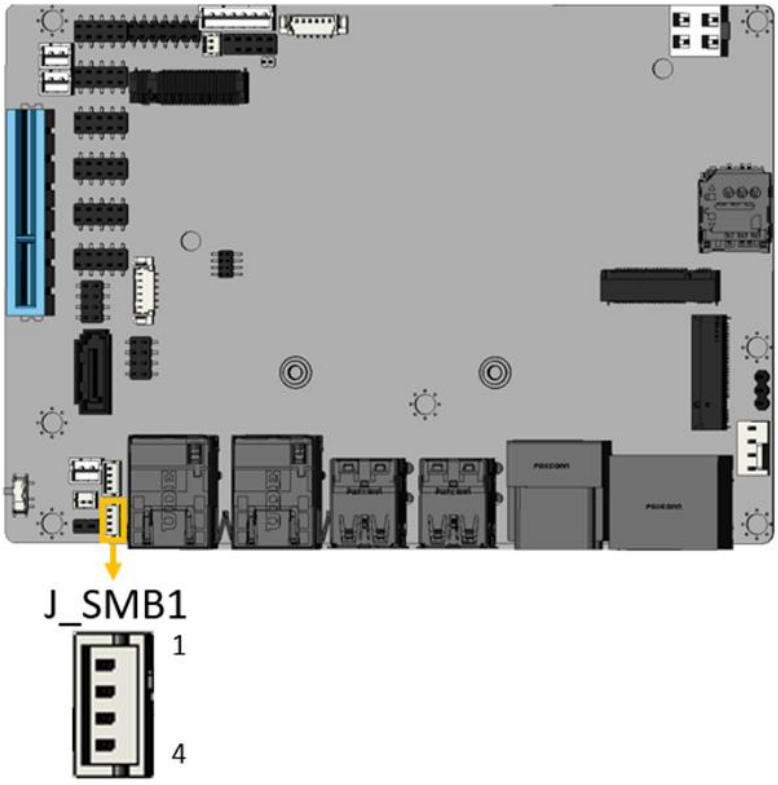


Figure 3-20: SMBus Connector Location

PIN NO.	DESCRIPTION
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-21: SMBus Connector Pinouts

3.2.20 Flash SPI ROM Connector

CN Label: **J_SPI1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-22**

The 6-pin Flash SPI ROM connector is used to flash the BIOS.

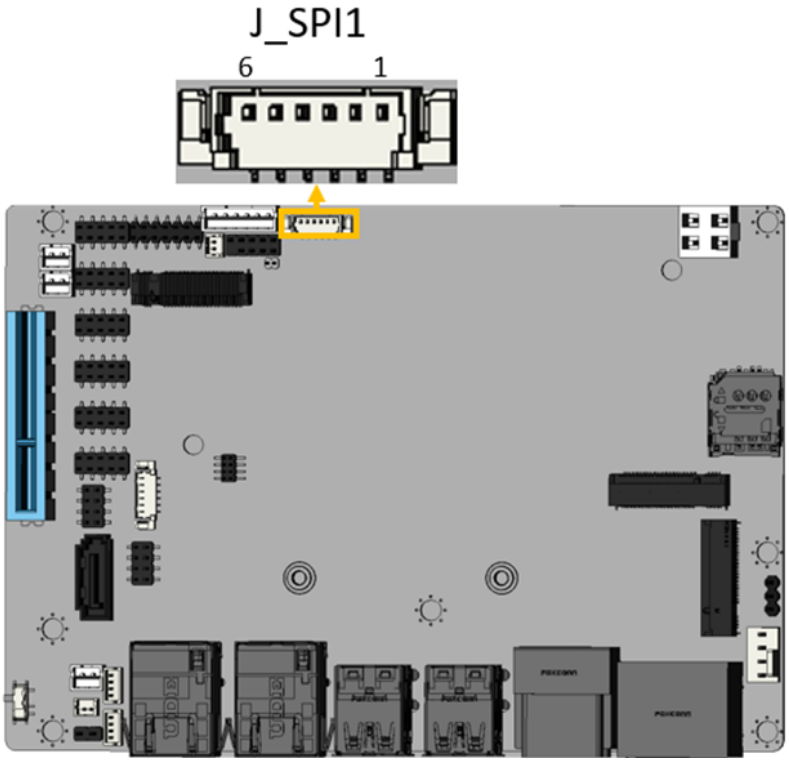


Figure 3-21: Flash SPI ROM Connector Location

PIN NO.	DESCRIPTION
1	+3.3V
2	SPI_CS#
3	SPI SO
4	SPI CLK
5	SPI SI
6	GND

Table 3-22: Flash SPI ROM Connector Pinouts

3.2.21 Flash EC ROM Connector

CN Label: **EC_SPI1**

CN Type: 8-pin header, p=1.27 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-23**

The 8-pin Flash EC ROM connector is used to flash the EC internal ROM.

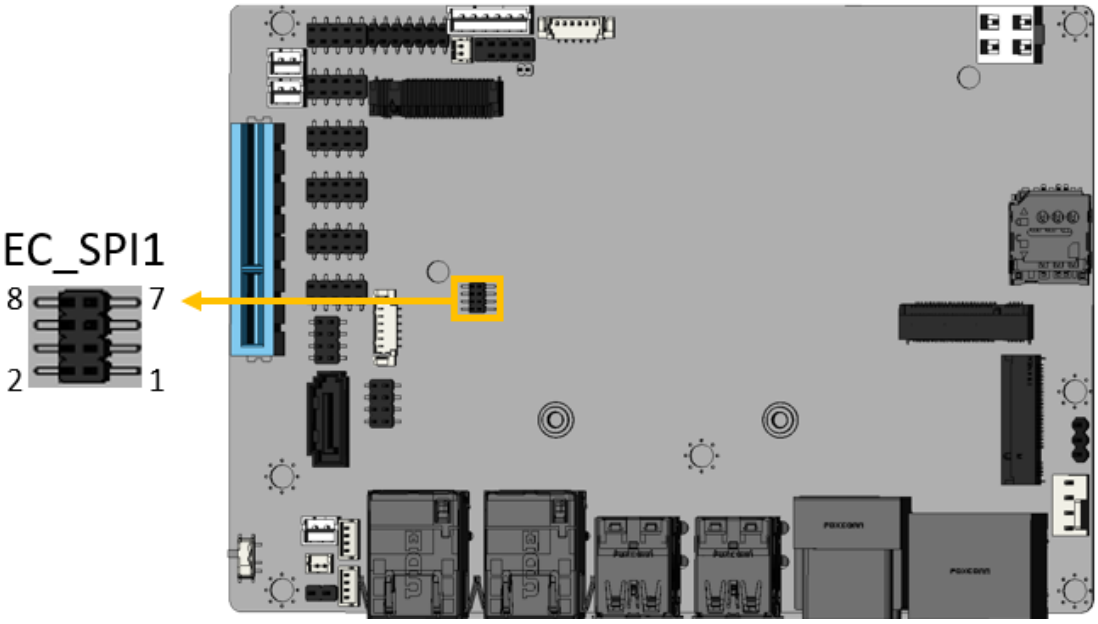


Figure 3-22: Flash EC ROM Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	CS	2	VCC3.3V
3	MISO	4	HOLD
5	DET#	6	CLK
7	GND	8	MOSI

Table 3-23: Flash EC ROM Connector Pinouts

3.2.22 EC Debug Connector

CN Label: **EC_DBG1**

CN Type: 6-pin header, p=1.25 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-24**

The EC_DBG1 connector is used for EC debug (with SPI protocol).

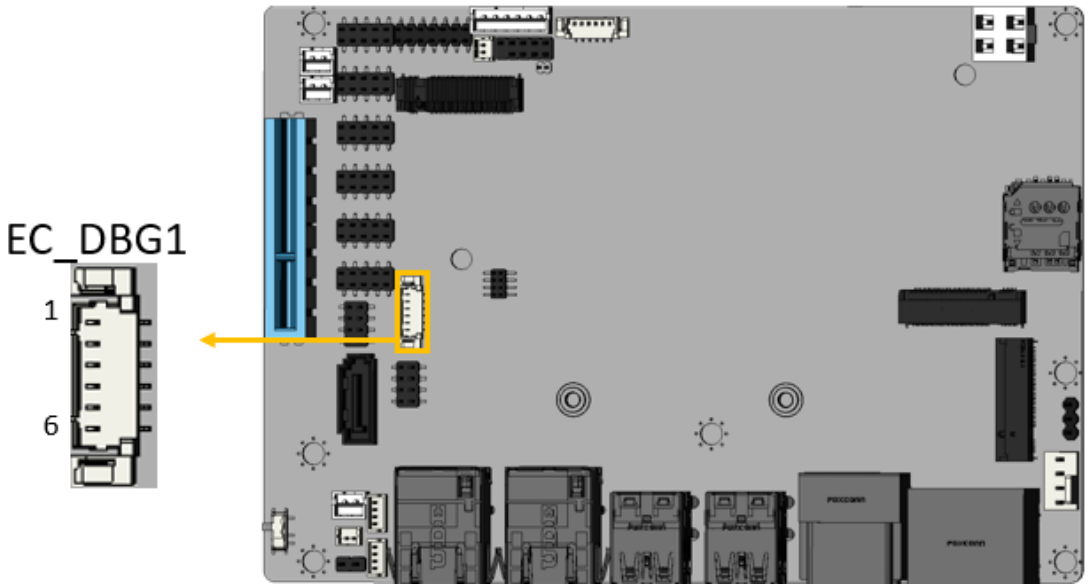


Figure 3-23: EC Debug Connector Location

Pin	Description	Pin	Description
1	NC	2	EDICS
3	EDIDO	4	EDICLK
5	EDIDI	6	GND

Table 3-24:EC Debug Connector Pinouts

3.2.23 MP2960GQKT FW Flash Connector

CN Label: **J1**

CN Type: 3-pin header, p=2.54 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-25**

Use the J1 connector to flash the firmware of MP2960GQKT PWM IC.

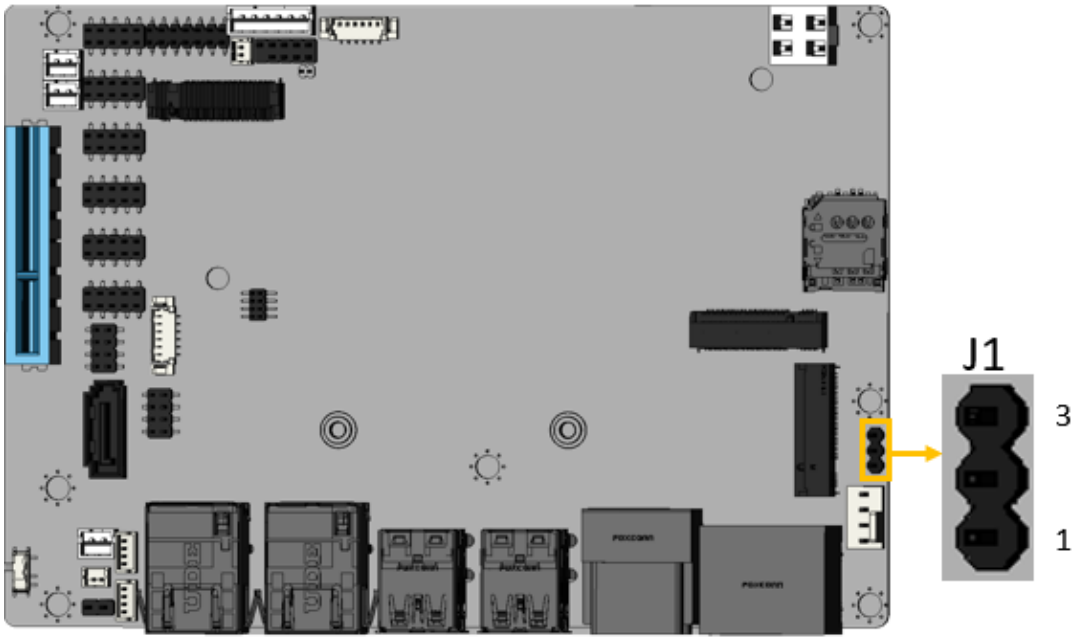


Figure 3-24: MP2960GQKT FW Flash Connector Location

Pin	Description	Pin	Description
1	PM_SCL	2	PM_SDA
3	GND		

Table 3-25: MP2960GQKT FW Flash Connector Pinouts

3.2.24 Internal USB 2.0 Connectors

CN Label: **USB2_1, USB2_2**

CN Type: 8-pin header, p=2.00 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-26**

Each USB connector provides two USB 2.0 ports by dual-port USB cable.

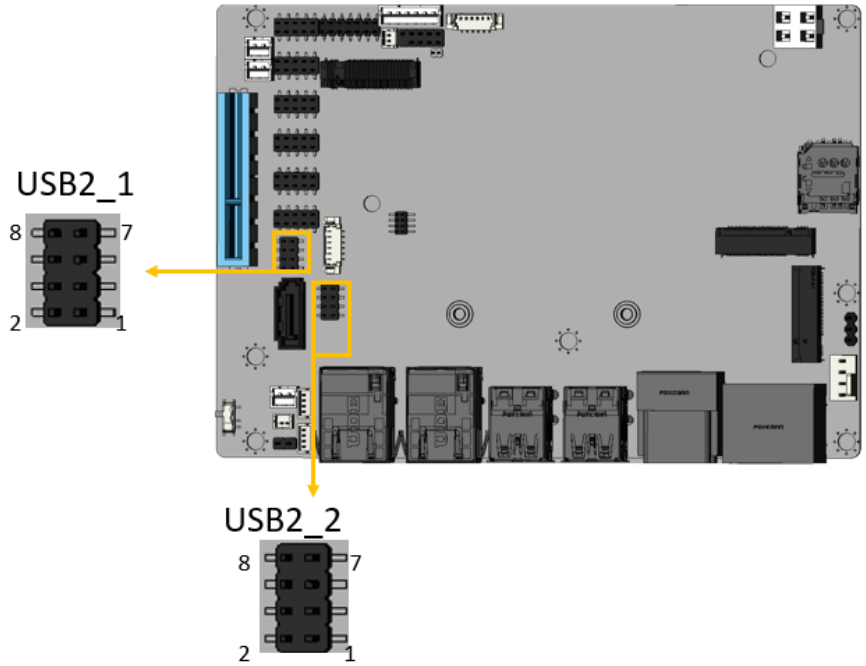


Figure 3-25: Internal USB 2.0 Connectors Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

Table 3-26: Internal USB 2.0 Connectors Pinouts

3.2.25 M.2 2242/2280 M Key Slot

CN Label: **M2_M1**

CN Type: M.2 M-key slot

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-27**

The M.2 slot is keyed in the M position. The M.2 slot supports PCIe Gen4 x4 signals.

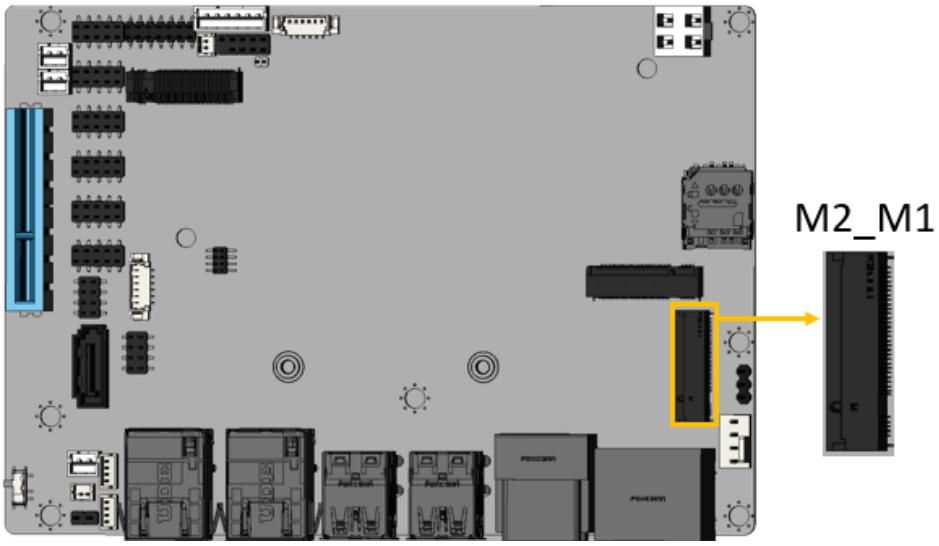


Figure 3-26: M.2 2242/2280 M-key Slot Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+V3.3
3	GND	4	+V3.3
5	PCIE_3_RX_DN	6	NC
7	PCIE_3_RX_DP	8	NC
9	GND	10	NGFF1_ACT_N
11	PCIE_3_TX_DN	12	+V3.3
13	PCIE_3_TX_DP	14	+V3.3
15	GND	16	+V3.3
17	PCIE_2_RX_DN	18	+V3.3
19	PCIE_2_RX_DP	20	NC
21	GND	22	NC

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
23	PCIE_2_TX_DN	24	NC
25	PCIE_2_TX_DP	26	NC
27	GND	28	NC
29	PCIE_1_RX_DN	30	NC
31	PCIE_1_RX_DP	32	NC
33	GND	34	NC
35	PCIE_1_TX_DN	36	NC
37	PCIE_1_TX_DP	38	M_2_SSD_SLP
39	GND	40	NC
41	PCIE_0_RX_DN	42	NC
43	PCIE_0_RX_DP	44	NC
45	GND	46	NC
47	PCIE_0_TX_DN	48	NC
49	PCIE_0_TX_DP	50	SLOT_RST
51	GND	52	NC
53	PCIE_CLK_DN	54	NC
55	PCIE_CLK_DP	56	NC
57	GND	58	NC
59	Module Key	60	Module Key
61	Module Key	62	Module Key
63	Module Key	64	Module Key
65	Module Key	66	Module Key
67	NC	68	NC
69	NC	70	+V3.3
71	GND	72	+V3.3
73	GND	74	+V3.3
75	GND		

Table 3-27: M.2 2242/2280 M-Key Slot Pinouts

3.2.26 M.2 2230 A-key Slot

CN Label: **M2_A1**

CN Type: M.2 A-key slot

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-28**

The M.2 slot is keyed in the A position and accepts 2230 size of M.2 modules. The M.2 slot supports PCIe Gen3 x1 and USB 2.0 signals.

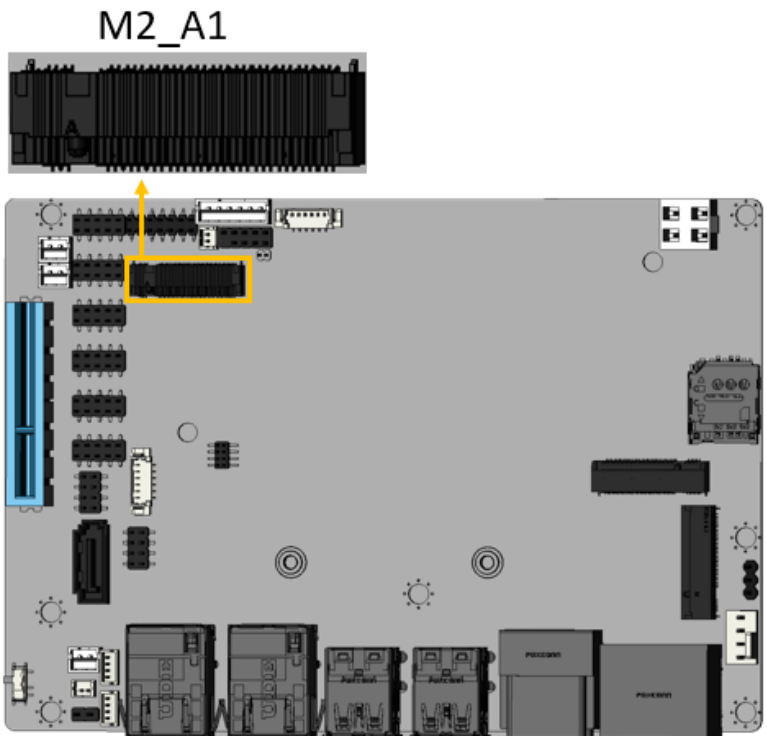


Figure 3-27: M.2 2230 A-key Slot Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+3.3V
3	USB2_DP	4	+3.3V
5	USB2_DN	6	NC
7	GND	8	Module Key
9	Module Key	10	Module Key
11	Module Key	12	Module Key

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
13	Module Key	14	Module Key
15	Module Key	16	NC
17	NC	18	GND
19	NC	20	NC
21	NC	22	NC
23	GND	24	GND
27	NC	28	NC
29	GND	30	GND
31	NC	32	NC
33	GND	34	NC
35	PCIE_TX_DP	36	GND
37	PCIE_TX_DN	38	WLAN_CL_RST_N
39	GND	40	WLAN_CL_DATA
41	PCIE_RX_DP	42	WLAN_CL_CLK
43	PCIE_RX_DN	44	NC
45	GND	46	NC
47	PCIE_CLK+	48	NC
49	PCIE_CLK-	50	NC
51	GND	52	SLOT_RST
53	NC	54	+3.3V
55	M.2_A_WAKE	56	+3.3V
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	GND	64	NC
65	NC	66	NC
67	NC	68	NC
69	GND	70	NC
71	NC	72	+3.3V
73	NC	74	+3.3V
75	GND		

Table 3-28: M.2 2230 A-Key Slot Pinouts

3.2.27 M.2 3042 B-key Slot

CN Label: **M2_B1**

CN Type: M.2 B-key slot

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-29**

The M.2 3042 B key slot with PCIe Gen3 x2 and USB 2.0 signal supports NVMe storage or 5G module with SIM holder

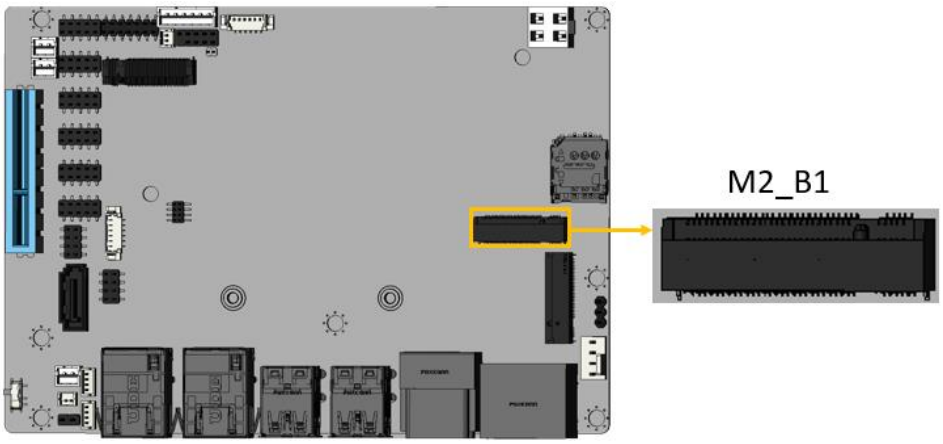


Figure 3-28: M.2 3042 B-key Slot Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+V3.3
3	GND	4	+V3.3
5	GND	6	NC
7	USB2_DP	8	W_DISABLE_N
9	USB2_DN	10	NC
11	GND	12	Module Key
13	Module Key	14	Module Key
15	Module Key	16	Module Key
17	Module Key	18	Module Key
19	Module Key	20	NC
21	GND	22	NC
23	M.2_B_WAKE	24	NC

25	NC	26	NC
27	GND	28	NC
29	PCIE_1_RX_DN	30	SIM_RST
31	PCIE_1_RX_DP	32	SIM_CLK
33	GND	34	SIM_CIO
35	PCIE_1_TX_DN	36	SIM_VCC
37	PCIE_1_TX_DP	38	NC
39	GND	40	NC
41	PCIE_0_RX_DN	42	NC
43	PCIE_0_RX_DP	44	NC
45	GND	46	NC
47	PCIE_0_TX_DN	48	NC
49	PCIE_0_TX_DP	50	SLOT_RST
51	GND	52	NC
53	PCIE_CLK_DN	54	M.2_B_WAKE
55	PCIE_CLK_DP	56	NC
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC
65	NC	66	NC
67	NC	68	NC
69	NC	70	+V3.3
71	GND	72	+V3.3
73	GND	74	+V3.3
75	GND		

Table 3-29: M. 2 3042 B-key Slot Pinouts

3.2.28 SIM Card Slot

CN Label: **SIM1**

CN Type: 6-pin SIM holder, p=1.25mm

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-30**

The SIM card slot accepts a SIM card for 5G network communication.

NOTE:

A WWAN module must be installed in the M.2 B key slot (M2_B1) to provide WWAN communication.

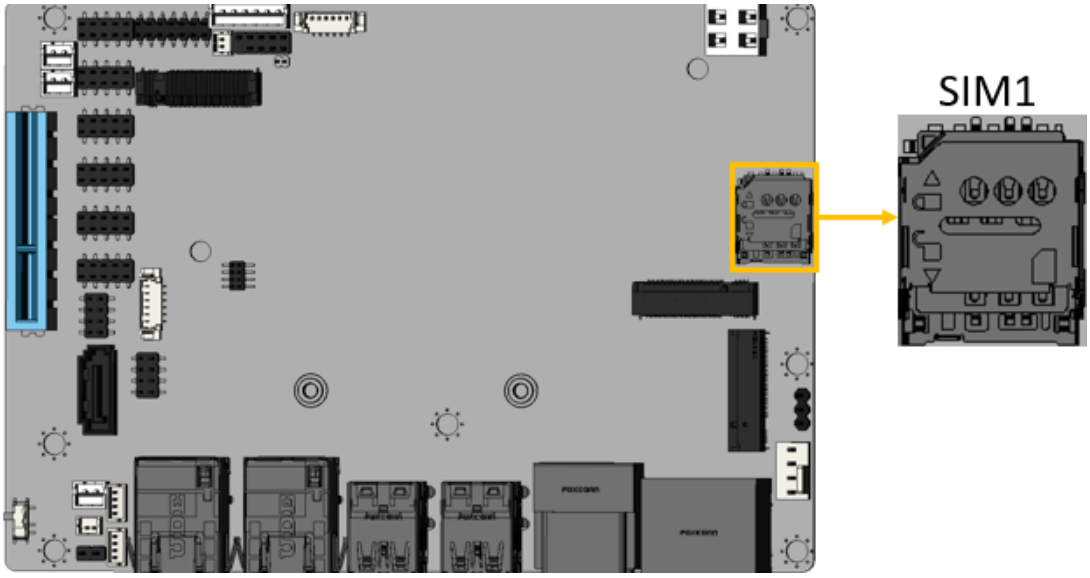


Figure 3-29: SIM Card Slot Location

PIN NO.	DESCRIPTION
C1	SIM_VCC
C2	SIM_RST
C3	SIM_CLK
C5	GND
C6	NC

C7	SIM_CIO
G1	GND
G2	GND
G3	GND
G4	GND

Table 3-30: SIM Card Slot Pinouts

3.3 External Peripheral Interface Connector Panel

Figure 3-30 shows the WAFER-ADL-P external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 2 x HDMI connector
- 2 x DP connector
- 2 x 2.5GbE RJ-45 connector
- 4 x USB 3.2 Gen 2 connector

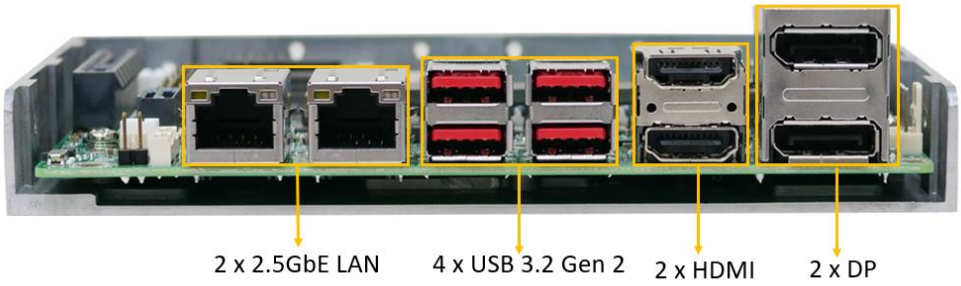


Figure 3-30: External Peripheral Interface Connector

3.3.1 External 2.5GbE RJ-45 Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-31**

CN Pinouts: See **Table 3-31** & **Table 3-32**

The LAN connector connects to a local network.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LAN1_MD0+	5	LAN1_MD2+
2	LAN1_MD0-	6	LAN1_MD2-
3	LAN1_MD1+	7	LAN1_MD3+
4	LAN1_MD1-	8	LAN1_MD3-

Table 3-31: External 2.5GbE RJ-45 Connectors Pinouts

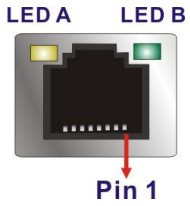


Figure 3-31: LAN LED Location

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received	B	off: 100 Mb/s orange: 1000 Mb/s green: 2500 Mb/s

Table 3-32: LAN LED Pinouts

3.3.2 External Dual DisplayPort Connector

CN Label: **DP1**

CN Type: External DP connector

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-33**

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LANE0P	11	GND
2	GND	12	LANE3N
3	LANE0N	13	CONFIG_A_1
4	LANE1P	14	CONFIG_A_2
5	GND	15	AUXP
6	LANE1N	16	GND
7	LANE2P	17	AUXN
8	GND	18	HPD
9	LANE2N	19	GND
10	LANE3P	20	+5V

Table 3-33: External DisplayPort Connector Location

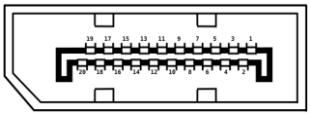


Figure 3-32: External DisplayPort Connector Pinouts

3.3.3 External Dual HDMI Connectors

CN Label: **HDMI1**

CN Type: HDMI connector

CN Location: See **Figure 3-33**

CN Pinouts: See **Table 3-34**

The HDMI connectors can connect to HDMI devices.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	HDMI_DATA2P	11	GND
2	GND	12	HDMI_CLKN
3	HDMI_DATA2N	13	N/C
4	HDMI_DATA1P	14	N/C
5	GND	15	HDMI_CLK
6	HDMI_DATA1N	16	HDMI_SDA
7	HDMI_DATA0P	17	GND
8	GND	18	+5V
9	HDMI_DATA0N	19	HDMI_HPD
10	HDMI_CLKP		

Table 3-34: External HDMI Connector Pinouts

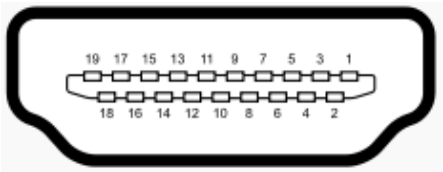


Figure 3-33: External HDMI Connector Location

3.3.4 External Dual USB 3.2 Gen 2 Connectors

CN Label: **USB3_1, USB3_2**

CN Type: USB 3.2 Gen 2 port Type-A

CN Location: See **Figure 3-34**

CN Pinouts: See **Table 3-35**

The WAFER-ADL-P has four external USB 3.2 Gen 2 ports. The USB connector can be connected to a USB 2.0 or USB 3.2 device. The pinouts of USB 3.2 Gen 2 connectors are shown below.

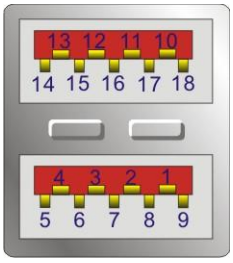


Figure 3-34: External USB 3.2 Gen 2 Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	10	VCC
2	USB_DATA-	11	USB_DATA-
3	USB_DATA+	12	USB_ DATA+
4	GND	13	GND
5	USB3_RX-	14	USB3_RX-
6	USB3_RX+	15	USB3_ RX+
7	GND	16	GND
8	USB3_TX-	17	USB3_TX-
9	USB3_TX+	18	USB3_TX+

Table 3-35: External USB 3.2 Gen 2 Connectors Pinouts

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the WAFER-ADL-P may result in permanent damage to the WAFER-ADL-P and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the WAFER-ADL-P. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the WAFER-ADL-P or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding*** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the WAFER-ADL-P, place it on an anti-static pad. This reduces the possibility of ESD damaging the WAFER-ADL-P.
- ***Only handle the edges of the PCB***: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the WAFER-ADL-P, WAFER-ADL-P components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the WAFER-ADL-P installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the WAFER-ADL-P on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the WAFER-ADL-P off:
  - When working with the WAFER-ADL-P, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the WAFER-ADL-P **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 M.2 Module Installation

The way the WAFER-EHL provides is to mount the M.2 expansion card using screws. Please follow the steps below.

Mode: Using screw

Step 1: Locate the M.2 module slot. See **Chapter 3**.

Step 2: Remove the retention screw secured on the motherboard.

Step 3: Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º (**Figure** 4-1**)**.

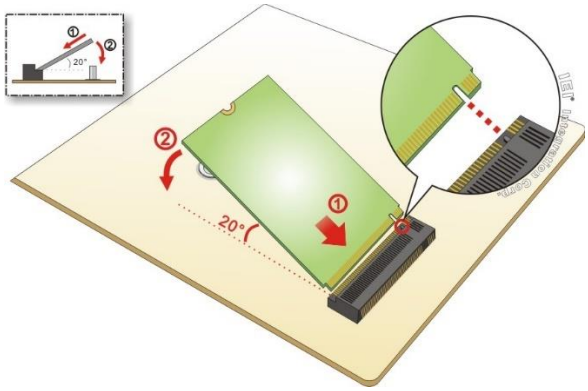


Figure 4-1: Inserting The M.2 Module Into The Slot At An Angle

Step 4: Secure the M.2 module with the previously removed retention screw (**Figure 4-2**).

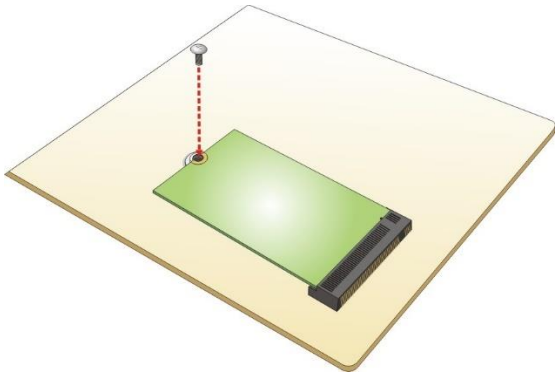


Figure 4-2: Securing The M.2 Module

4.4 Chassis Installation

4.4.1 Heat Spreader

WARNING:

The heat spreader installed on the WAFER-ADL-P can only serve as a heat conductor, which needs additional heat dissipation mechanism to achieve suitable thermal condition. DO NOT put the WAFER-ADL-P with the heat spreader directly on a surface that cannot dissipate system heat, and never run the WAFER-ADL-P without the heat spreader secured to the board.

When the WAFER-ADL-P is shipped, it is secured to a heat spreader with five retention screws. The heat spreader must have a direct contact with a heat dissipation surface to ensure stable operation. In addition, a thin layer of thermal paste has to be applied onto the heat dissipation surface where it contacts the heat spreader.

Figure 4-3: Heat Sink Retention Screws

IEI also provides two thermal solutions for customers to choose.

IEI has developed a highly efficient thermal solution for the 3.5" motherboard - IEI Heat Conduction Casing (IHCC). With its well-design structure, the IHCC can effectively improve heat transfer performance and cut time-to-market. It completely joints with the heat spreader for better CPU heat transfer in 0ºC–60ºC operating temperature using active cooling (P/N: CM-WAFER-WOF-R10, see **Figure 4-4**), and in 0ºC–45ºC operating temperature using passive cooling (P/N: CM-WAFER-WOF-R10 see **Figure 4-5).**

Figure 4-4: Passive Cooling

Figure 4-5:Active Cooling

4.5 Riser Card Installation

The WAFER-ADL-P features a PCIe x4 (PCIe x4 signal, x4 & x2+x2) slot, which is a new design of the WAFER motherboard to expand functionality. By installing an IEI-developed riser card into the PCIe slot, the x4 signal is divided into two x2 slots, offering great configuration flexibility and expandability.

Two types of riser cards with different orientation are available, one with slots facing outwards and the other with slots facing inwards.

The outwards-facing riser card (P/N: NWR-L2S-R10), although lower in height, is able to provide better spacing to ensure expansion cards to run at a low temperature. It is ideal for the chassis that is wide enough for the expansion card to be placed.

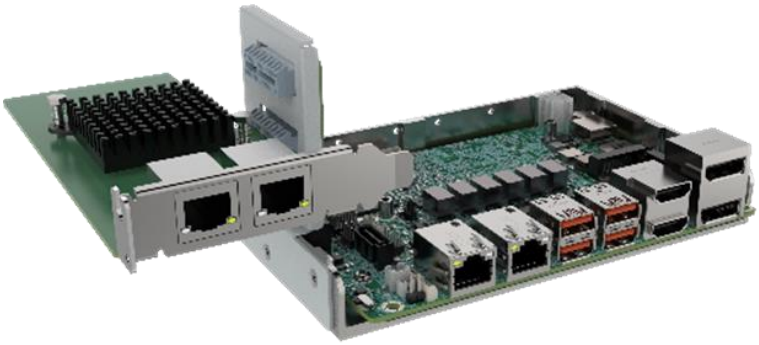


Figure 4-6:Outwards Riser Card Installation Example

Figure 4-7:NWR-L2S-R10

The inwards-facing riser card (P/N: NWR-R2S-R10) is designed with higher height to keep a decent space between the expansion cards and the motherboard. This can help improve the airflow and heat transfer within the system. It is suitable for installation where space is limited.

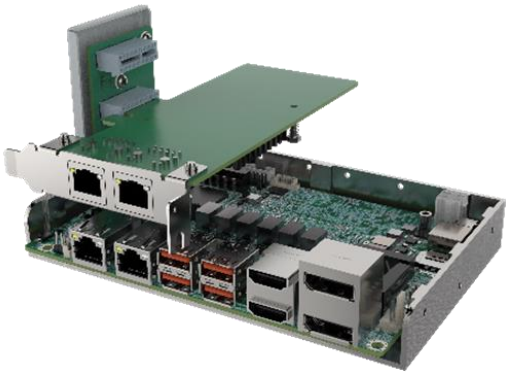


Figure 4-8: Inwards Riser Card Installation Example

Figure 4-9:NWR-R2S-R10

Both of the riser cards can be firmly secured to enhance stability by using the L-shaped bracket, in which screw holes are perfectly matched with those on the side of the heat spreader to make it simple and easy to install. See **Figure 4-10**.

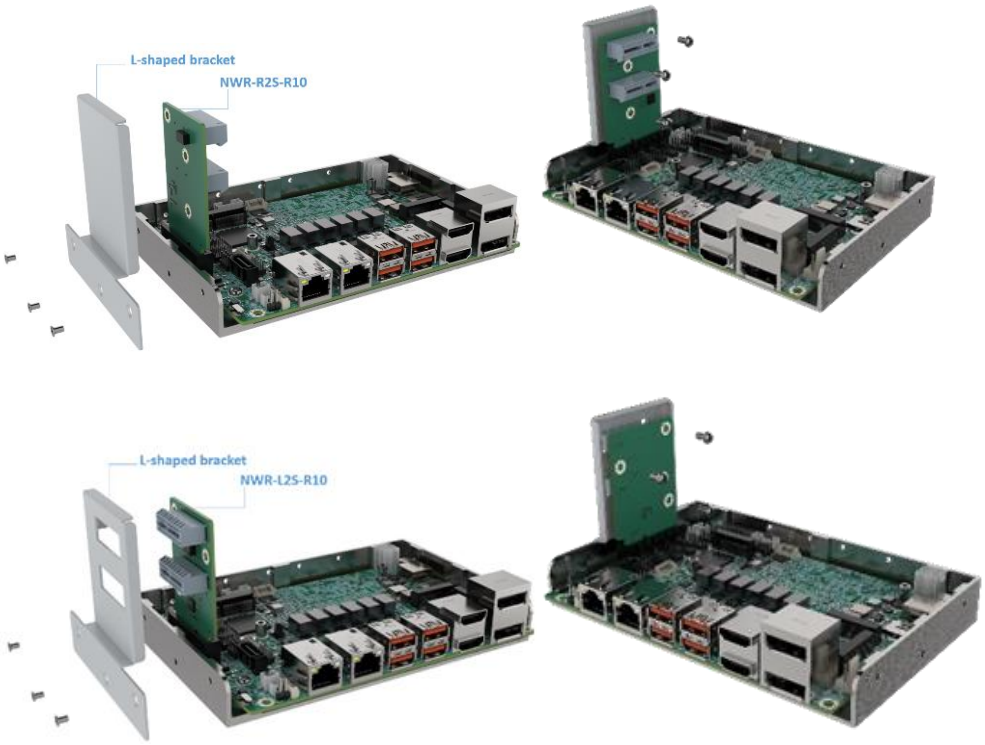


Figure 4-10:L-shaped Bracket Installation Example

4.6 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

4.6.1 AT Power Connection

Follow the instructions below to connect the WAFER-ADL-P to an AT power supply.

WARNING:

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the WAFER-ADL-P.

Step 1: **Locate the power cable**. The power cable is shown in the packing list in **Chapter 2**.

Step 2: **Connect the power cable to the motherboard**. Connect the 4-pin (2x2) Molex type power cable connector to the power connector on the motherboard. See **Figure 4-11**

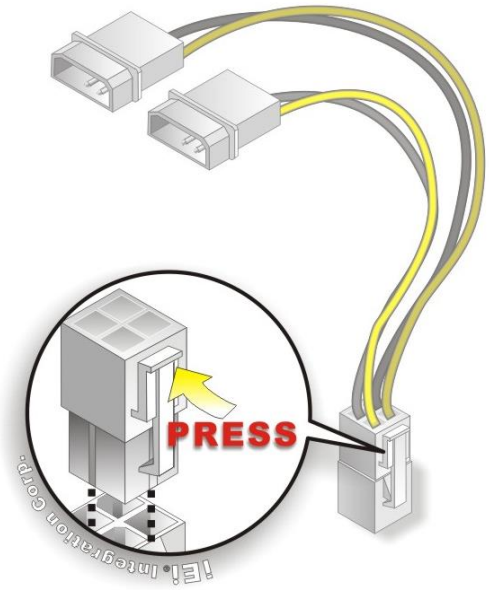


Figure 4-11: Power Cable to Motherboard Connection

Step 3: **Connect power cable to power supply**. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT power supply. See **Figure 4-12**

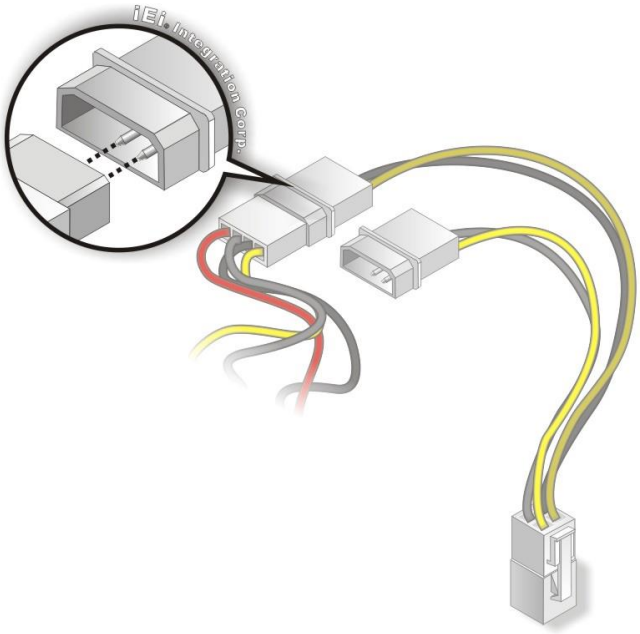


Figure 4-12: Connect Power Cable to Power Supply

4.6.2 7.1 Channel Audio Kit Installation

NOTE:

This item must be ordered separately, and connects to the audio connector. For further information please contact the nearest distributor, reseller or vendor or contact an IEI sales representative directly.

The audio kit attaches to the audio connector. The audio kit provides 7.1 channel audio. To install the audio kit, please refer to the steps below:

Step 1: **Connect the cable to the audio kit.** Connect the included cable to the audio kit. Make sure pin 1 aligns with the marked pin.

Step 2: **Conect the cable to the board**. Connect the other end of the cable to the board. Make sure to line up the marked pin 1.

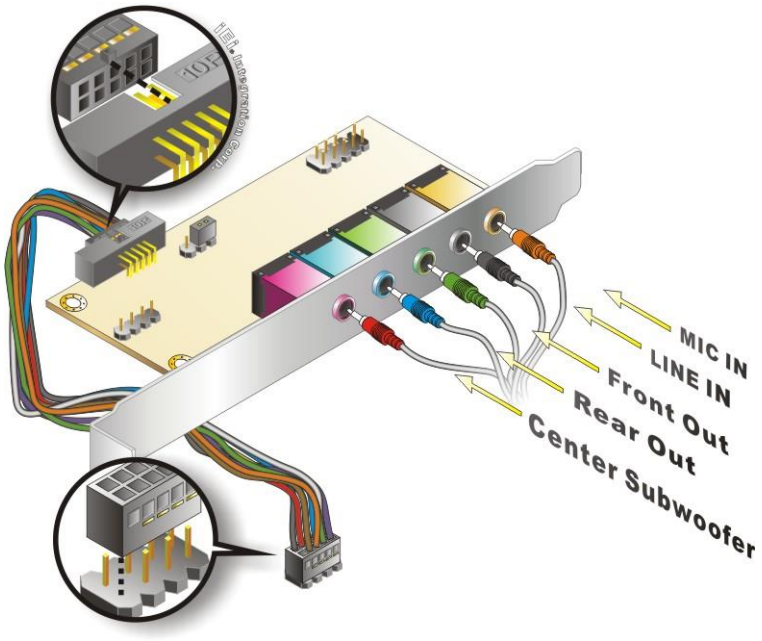


Figure 4-13: 7.1 Channel Audio Kit

Step 3: **Mount the audio kit onto the chassis**. Once the audio kit is connected to the board, secure the audio kit bracket to the system chassis.

Step 4: **Connect the audio devices**. Connect speakers and external audio sources to the audio jacks on the audio kit.

Step 5: **Install the driver**. Install the 7.1 channel audio driver included with the board.

4.6.3 SATA Drive Connection

The WAFER-ADL-P is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

Step 1: **Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-14**.

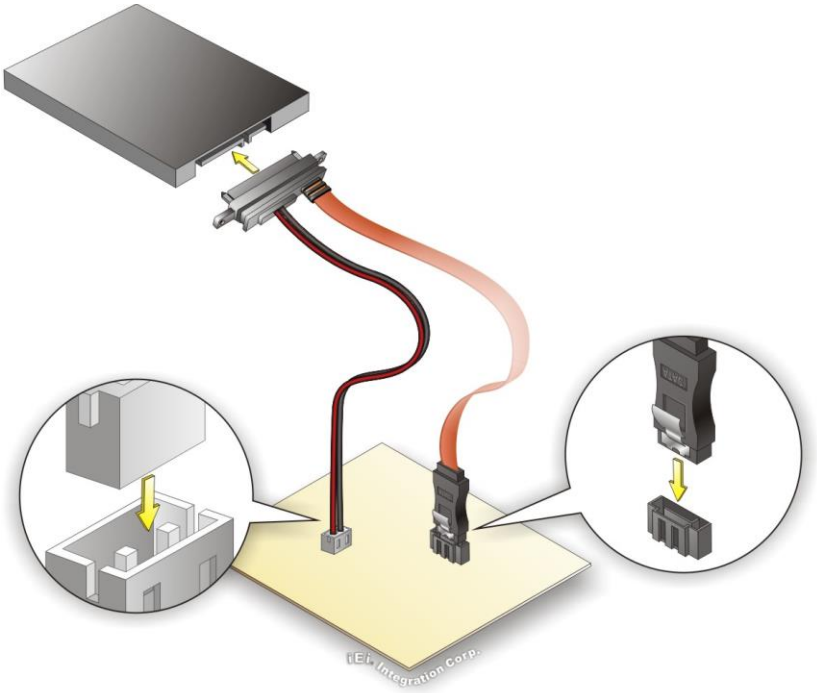


Figure 4-14: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive.

Step 4: To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

4.7 Software Drivers

4.7.1 Available Drivers

All the drivers for the WAFER-ADL-P are available on IEI Resource Download Center (https://download.ieiworld.com). Type WAFER-ADL-P and press Enter to find all the relevant software, utilities, and documentation.

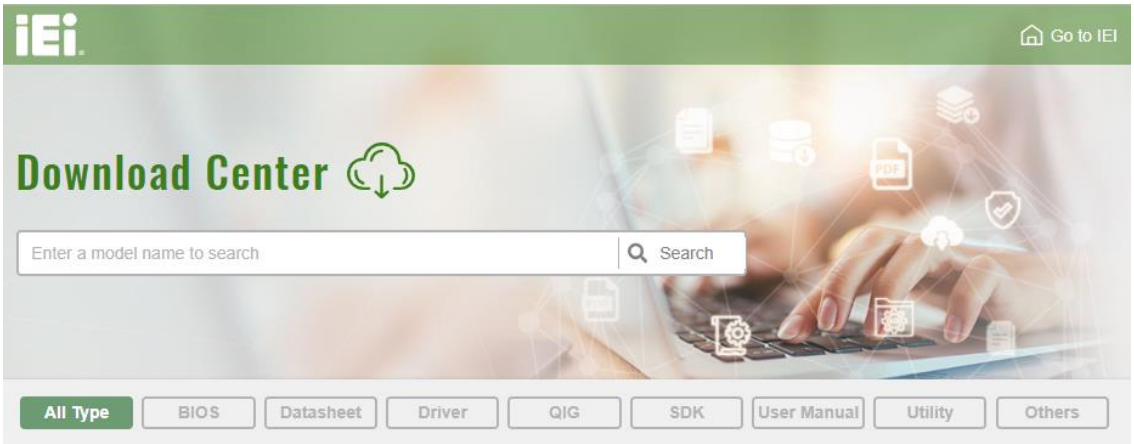
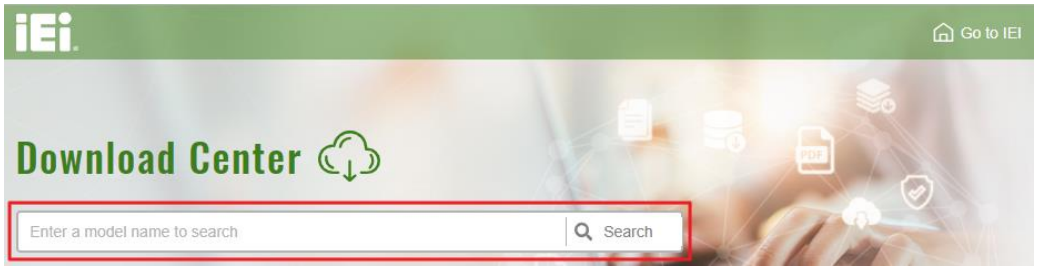


Figure 4-15: IEI Resource Download Center

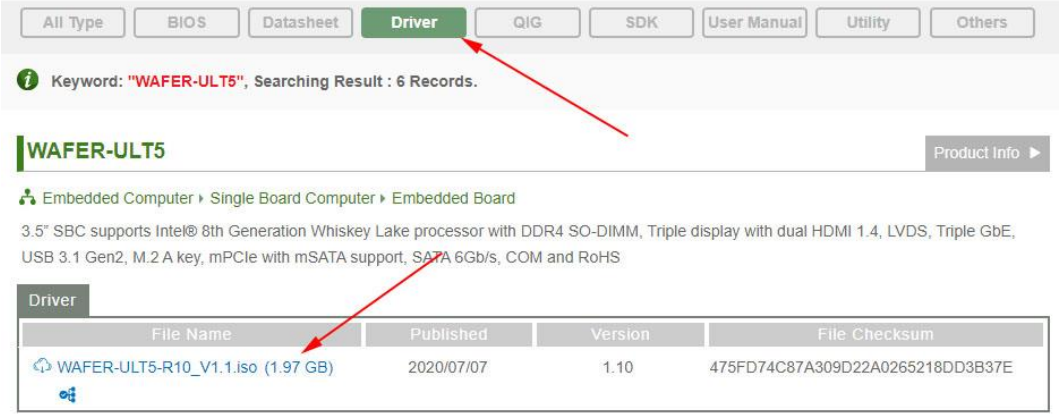
4.7.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

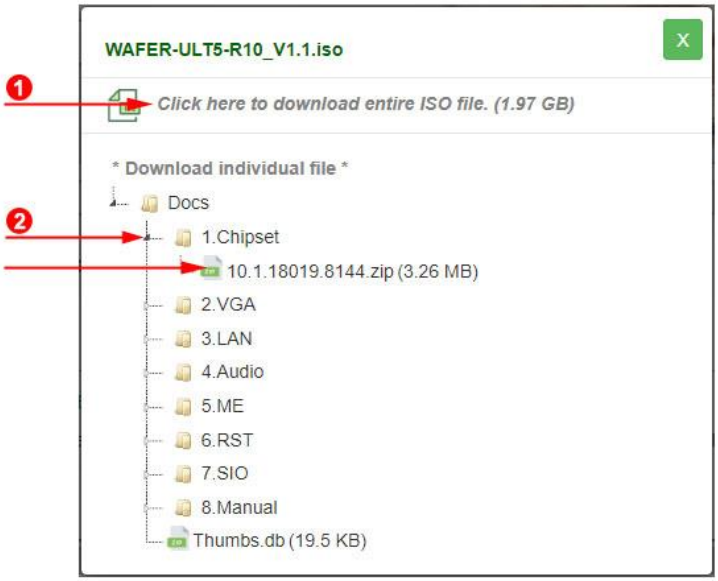
Step 1: Go to https://download.ieiworld.com. Type WAFER-ADL-P and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard**: Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen**: Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

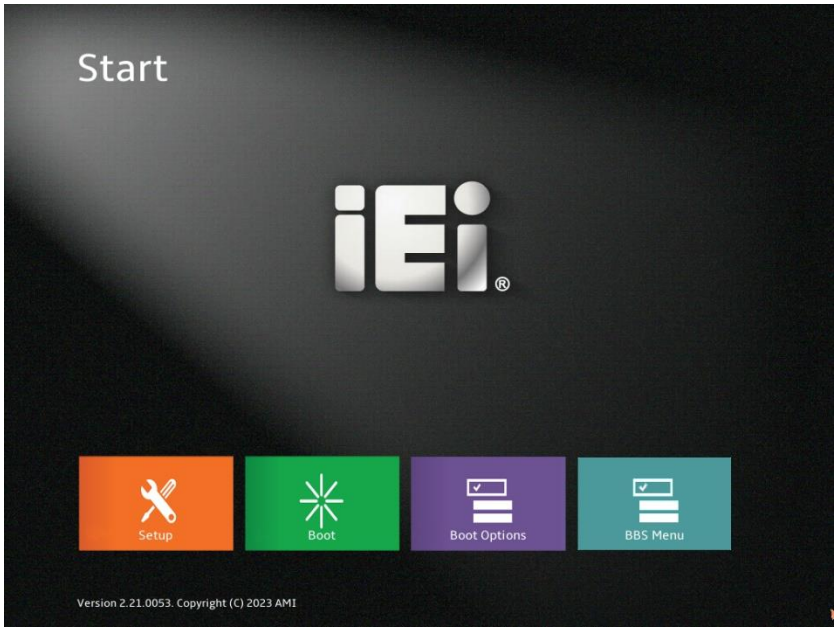


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

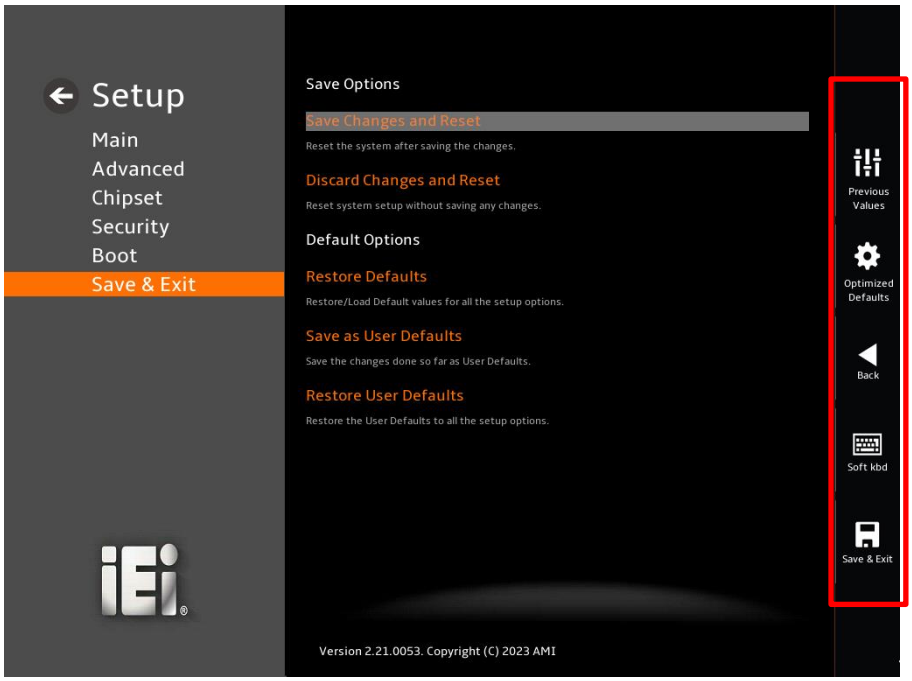
For keyboard navigation, use the navigation keys shown in **Table 5-1**.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1 & BIOS Menu 2**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.

BIOS Menu 1:Main (1/2)

BIOS Menu 2: Main (2/2)

➔ BIOS Information

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliancy:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **Access Level:** Current Access Administrator
- **EC Version:** Current EC version

➔ **Processor Information**

The **Processor Information** lists a brief summary of the Processor. The fields in **Processor Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the Processor Details
- **Type:** Displays the Processor Type
- **Speed:** Displays the Processor Speed
- **ID:** Displays the Processor ID
- **Stepping:** Displays the Processor Stepping
- **Microcode Revision:** CPU Microcode Revision
- **Total Memory:** Total Memory in the System
- **Memory Frequency:** Displays Frequency of Memory

➔ **PCH Information**

The **PCH Information** lists a brief summary of the PCH. The fields in **PCH Information** cannot be changed. The items shown in the system overview include:

- **Name:** Displays the PCH Name
- **PCH SKU:** Displays the PCH SKU
- **Stepping:** Displays the PCH Stepping
- **ME FW Version:** Displays the ME Firmware Version
- **ME Firmware SKU:** Displays the ME Firmware SKU
- **System Date:** Displays the System Date

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx: xx: xx]**

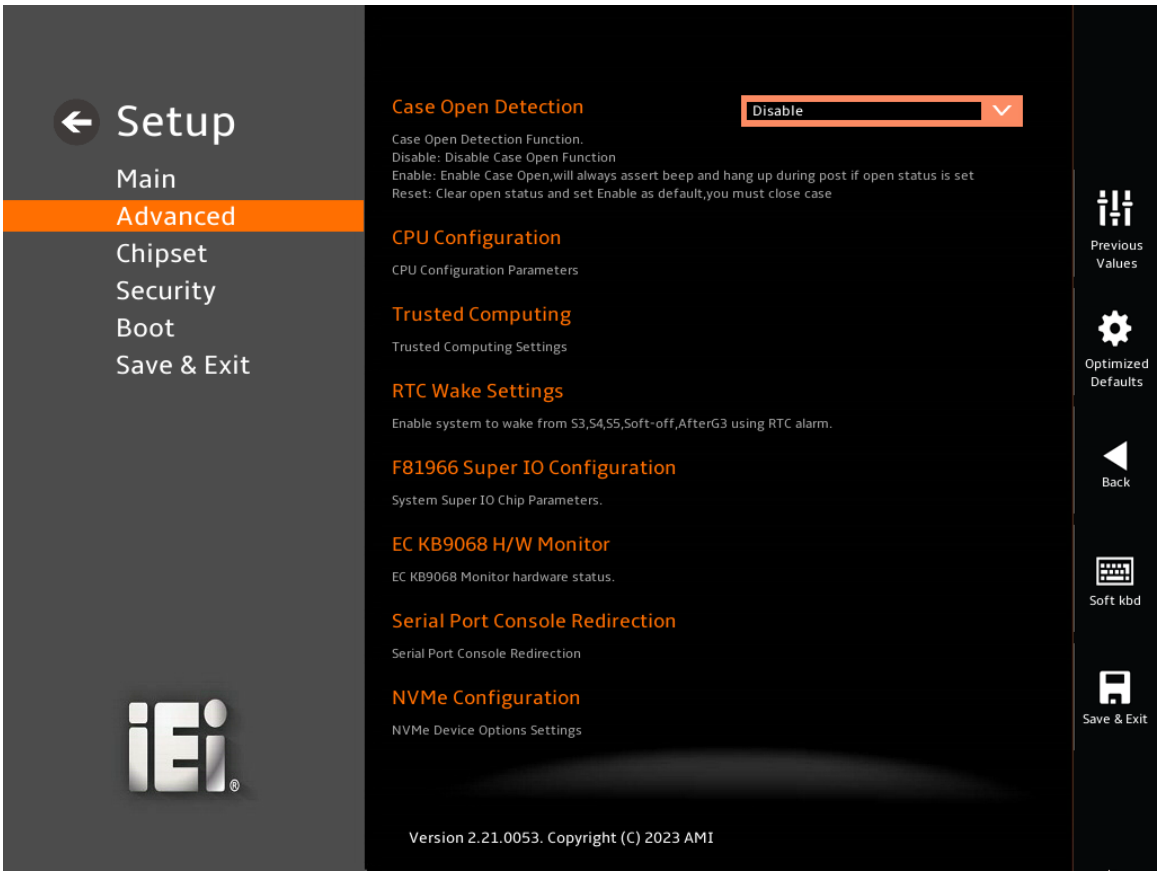
Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 3**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 3:Advanced

5.3.1 Case Open Detection

Use the **Advanced** menu (**BIOS Menu 4)** to case open detection function.

➔ **Case Open Detection [Disable]**

Case open detection function.

- ➔ **Disable:** Disabled Case Open Function.
- ➔ **Enable:** Enable Case open, will always assert beep and hang up during post if open status is set
- ➔ **Reset:** Clear open status and set Enables as default, you must close case

BIOS Menu 4: Case open detection

5.3.2 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 5 & BIOS Menu 6**) to view detailed CPU specifications or enable the Intel Virtualization Technology.

BIOS Menu 5: CPU Configuration (1/2)

BIOS Menu 6: CPU Configuration (2/2)

➔ Intel (VMX) Virtualization Technology [Enabled]

Use the **Intel (VMX) Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

➔ **Disabled**		Disables Intel Virtualization Technology.
➔ **Enabled**	**DEFAULT**	Enables Intel Virtualization Technology.

➔ Power Limit 1

Use the **Power Limit 1** to set Power Limit in Milli Watts. BIOS will round to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power limit and TDP Limit. If value is 0, BIOS will program TDP value.

➔ **Power Limit 2**

Use the **Power Limit 2** to set Power Limit in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*TDP. For 12.50W, enter 12500. Processor applies control policies such that the package power does not exceed this limit.

➔ **Power Limit 1 Time Window**

Power Limit 1 Time Window value in second. The value may vary from 0 to 128. 0 = default value (28 sec for mobile and 8 sec for desktop). Defines time window which TDP value should be maintained.

➔ **EIST [Enable]**

Use the **EIST** option to enable more than two frequency ranges to be supported.

➔ **Disabled**		Disables more than two frequency ranges
➔ **Enabled**	**DEFAULT**	Enables more than two frequency ranges

➔ **C states [Disabled]**

Use the **C states** option to enable or disable the CPU Power Management.

➔ **Disabled**	**DEFAULT**	Disables CPU to go to C states when it's not 100% utilized.
➔ **Enabled**		Enables CPU to go to C states when it's not 100% utilized.

➔ **Active Performance Cores [All]**

Use the **Active Performance Cores** BIOS option to enable numbers of P-cores in the processor package.

➔ **Active Efficient cores [All]**

Use the **Active Efficient Cores** BIOS option to enable numbers of E-cores in the processor package.

5.3.3 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 7**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).

BIOS Menu 7: Trusted Computing

➔ **Security Device Support [Enable]**

Use the **Security Device Support** option to configure support for the TPM.

➔ **Disable**		TPM support is disabled.
➔ **Enable**	**DEFAULT**	TPM support is enabled.

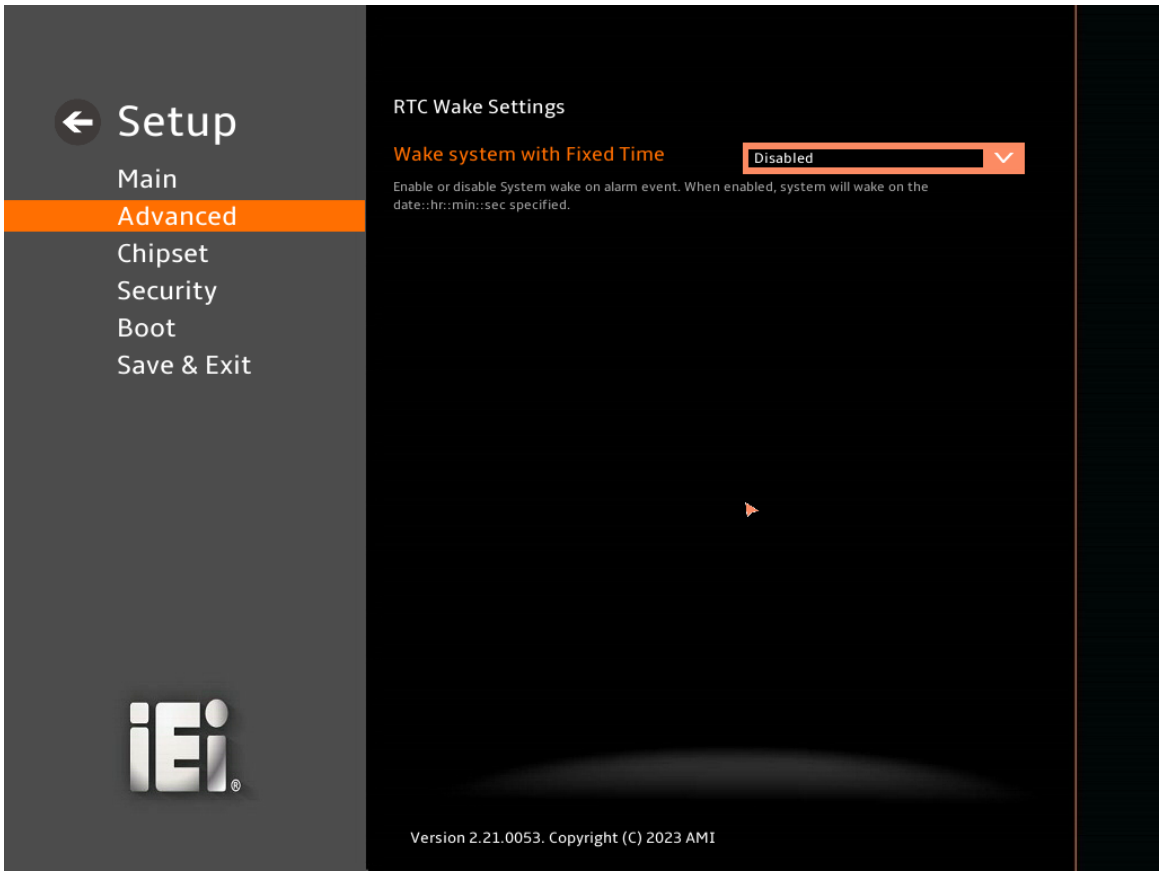
➔ **Pending Operation [None]**

Use the **Pending Operation** option to schedule an operation for the security device.

- ➔ **None** **DEFAULT** TPM information is previous.
- ➔ **TPM Clear** TPM information is cleared.

5.3.4 RTC Wake Settings

Use the RTC Wake Settings menu (**BIOS Menu 8 & BIOS Menu 9**) to enable or disable System wake on alarm event. When enabled, system will wake on the date:hour:minute:second: specified.



BIOS Menu 8:RTC Wake Settings

BIOS Menu 9: Wake system with Fixed Time [Enabled]

➔ **Wake system with Fixed Time [Disabled]**

Use the **RTC Wake Settings** Enable or disable System wake on alarm event.

➔ **Disabled**	**DEFAULT**	RTC Wake Settings support is disabled
➔ **Enabled**		RTC Wake Settings support is enabled

➔ **Wake up every day [Disabled]**

Use the **Wake up every day** to select Enable or disable RTC Wake every day on the hour:minute:second: specified.

➔ **Disabled**	**DEFAULT**	RTC Wake Settings support is disabled
➔ **Enabled**		RTC Wake Settings support is enabled

➔ **Wake up date [1]**

Use the **Wake up date** select 1-31 for which day of the month that you would like the system to wake up.

➔ **Wake up hour [0]**

Use the **Wake up hour** select 0-23 For example enter 3 for 3am and 15 for 3pm.

➔ **Wake up minute [0]**

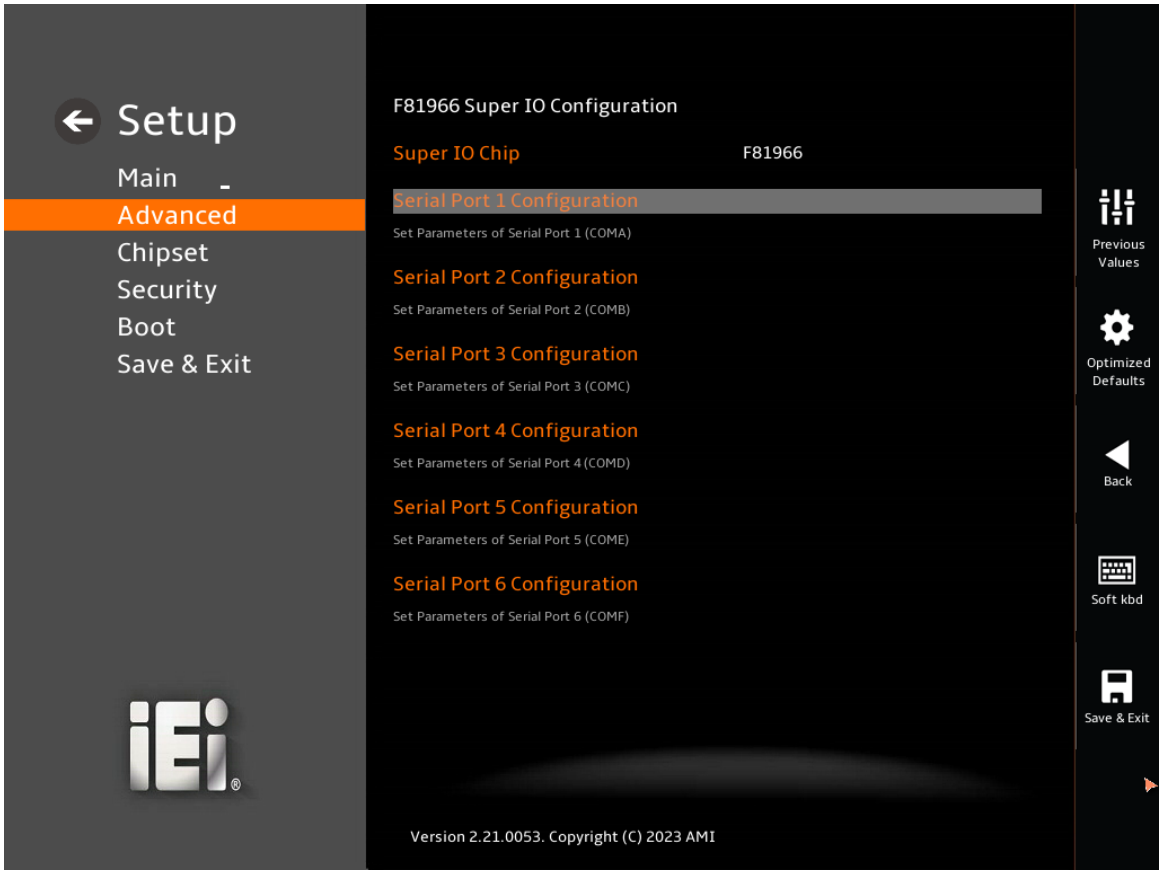
Use the **Wake up minute** select 0-59 for which minute that you would like the system to wake up.

➔ **Wake up second [0]**

Use the **Wake up second** select 0-59 for which second that you would like the system to wake up.

5.3.5 F81966 Super IO Configuration

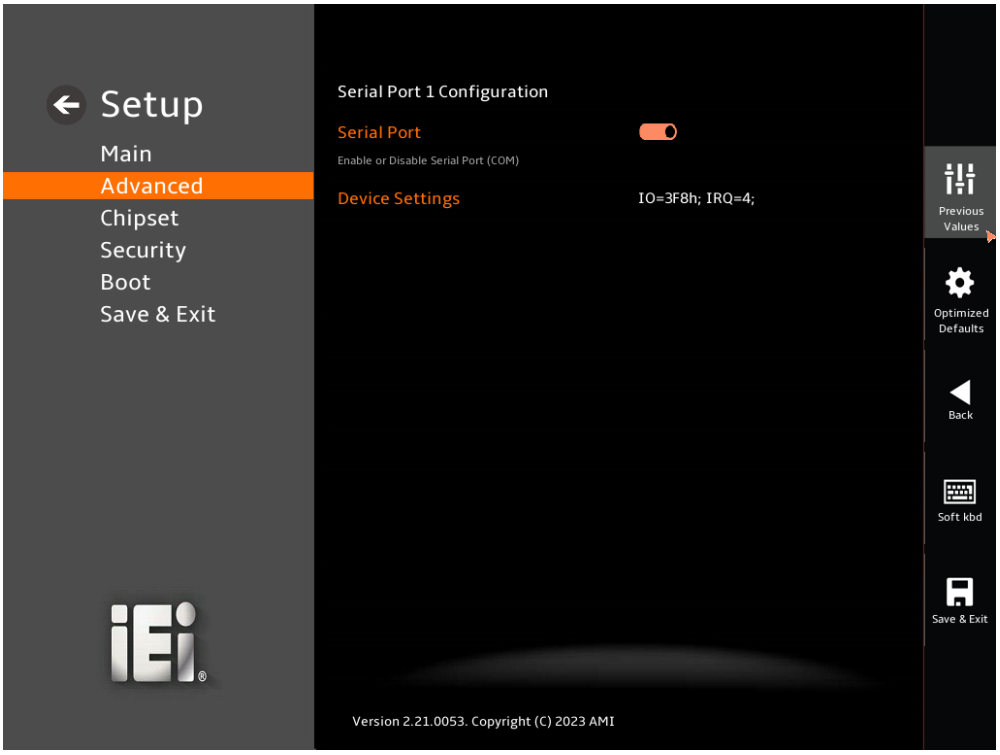
Use the **F81966 Super IO Configuration** menu (**BIOS Menu 10**) to set or change the configurations for the serial ports.



BIOS Menu 10: F81966 Super IO Configuration

5.3.5.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 11**) to configure the serial port.



BIOS Menu 11: Serial Port 1 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

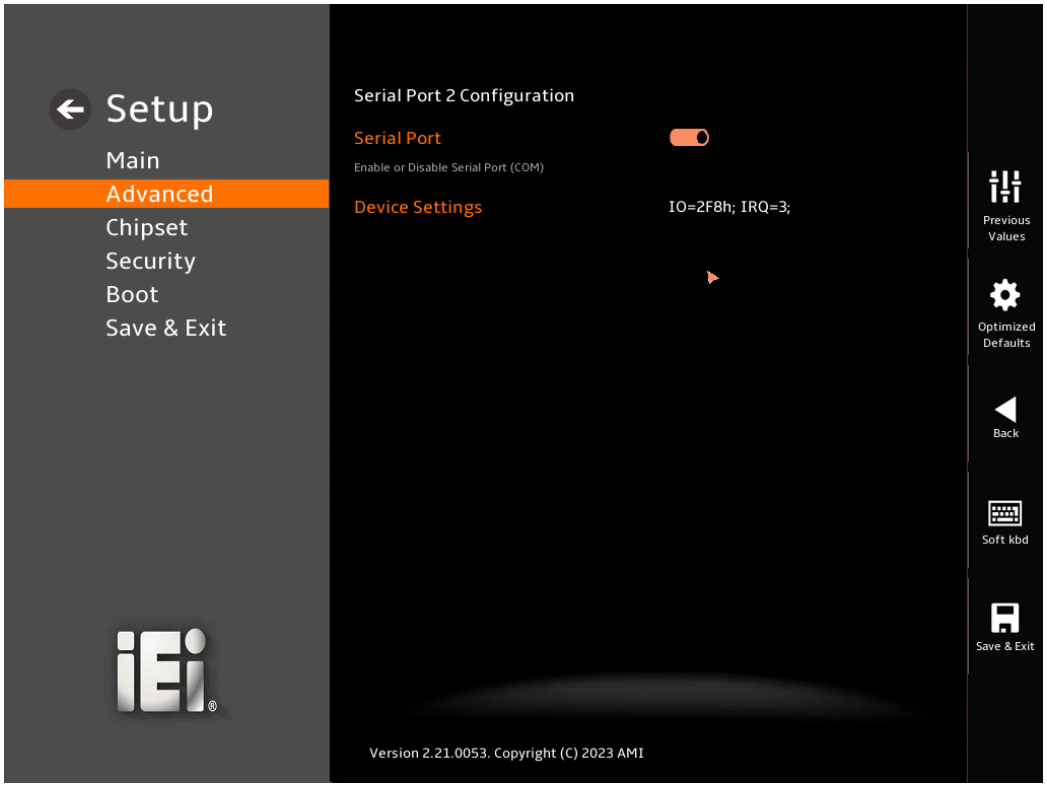
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=3F8h; IRQ=4**	Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

5.3.5.2 Serial Port 2 Configuration

Use the **Serial Port 2 Configuration** menu (**BIOS Menu 12**) to configure the serial port.



BIOS Menu 12: Serial Port 2 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

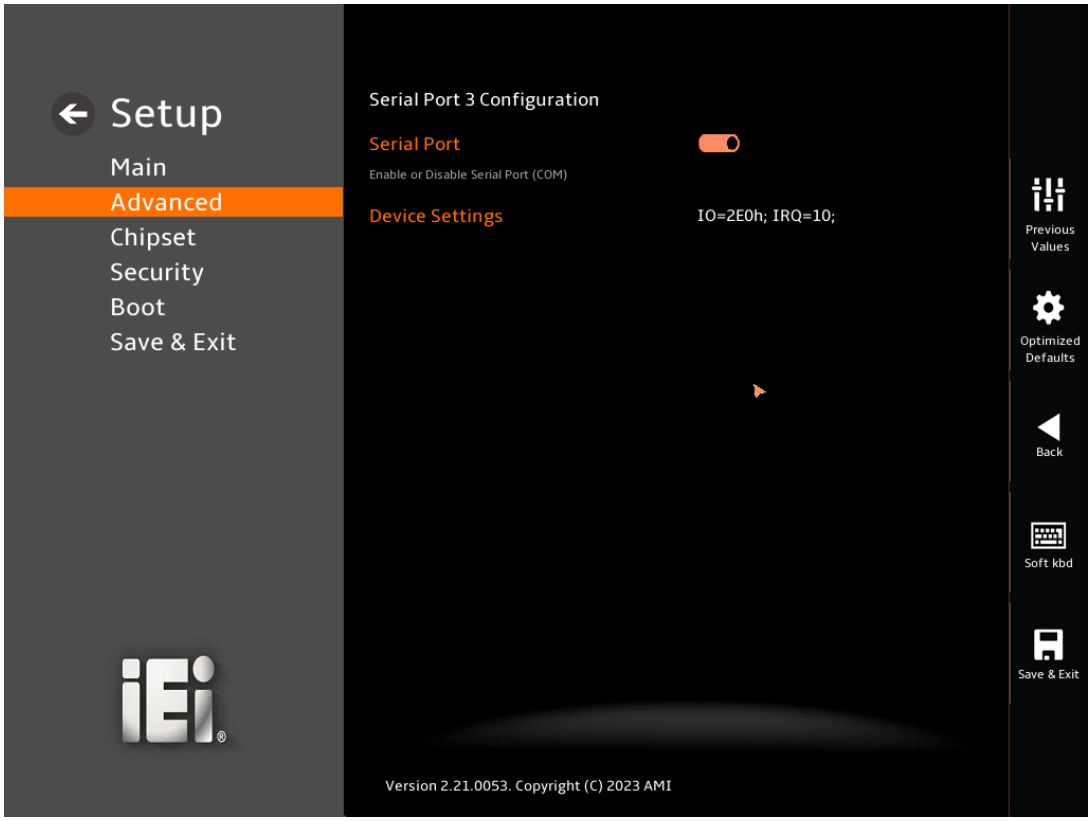
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2F8h; IRQ=3**	Serial Port I/O port address is 2F8h and the interrupt address is IRQ3

5.3.5.3 Serial Port 3 Configuration

Use the **Serial Port 3 Configuration** menu (**BIOS Menu 13**) to configure the serial port.



BIOS Menu 13: Serial Port 3 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

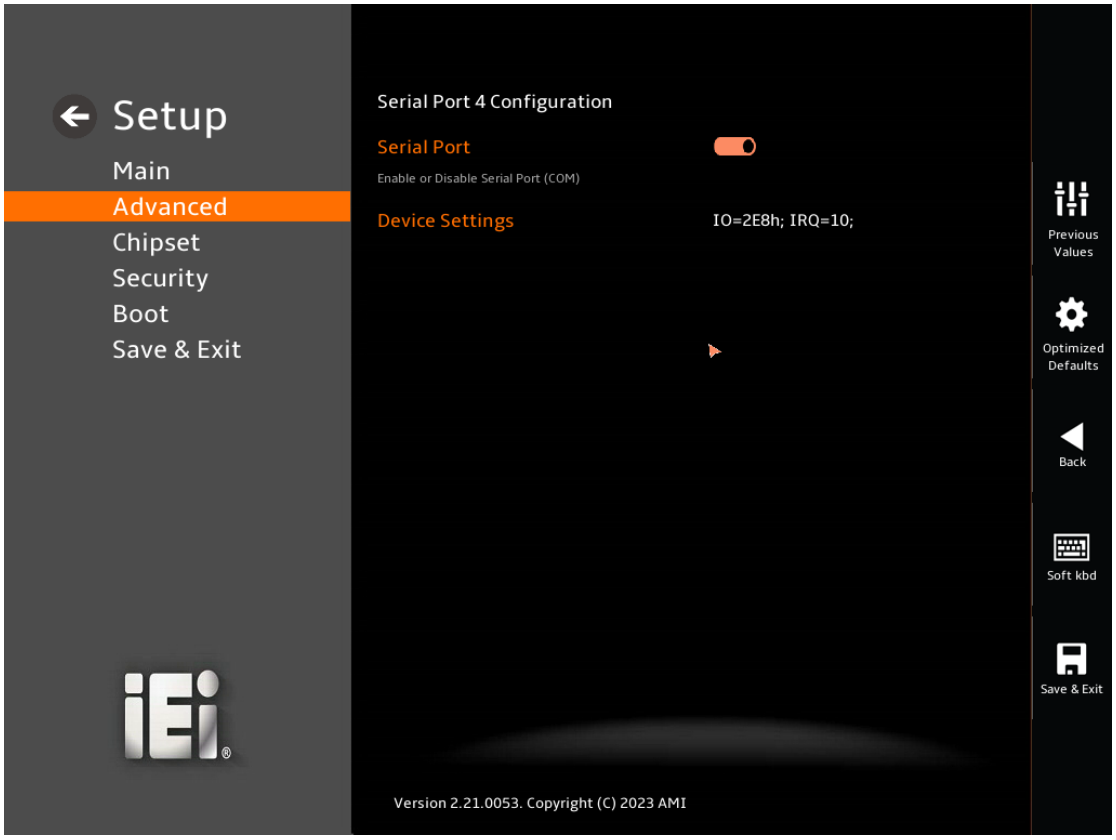
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E0h; IRQ=10**	Serial Port I/O port address is 2E0h and the interrupt address is IRQ10

5.3.5.4 Serial Port 4 Configuration

Use the **Serial Port 4 Configuration** menu (**BIOS Menu 14**) to configure the serial port.



BIOS Menu 14: Serial Port 4 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2E8h; IRQ=10**	Serial Port I/O port address is 2E8h and the interrupt address is IRQ10

5.3.5.5 Serial Port 5 Configuration

Use the **Serial Port 5 Configuration** menu (**BIOS Menu 15**) to configure the serial port.

BIOS Menu 15: Serial Port 5 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2C0h; IRQ=10** — Serial Port I/O port address is 2C0h and the interrupt address is IRQ10

➔ **Device Mode**

Use the **Device Mode** option to change the serial port mode.

➔ **RS232** — The serial port mode is RS-232

RS422 with Register — The serial port mode is RS-422

RS485 with Register — The serial port mode is RS-485

5.3.5.6 Serial Port 6 Configuration

Use the **Serial Port 6 Configuration** menu (**BIOS Menu 16**) to configure the serial port.

BIOS Menu 16: Serial Port 6 Configuration Menu

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=2C8h; IRQ=10**	Serial Port I/O port address is 2C8h and the interrupt address is IRQ10

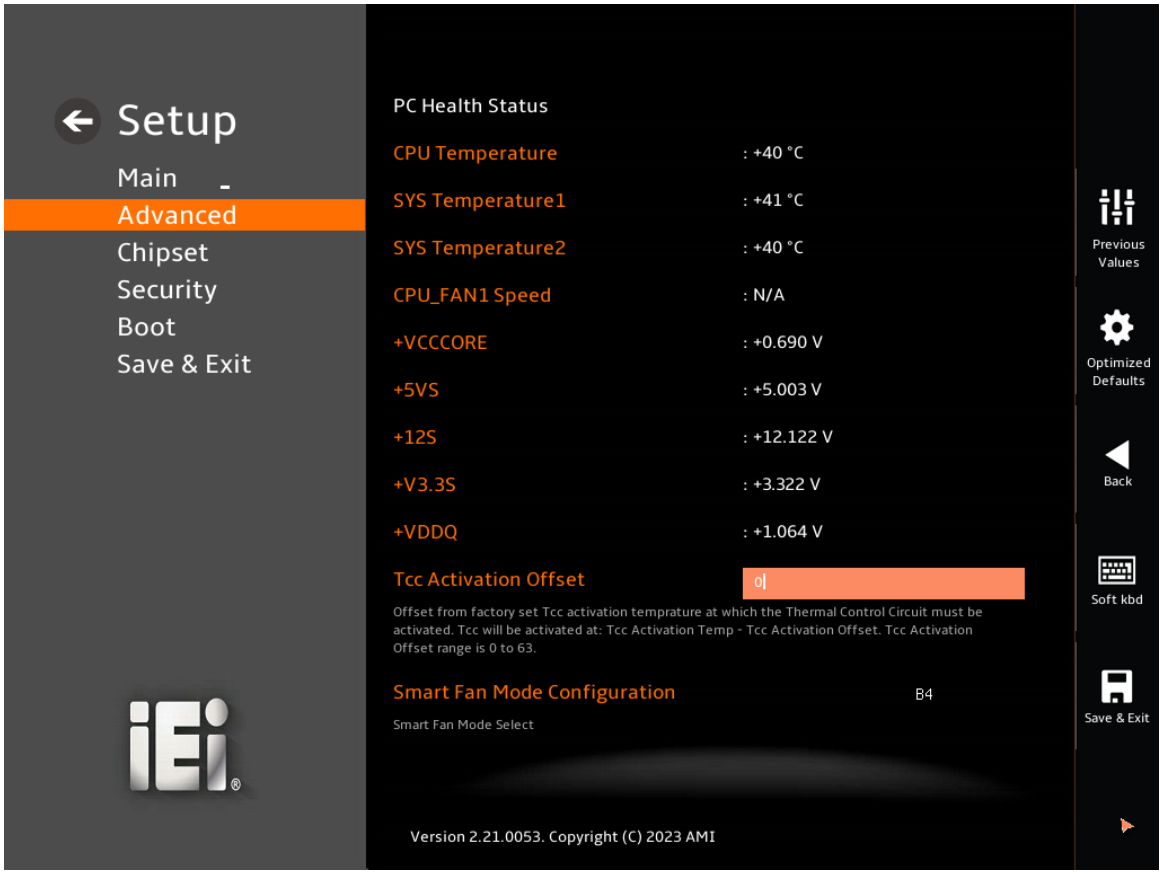
➔ **Device Mode**

Use the **Device** Mode option to change the serial port mode.

➔ **RS232**	The serial port mode is RS-232
RS422 with Register	The serial port mode is RS-422
RS485 with Register	The serial port mode is RS-485

5.3.6 EC KB9068 H/W Monitor

The EC KB9068 H/W Monitor menu (**BIOS Menu 17**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 17: EC KB9068 H/W Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - System Temperature1
  - System Temperature2

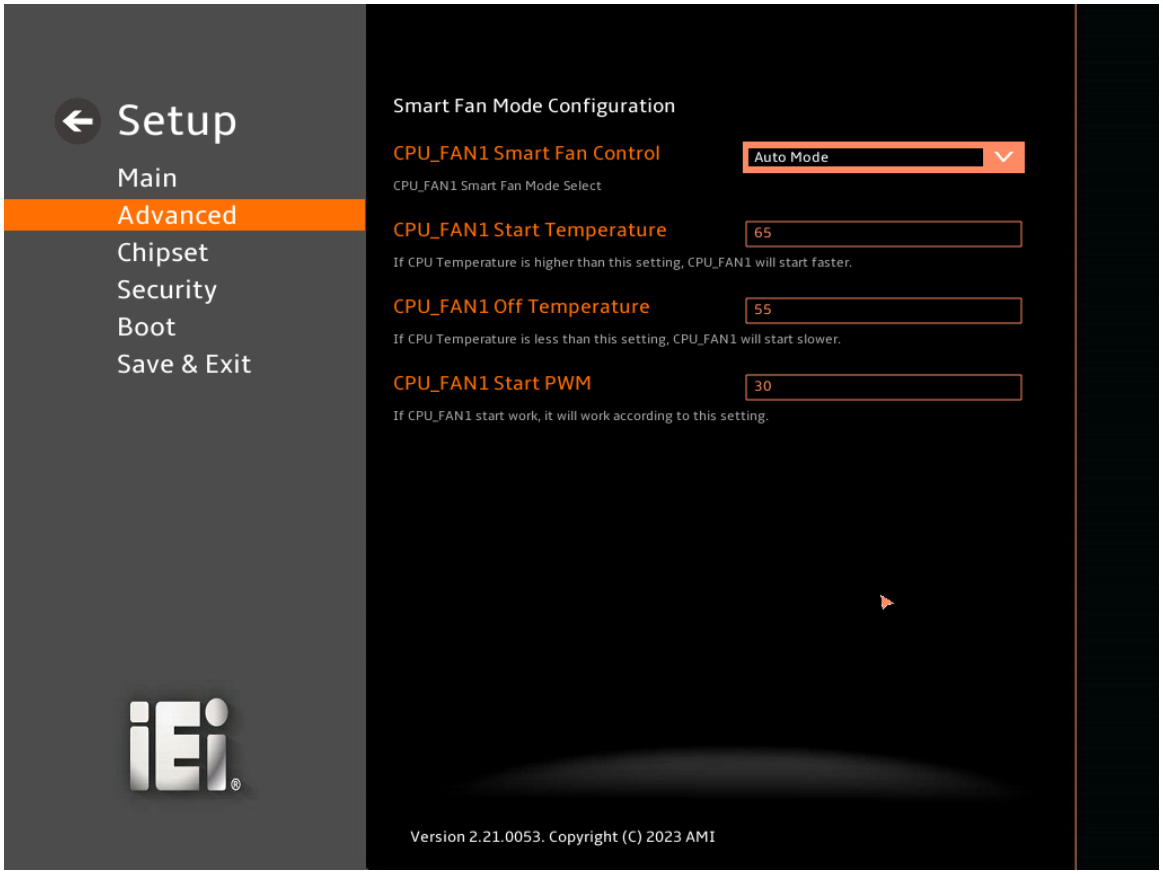
- Fan Speeds:
  - CPU_Fan1 Speed
- Voltages:
  - VCCCORE
  - +5VS
  - +12S
  - +V3.3S
  - +VDDQ

➔ **Tcc Activation Offset**

Offset from factoryset Tcc activation temprature at which the Thermal Control Circuit must be activated. Tcc will be activated at: Tcc Activation Temp-Tcc Activation Offset.Tcc Activation Offset range is 0 to 63.

5.3.6.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 18**) to configure the CPU/system fan start/off temperature and control mode.



BIOS Menu 18: Smart Fan Mode Configuration

➔ **Smart Fan Control [Auto Mode]**

Use the **Smart Fan Control** option to configure the CPU Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

➔ **CPU_FAN1 Start Temperature**

If the CPU temperature is between **fan off** and **fan start**, the fan speed change to **fan start PWM**. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **CPU_FAN1 Off Temperature**

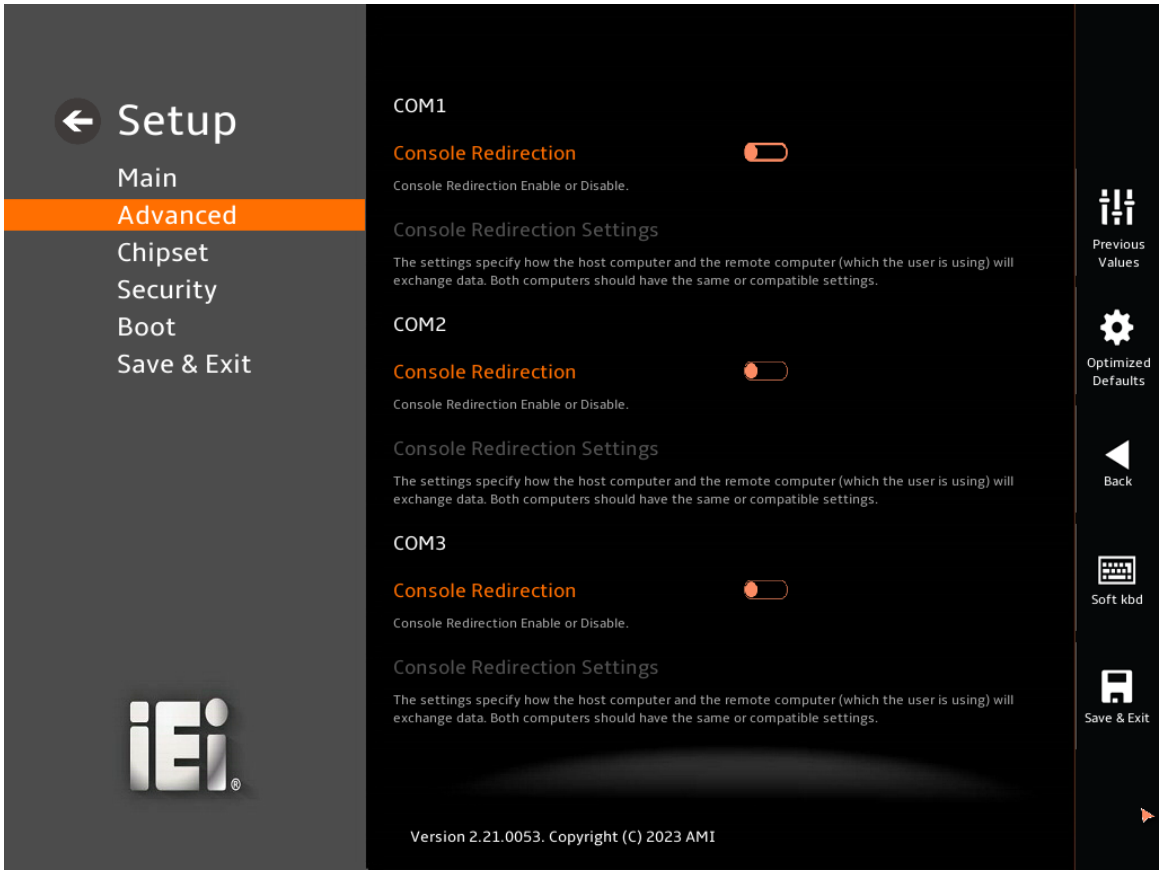
If the CPU temperature is lower than the value set this option, the fan speed change to be lowest. To set a value, Use the + or – key to change the value or enter a decimal number between 1 and 100.

➔ **CPU_FAN1 Start PWM**

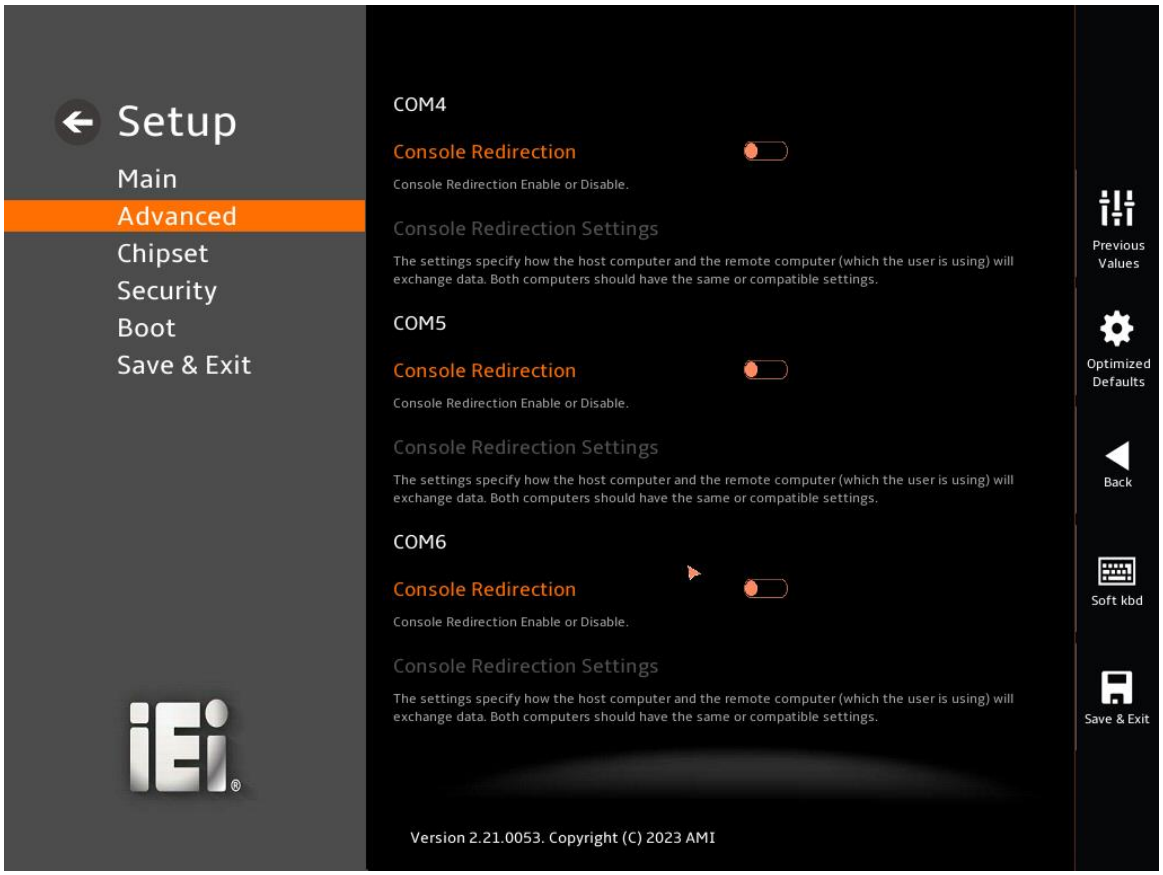
Use the **CPU_FAN1 Start PWM** option to set the PWM start value. Use the + or – key to change the value or enter a decimal number between 1 and 100.

5.3.7 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 19** & **BIOS Menu 20**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 19:Serial Port Console Redirection (1/2)



BIOS Menu 20: Serial Port Console Redirection (2/2)

➔ **Console Redirection [Disabled]**

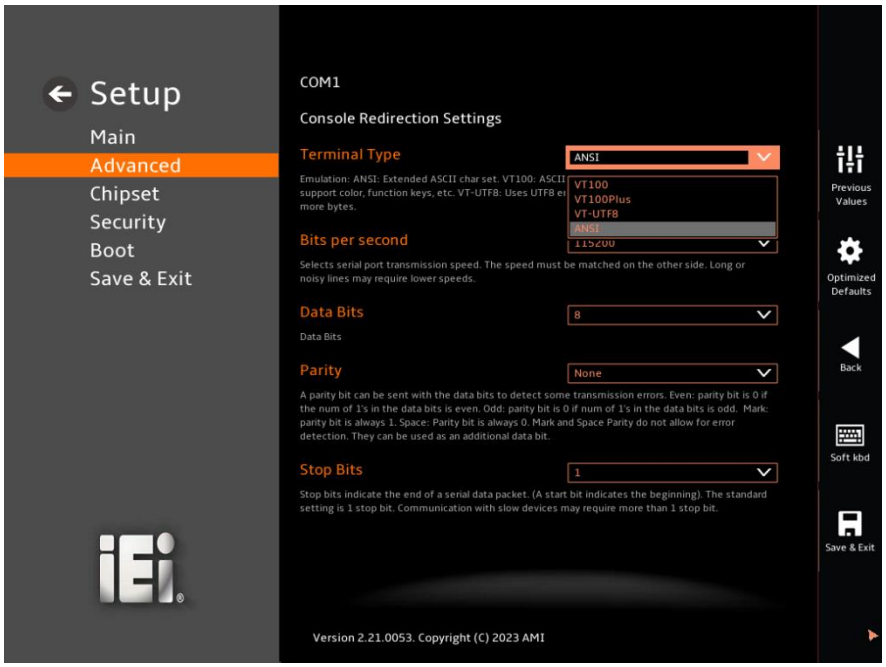
Use **Console Redirection** option to enable or disable the console redirection function.

➔ **Disabled**	**DEFAULT**	Disabled the console redirection function
➔ **Enabled**		Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.7.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 21**) when the **COM Console Redirection** (for COM1 to COM6) option is enabled.



BIOS Menu 21: COM Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100**		The target terminal type is VT100
➔ **VT100Plus**		The target terminal type is VT100Plus
➔ **VT-UTF8**		The target terminal type is VT-UTF8
➔ **ANSI**	**DEFAULT**	The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

- **9600** — Sets the serial port transmission speed at 9600.
- **19200** — Sets the serial port transmission speed at 19200.
- **57600** — Sets the serial port transmission speed at 57600.
- **115200** **DEFAULT** — Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

- **7** — Sets the data bits at 7.
- **8** **DEFAULT** — Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- **None** **DEFAULT** — No parity bit is sent with the data bits.
- **Even** — The parity bit is 0 if the number of ones in the data bits is even.
- **Odd** — The parity bit is 0 if the number of ones in the data bits is odd.
- **Mark** — The parity bit is always 1. This option does not allow for error detection.
- **Space** — The parity bit is always 0. T This option does not allow for error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- **1** **DEFAULT** — Sets the number of stop bits at 1.
- **2** — Sets the number of stop bits at 2.

5.3.8 NVMe Configuration

Use the **NVMe Configuration** (**BIOS Menu 22**) menu to display the NVMe controller and device information.

BIOS Menu 22: NVMe Configuration

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 23**) to access the PCH IO and System Agent (SA) configuration menus.

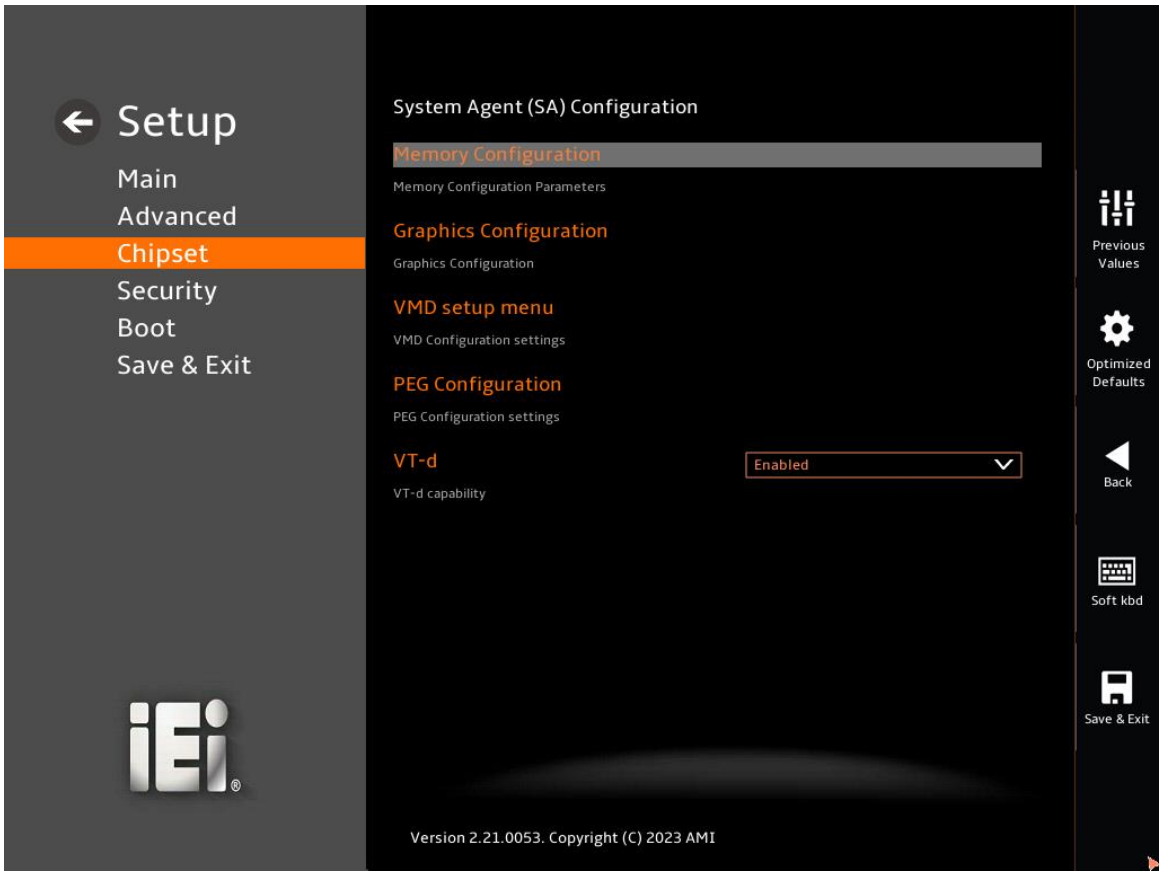
WARNING!

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

BIOS Menu 23: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 24**) to configure the System Agent (SA) parameters.



BIOS Menu 24: System Agent (SA) Configuration

➔ **VT-d [Enabled]**

Use the **VT-d** option to enable or disable the VT-d capability.

➔ **Disabled**		Disable the VT-d capability
➔ **Enabled**	**DEFAULT**	Enable the VT-d capability

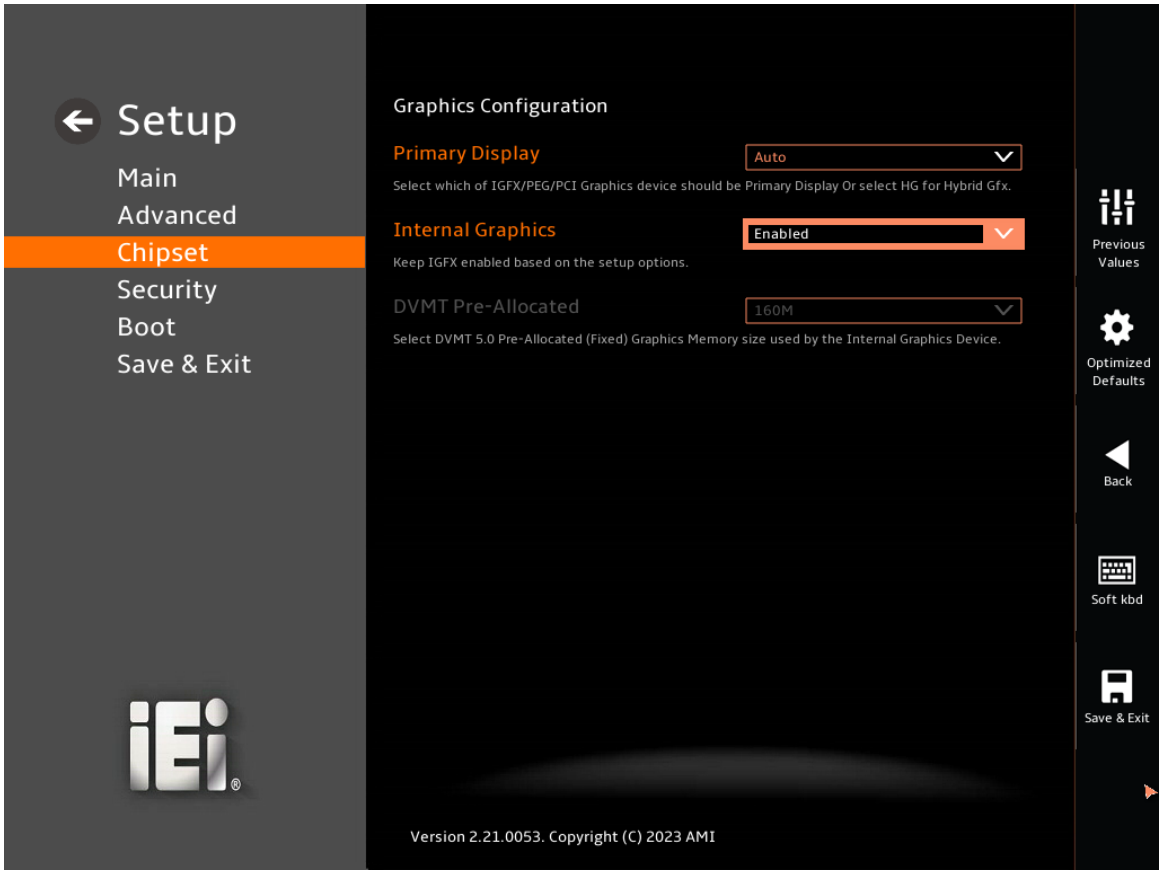
5.4.1.1 Memory Configuration

Use the **Memory Configuration** submenu (**BIOS Menu 25**) to view memory information.

BIOS Menu 25: Memory Configuration

5.4.1.2 Graphics Configuration

Use the **Graphics Configuration** (**BIOS Menu 26**) menu to configure the video device connected to the system.



BIOS Menu 26: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the primary graphics controller the system uses. The following options are available:

- Auto **Default**
- IGFX
- PEG Slot
- PCH PCI
- HG

➔ **Internal Graphics [Enabled]**

Use the **Internal Graphics** option to configure whether to keep IGFX enabled. If user wants to support dual display by internal graphics and external graphics, this Internal Graphics option should be set to Enabled and the above Primary Display option should be set to IGFX.

➔ **Auto**		Auto mode
➔ **Disabled**		Disables IGFX.
➔ **Enabled**	**Default**	Enables IGFX.

➔ **DVMT Pre-Allocated [160M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 80M
- 160M **Default**

5.4.1.3 VMD setup menu

Use the **VMD setup menu** (**BIOS Menu 27**) menu to configure the video device connected to the system.

BIOS Menu 27: VMD setup menu

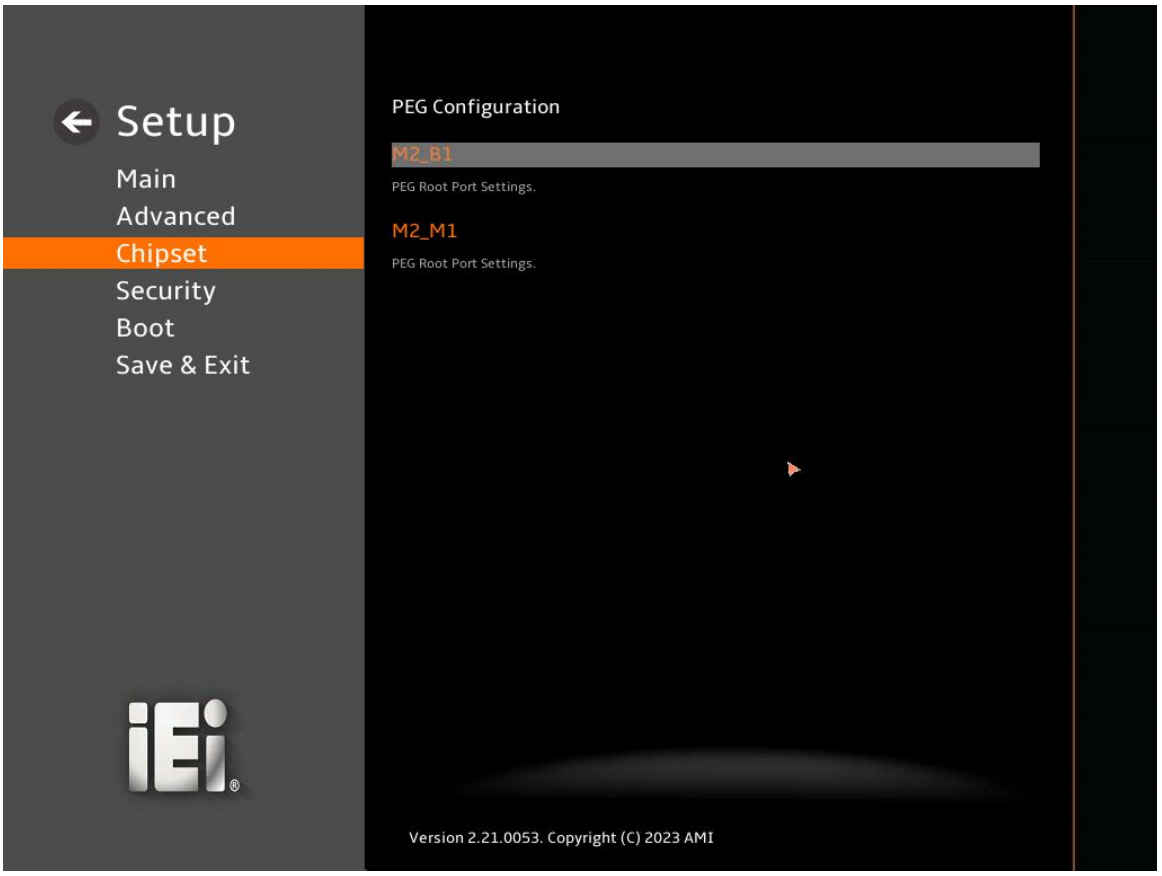
➔ **Enable VMD controller**

Use the **VMD controller** to select Enable/Disable

➔ **Disabled**	**DEFAULT**	Disable to VMD controller
➔ **Enable**		Enable to VMD controller

5.4.1.4 PEG Configuration

Use the **PEG Configuration** (**BIOS Menu 28**) menu to configure the M2_B1 slot and the M2_M1 slot.



BIOS Menu 28:PEG Configuration

5.4.1.4.1 M2_B1 Slot

Use the **M2_B1** menu **(BIOS Menu 29**) to change and/or set the configuration of the M2_B1 devices installed in the system.

BIOS Menu 29: M2_B1

➔ **M2_B1 [Enabled]**

Use the **M2_B1** to Control the PEG Root Port.

➔ **Disabled**		Disable the M2_B1
➔ **Enabled**	**DEFAULT**	Enable the M2_B1

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.
➔ **Gen4**		Configure PCIe Speed to Gen4.

➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.1.4.2 M2_M1 Slot

Use the **M2_M1** menu (**BIOS Menu 30**) to change and/or set the configuration of the M2_M1 devices installed in the system.

BIOS Menu 30: M2_M1

➔ **M2_M1 [Enabled]**

Use the **M2_M1** to Control the PEG Root Port.

➔ **Disabled**		Disable the M2_M1
➔ **Enabled**	**DEFAULT**	Enable the M2_M1

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.
➔ **Gen4**		Configure PCIe Speed to Gen4.
➔ **Gen5**		Configure PCIe Speed to Gen5.

➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 31** & **BIOS Menu 32**) to configure the PCH parameters.

BIOS Menu 31:PCH-IO Configuration (1/2)

BIOS Menu 32:PCH-IO Configuration (2/2)

➔ **Auto Power Button Function [Disabled (ATX)]**

Use the **Auto Power Button Function** BIOS option to show the power mode state. Use the **J_ATX_AT1** to switch the AT/ATX power mode.

➔ **Disabled (ATX)**	**DEFAULT**	The system power mode is ATX.
➔ **Enabled (AT)**		The system power mode is AT.

➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system when the power mode is ATX.

➔ **Power Off**	The system remains turned off

- ➔ **Power On** The system turns on
- ➔ **Last State** **DEFAULT** The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **Power Saving Function (EUP) [Disabled]**

Use the **Power Saving Function (EUP)** BIOS option to enable or disable the power saving function.

- ➔ **Disabled** **DEFAULT** Power saving function is disabled.
- ➔ **Enabled** Power saving function is enabled. It will reduce power consumption when the system is off.

➔ **USB Power SW1 (USB3_1) [+5V DUAL]**

Use the **USB Power SW1 (USB3_1)** BIOS option to configure the USB power source for the corresponding USB connectors (Figure 5-2).

- ➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual
- ➔ **+5V** Sets the USB power source to +5V

➔ **USB Power SW2 (USB3_2) [+5V DUAL]**

Use the **USB Power SW2 (USB3_2)** BIOS option to configure the USB power source for the corresponding USB connectors (Figure 5-2).

- ➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual
- ➔ **+5V** Sets the USB power source to +5V

➔ **USB Power SW3 (USB2_1) [+5V DUAL]**

Use the **USB Power SW3 (USB2_1)** BIOS option to configure the USB power source for the corresponding USB connectors (**Figure 5-2).**

- ➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual
- ➔ **+5V** Sets the USB power source to +5V

➔ **USB Power SW4 (USB2_2) [+5V DUAL]**

Use the **USB Power SW4 (USB2_2)** BIOS option to configure the USB power source for the corresponding USB connectors (**Figure 5-2**).

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

➔ **+5V** Sets the USB power source to +5V

BIOS Options	Configured USB Ports
USB Power SW1	USB3_1 (external USB 3.2 Gen 2 ports)
USB Power SW2	USB3_2 (external USB 3.2 Gen 2 ports)
USB Power SW3	USB2_1 (internal USB 2.0 ports)
USB Power SW4	USB2_2 (internal USB 2.0 ports)

Figure 5-2: BIOS Options and Configured USB Ports

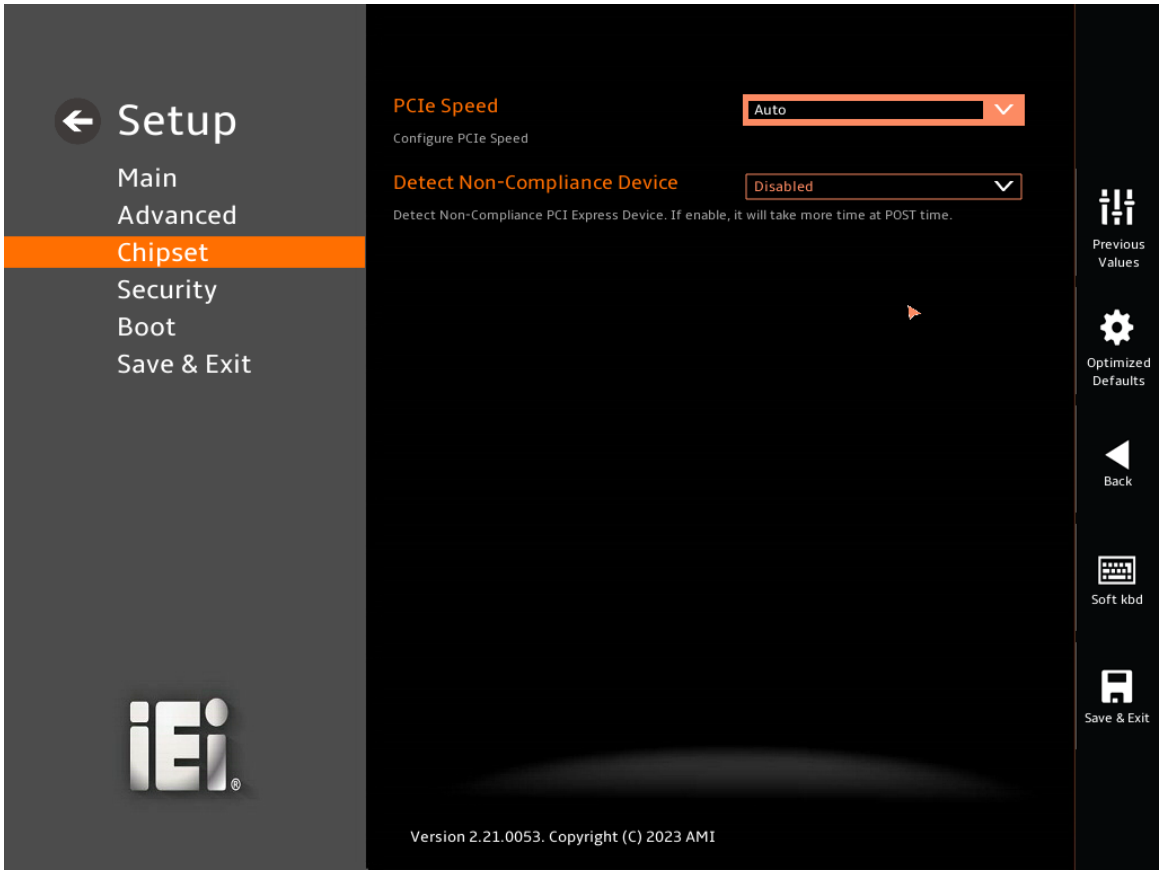
5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 33**) to configure the PCI Express slots.

BIOS Menu 33: PCI Express Configuration

5.4.2.1.1 PCIe Root Port Setting

Use the **PCIEX4_1_1, M2_A1 Slot** submenu (**BIOS Menu 34**) to configure the PCI Root Port Setting.



BIOS Menu 34: PCIe Slot Configuration Submenu

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.

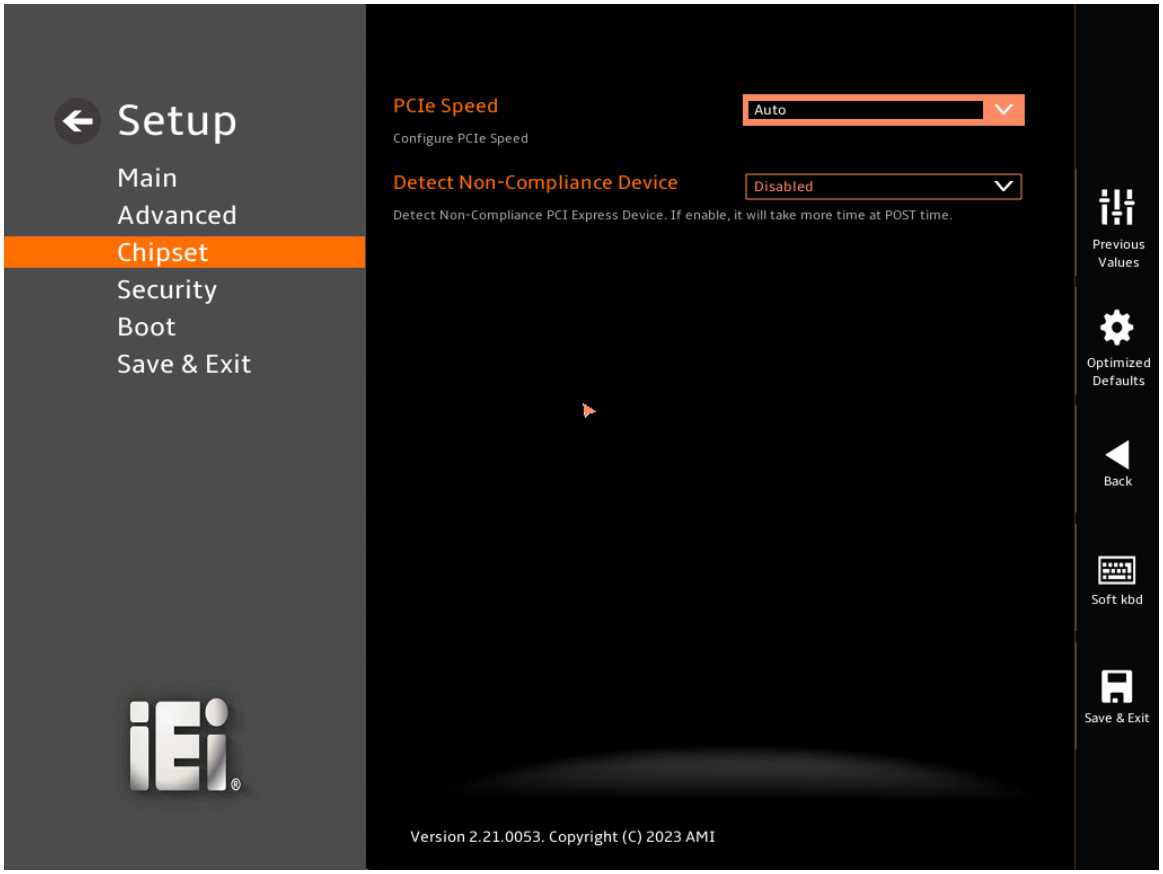
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.1.2 M2_A1 Slot

Use the **M2_A1** menu (**BIOS Menu 35**) to change and/or set the configuration of the M.2 devices installed in the system.



BIOS Menu 35: M2_A1

➔ **PCIe Speed [Auto]**

Use the **PCIe Speed** option to specify the PCI Express port speed. Configuration options are listed below.

➔ **Auto**	**DEFAULT**	Auto mode.
➔ **Gen1**		Configure PCIe Speed to Gen1.
➔ **Gen2**		Configure PCIe Speed to Gen2.
➔ **Gen3**		Configure PCIe Speed to Gen3.

➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to configure whether to detect if a non-compliance PCI Express device is connected to the PCI Express port.

➔ **Disabled**	**DEFAULT**	Do not detect if a non-compliance PCI Express device is connected to the PCI Express port.
➔ **Enabled**		Detect if a non-compliance PCI Express device is connected to the PCI Express port.

5.4.2.2 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 36**) to change and/or set the configuration of the SATA devices installed in the system.

BIOS Menu 36: SATA Configuration

➔ **SATA Controller(s) [Enabled]**

Use the **SATA Controller(s)** option to configure the SATA controller(s).

➔ **Enabled**	**DEFAULT**	Enables the on-board SATA controller(s).
➔ **Disabled**		Disables the on-board SATA controller(s).

➔ **SATA Mode Selection [AHCI]**

Use the **SATA Mode Selection** option to determine how the SATA devices operate.

➔ **AHCI** **DEFAULT** Configures SATA devices as AHCI device.

➔ **Hot Plug [Disabled]**

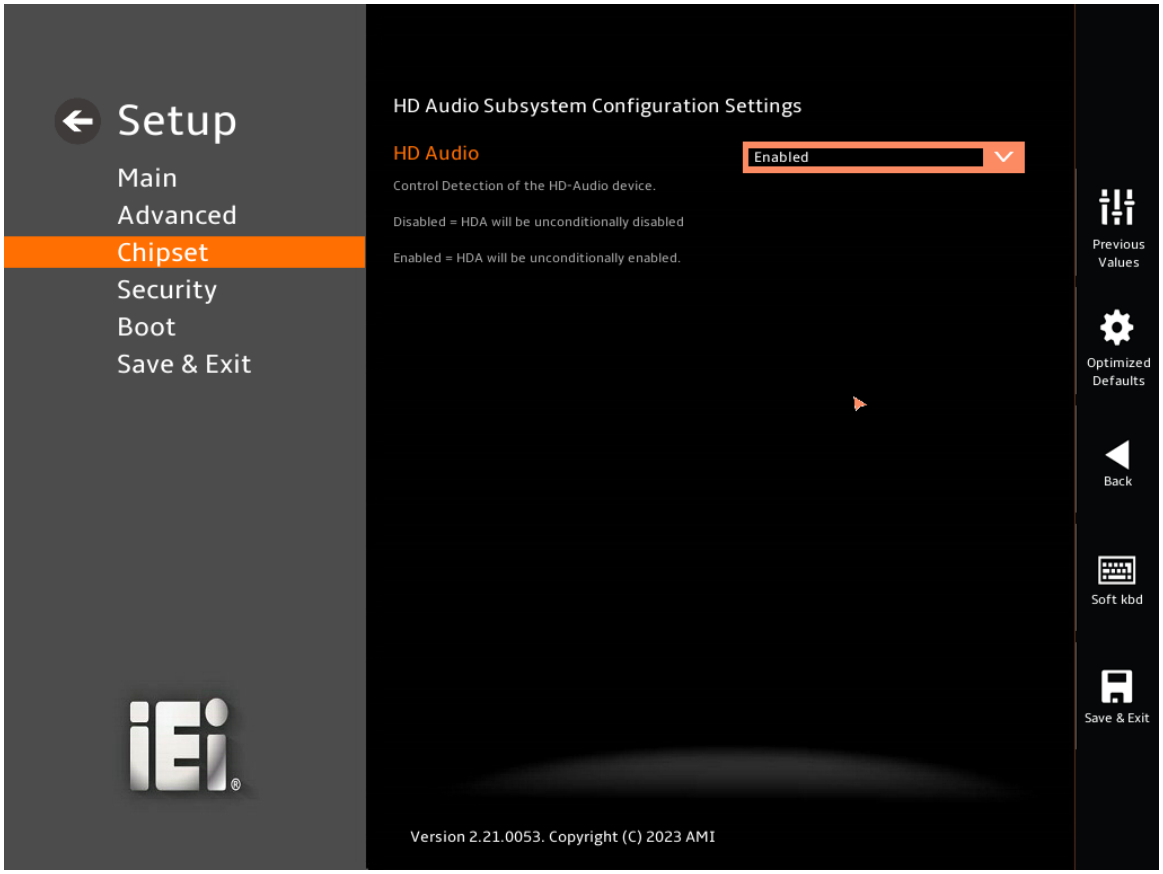
Use the **Hot Plug** option (for S_ATA1 and M2_M1) to designate the correspondent port as hot-pluggable.

➔ **Disabled** **DEFAULT** Disables the hot-pluggable function of the SATA port.

➔ **Enabled** Designates the SATA port as hot-pluggable.

5.4.2.3 HD Audio Configuration

Use the **HD Audio Configuration** menu (**BIOS Menu 37**) to configure the PCH Azalia settings.



BIOS Menu 37: HD Audio Configuration

➔ **HD Audio [Enabled]**

Use the **HD Audio** option to enable or disable the High Definition Audio controller.

➔ **Disabled**		The onboard High Definition Audio controller is disabled.
➔ **Enabled**	**DEFAULT**	The onboard High Definition Audio controller is enabled.

5.5 Security

Use the **Security** menu (**BIOS Menu 38**) to set system and user passwords.

BIOS Menu 38: Security

➔ Administrator Password

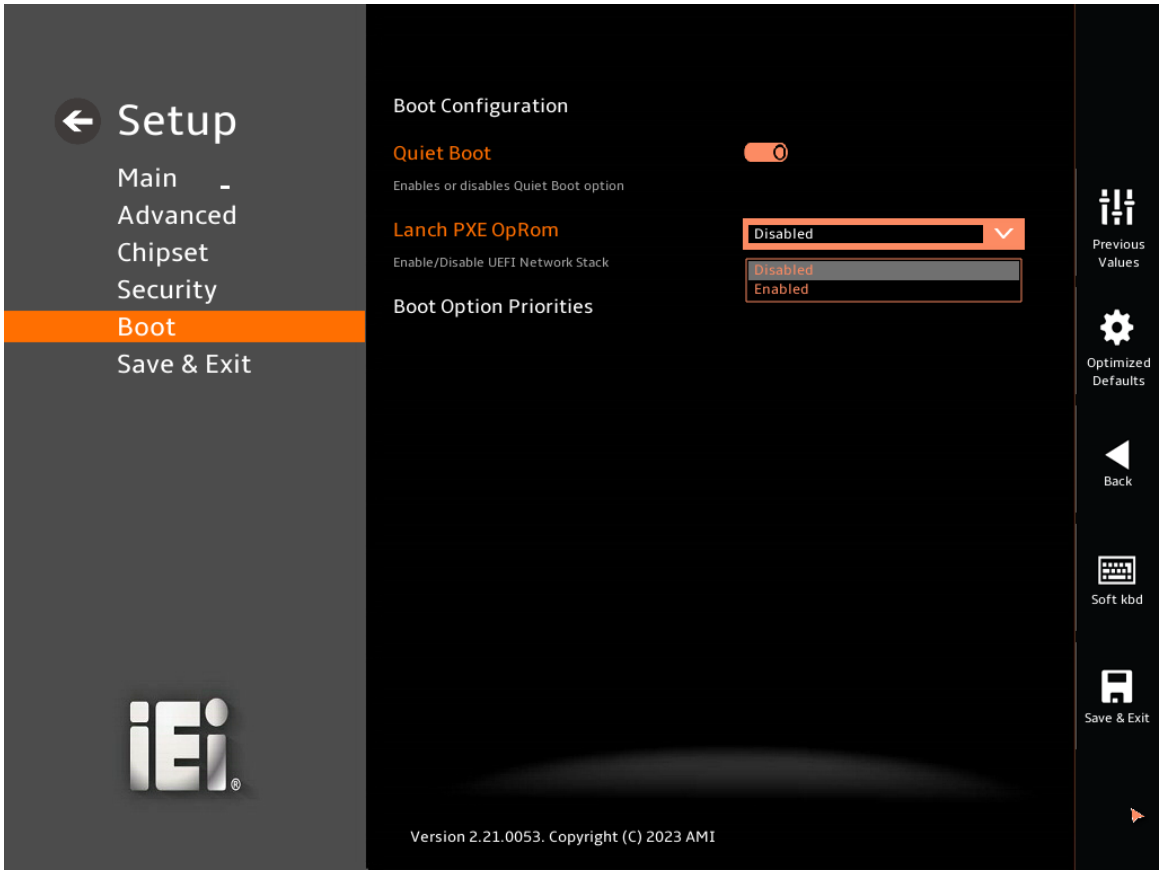
Use the **Administrator Password** to set or change a administrator password.

➔ User Password

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 39**) to configure system boot options.



BIOS Menu 39: Boot

5.6.1 Boot Configuration

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled**		Normal POST messages displayed
➔ **Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

5.6.2 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected, The following Boot Options are listed as an example.

➔ **Boot Option #1**

Sets the system boot order **ADATA SP580** as the first priority.

➔ **Windows Boot Manager (P1: ADATA SSD SP580 240GB)**

➔ **Disabled**

➔ **Boot Option #2**

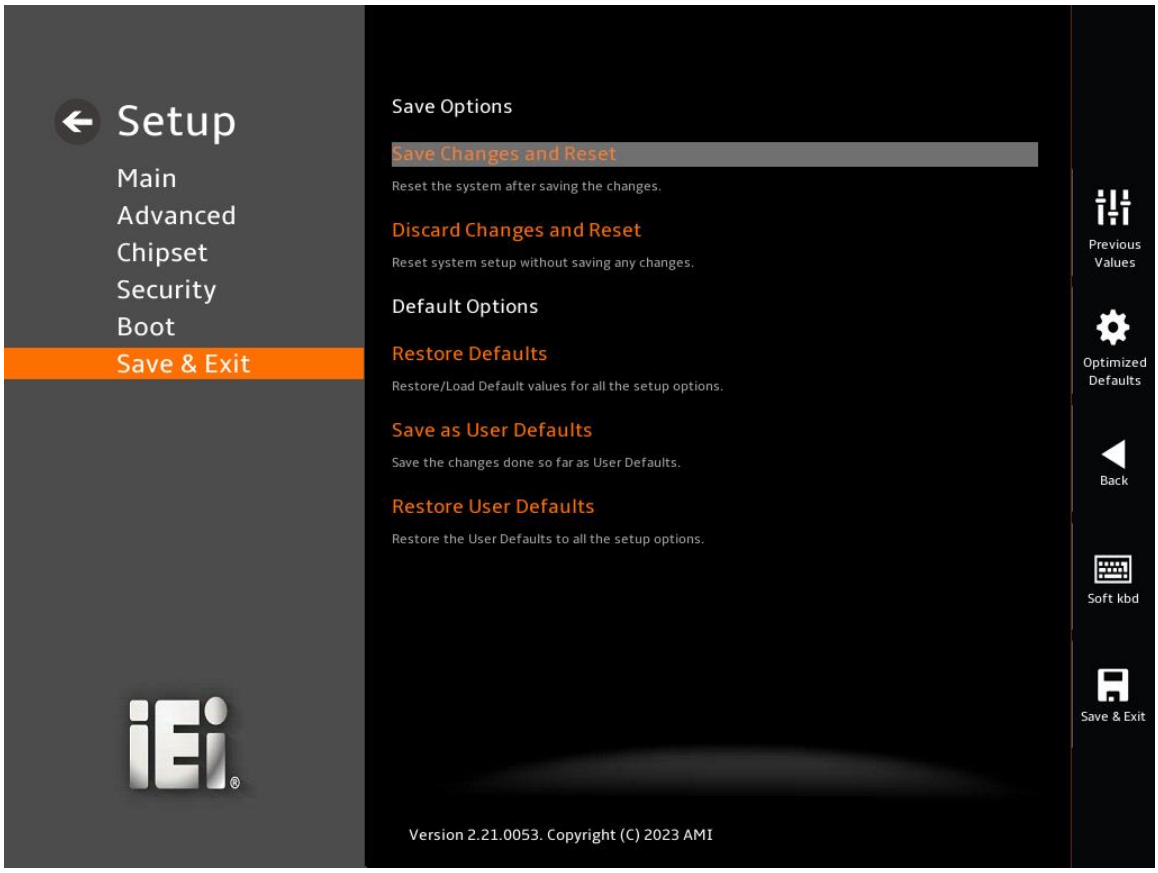
Sets the system boot order **USB Partition 1** as the second priority.

➔ **UEFI: USB, Partition 1**

➔ **Disabled**

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 40**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 40: Save & Exit

➔ Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

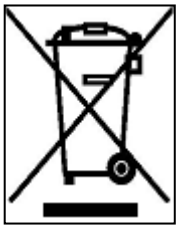
Product Disposal

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

E

Error Beep Code

E.1 PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

NOTE:

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybromina ted Biphenyls	Polybromina ted Diphenyl Ethers	Bis(2-ethylhexyl) phthalate	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。