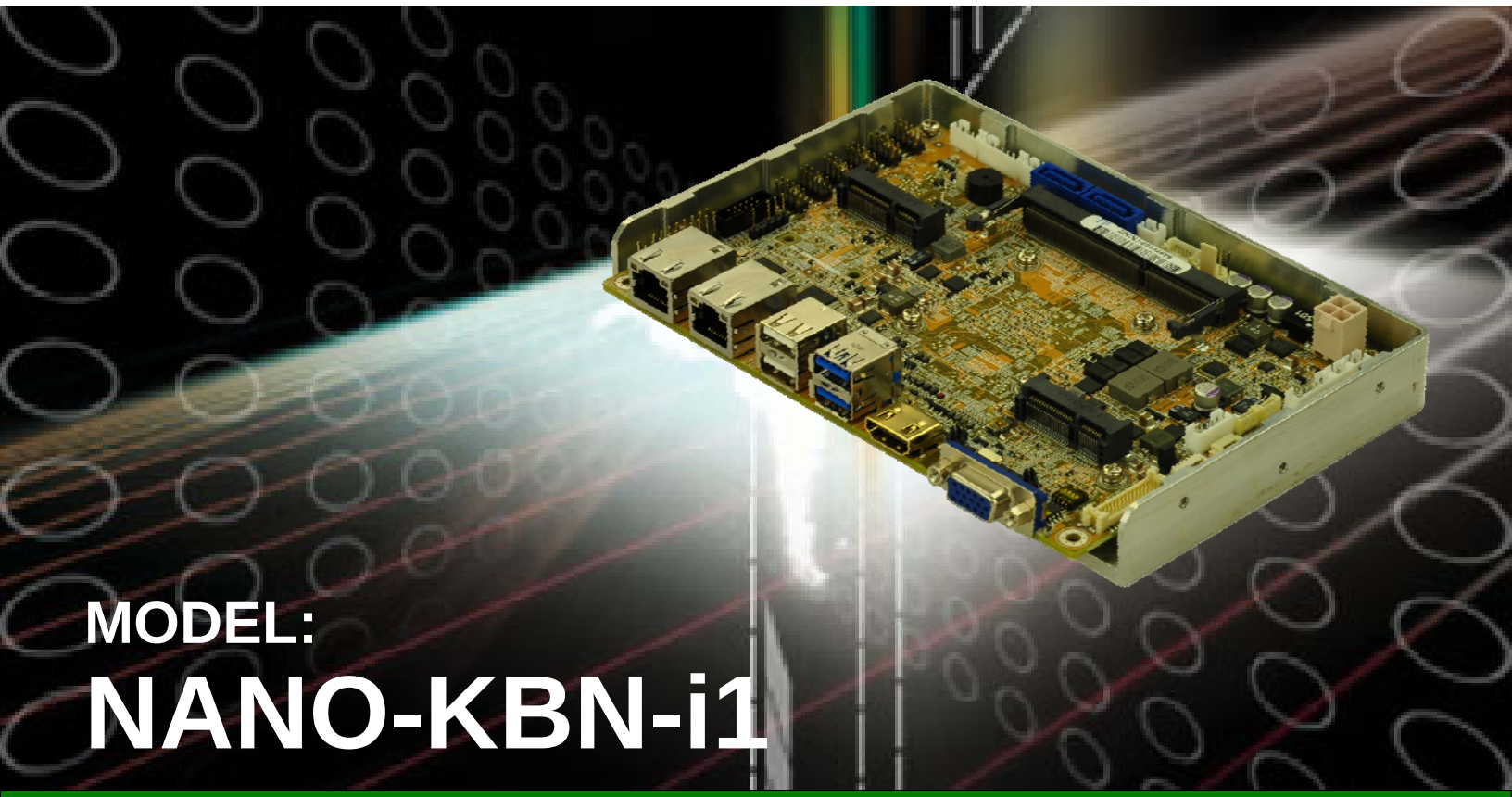
IEI Integration Corp.



MODEL:

NANO-KBN-i1

EPIC SBC supports AMD® Embedded G-Series SoC with VGA/HDMI/LVDS, Dual PCIe GbE, USB 3.0, PCIe Mini, SATA 6Gb/s, mSATA, COM, iRIS-1010, HD Audio and RoHS

User Manual

Rev. 1.02 - August 27, 2015

RoHS Lead Free

Revision

Date	Version	Changes
August 27, 2015	1.02	Updated Figure 1-3: Dimensions (mm) Added Section 4.5: Chassis Installation
September 17, 2014	1.01	Added I^2C connector
March 11, 2014	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

HOT SURFACE

This symbol indicates a hot surface that should not be touched without taking care.

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Chapter

1

Introduction

1.1 Introduction

Figure 1-1: NANO-KBN-i1

The NANO-KBN-i1 EPIC SBC motherboard is an AMD® G-Series SoC processor platform. It supports one 204-pin 1600/1333 MHz DDR3 SO-DIMM up to 8.0 GB.

The NANO-KBN-i1 supports dual display via VGA, HDMI and an internal LVDS connector. Expansion and I/O include two USB 3.0 connectors on the rear panel, four USB 2.0 connectors by pin header, two USB 2.0 connectors on the rear panel and two SATA 6Gb/s connectors. Serial device connectivity is provided by five internal RS-232 connectors and one internal RS-422/485 connector. Two RJ-45 Ethernet connectors provide the system with smooth connections to an external LAN.

1.2 Model Variations

The model variations of the NANO-KBN-i1 Series are listed below.

Model No.	SoC
NANO-KBN-i1-4201-R10	AMD® G-Series GX-420CA, 25W, 2.0GHz
NANO-KBN-i1-4151-R10	AMD® G-Series GX-415GA, 15W, 1.5GHz
NANO-KBN-i1-2171-R10	AMD® G-Series GX-217GA, 15W, 1.65GHz
NANO-KBN-i1-2101-R10	AMD® G-Series GX-210HA, 9W, 1.0GHz

Table 1-1: NANO-KBN-i1 Model Variations

1.3 Features

Some of the NANO-KBN-i1 motherboard features are listed below:

- EPIC SBC supports AMD® embedded G-Series SoC
- Dual independent display support
- One 204-pin 1600/1333 MHz dual-channel DDR3 & DDR3L SDRAM unbuffered SO-DIMM support up to 8GB
- HD Audio supported by SPDIF
- Support IPMI 2.0 by iRIS module
- COM, USB 3.0, SATA 6Gb/s PCIe Mini and mSATA supported
- IEI One Key Recovery solution allows you to create rapid OS backup and recovery

1.4 Connectors

The connectors on the NANO-KBN-i1 are shown in the figure below.

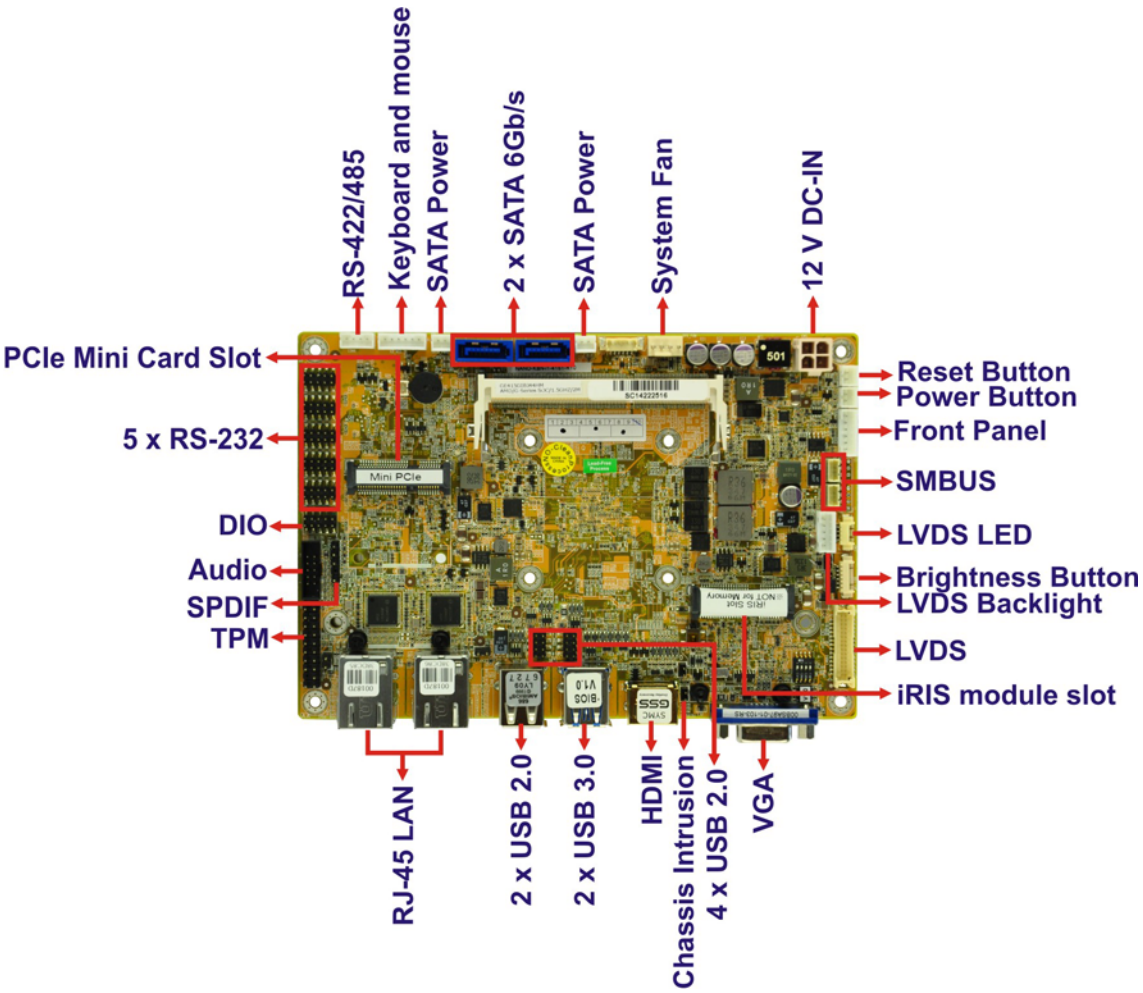
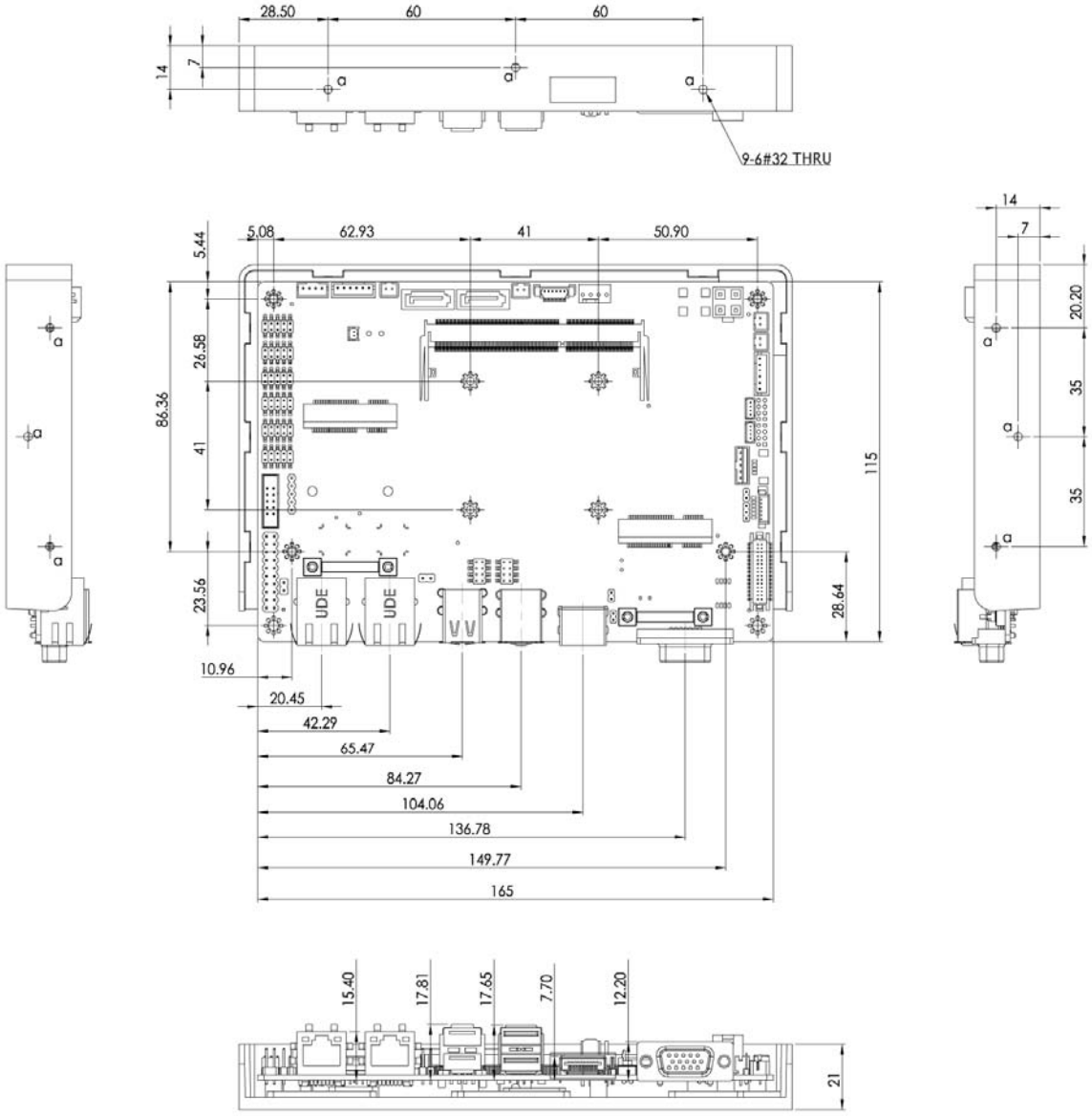


Figure 1-2: Connectors

1.5 Dimensions

The dimensions of the board are listed below:



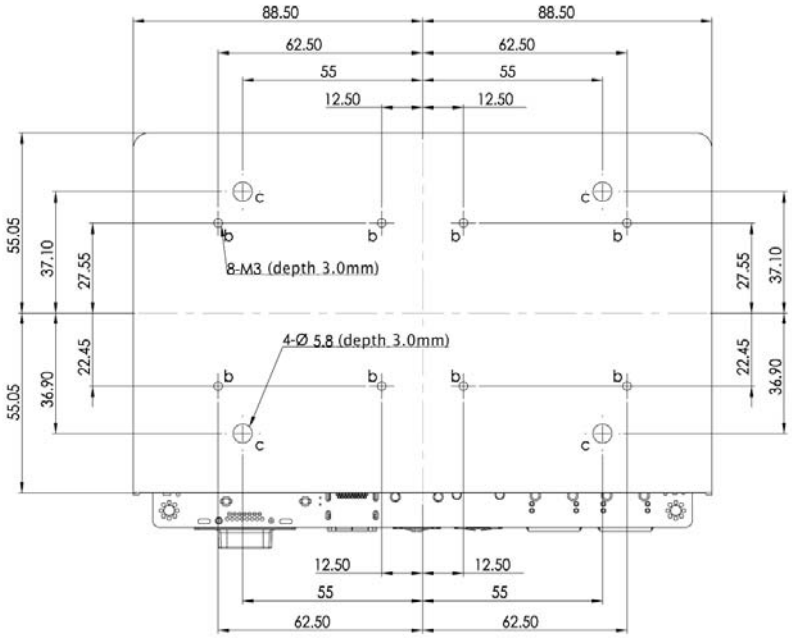


Figure 1-3: Dimensions (mm)

1.6 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

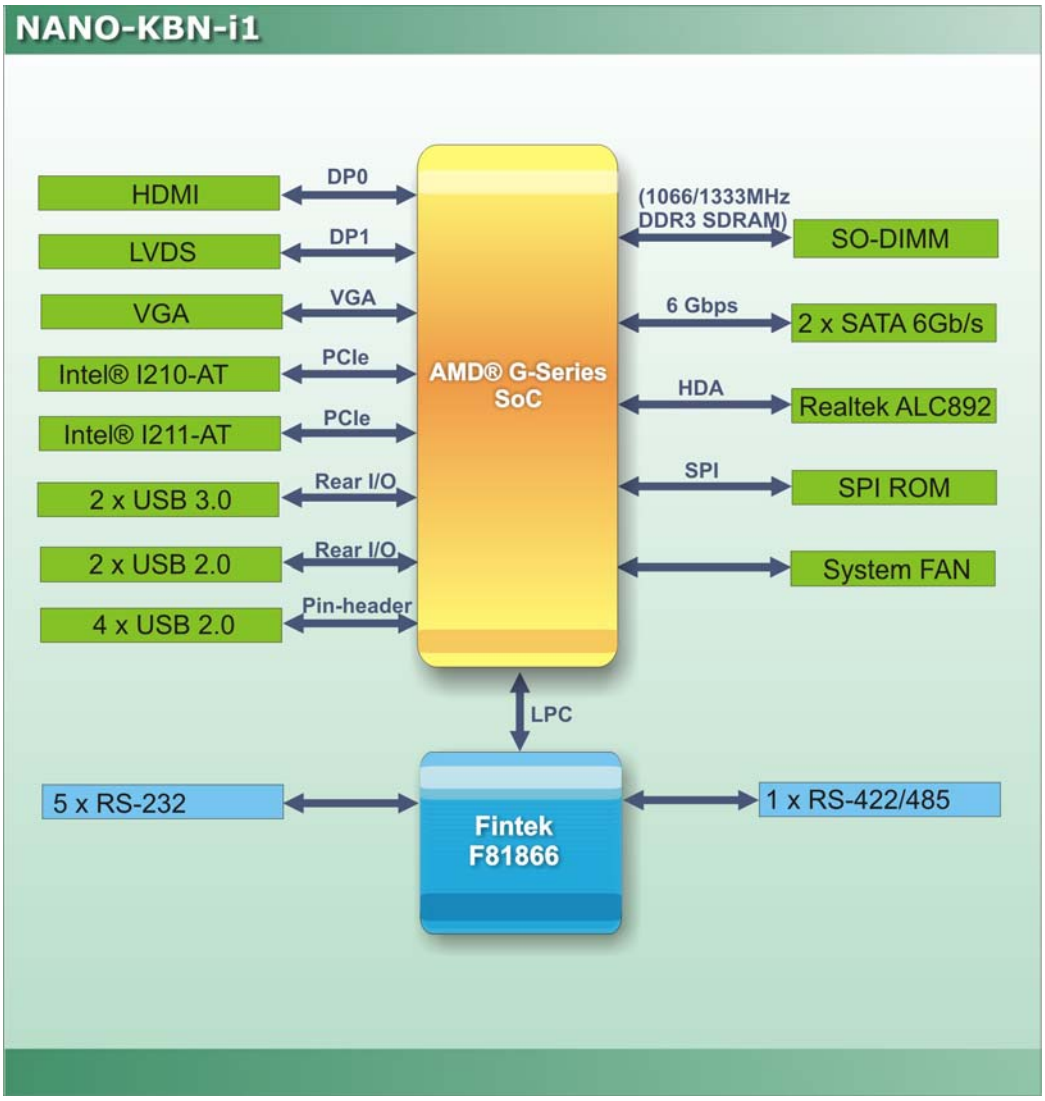


Figure 1-4: Data Flow Diagram

1.7 Technical Specifications

NANO-KBN-i1 technical specifications are listed below.

Specification	NANO-KBN-i1
SoC	AMD® Embedded G-Series SoC GX-415GA on-board SoC (1.5GHz, quad-core, 2MB cache, TDP=15W) GX-210HA on-board SoC (1.0GHz, dual-core, 1MB cache, TDP=9W) GX-420CA on-board SoC (2.0GHz, quad-core, 2MB cache, TDP=25W) (by request) GX-217GA on-board SoC (1.65GHz, dual-core, 1MB cache, TDP=15W) (by request)
Memory	One 204-pin 1600/1333 MHz dual-channel DDR3 & DDR3L SDRAM unbuffered SO-DIMM support up to 8GB
BIOS	UEFI BIOS
Ethernet	GbE1: Intel® I210-AT PCIe controller with NCSI support GbE2: Intel® I211-AT PCIe controller
Graphics	GPU frequency 500MHz (Radeon™ HD 8330E) for GX-415GA GPU frequency 450MHz (Radeon™ HD 8310E) for GX-210HA GPU frequency 600MHz (Radeon™ HD 8400E) for GX-420CA GPU frequency 300MHz (Radeon™ HD 8280E) for GX-217GA Support DX11.1, OpenGL 4.1 and OpenCL1.2 UVD4.2 decode for H.264, MPEG2/4, VC1, MVC VCE 2.0 encode for H.264, VCE

Specification	NANO-KBN-i1
Display Output	1 x VGA (2560x1600) 1 x HDMI via v1.4a compliant (2560x1600) 1 x 24-bit dual channel LVDS by CH7511B DP to LVDS converter (1920x1200)
Super IO	Fintek F81866
Audio	Realtek ALC892 HD codec 1 x SPDIF by 4-pin (1x4) header for digital audio 1 x Analog audio by 10-pin (2x5) header
Watchdog Timer	Software programmable supports 1~255 sec. system reset
I/O Interface Connectors	
KB/MS	1 x 6-pin wafer for PS/2 KB/MS
Serial Ports	5 x RS-232 (by pin header) 1 x RS-422/485 (by pin header)
USB Ports	2 x USB 3.0 (on rear I/O) 6 x USB 2.0 (two on rear I/O, four by pin header)
TPM	1 x 20-pin (2x10) header
SMBUS	1 x 4-pin (1x4) wafer
I^2C	1 x 4-pin (1x4) wafer
Fan	1 x 4-pin system fan connector
LAN LED	2 x 2-pin (1x2) header
Front Panel	1 x 6-pin (1x6) wafer for power LED & HDD LED 1 x 2-pin (1x2) wafer for power button 1 x 2-pin (1x2) wafer for power reset
IPMI	1 x PCIe Mini slot supports iRIS-1010
Expansion	
PCIe	1 x Full-size PCIe Mini card slot (supports mSATA co-lay SATA port 2)
Storage	

Specification	NANO-KBN-i1
Serial ATA	2 x SATA 6G/s with 5V SATA power connector
Environmental and Power Specifications	
Power Supply	12V DC input only (AT/ ATX support) 1 x 4-pin (2x2) internal power jack
Operating Temperature	0°C ~ 60°C
Storage Temperature	-20°C ~ 85°C
Humidity	5% ~ 95% (non-condensing)
Physical Specifications	
Dimensions	115 mm x 165 mm
Weight (Gross/Net)	850g / 350g

Table 1-2: Technical Specifications

Chapter

2

Unpacking

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the NANO-KBN-i1 is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the NANO-KBN-i1 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The NANO-KBN-i1 is shipped with the following components:

Quantity	Item and Part Number	Image
1	NANO-KBN-i1 motherboard	
1	Audio cable (**P/N**: 32007-002600-200-RS)	
2	SATA with 5V output cable kit (**P/N**: 32801-000201-300-RS)	
2	RS-232 cable (**P/N**: 32205-002700-100-RS)	
1	Power cable (**P/N**: 32100-087100-RS)	
1	Utility CD	

1	One Key Recovery CD	
1	Quick Installation Guide	

2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
Dual-port USB cable without bracket (**P/N**: 32000-070301-RS)	
RS-422/485 cable, 200mm (**P/N**: 32205-003800-100-RS)	
PS/2 KB/MS cable (**P/N**: 32000-023800-RS)	
20-Pin Infineon TPM module, software management tool, firmware V3.17 (**P/N**: TPM-IN01-R11)	

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 NANO-KBN-i1 Layout

The figures below show all the connectors and jumpers.

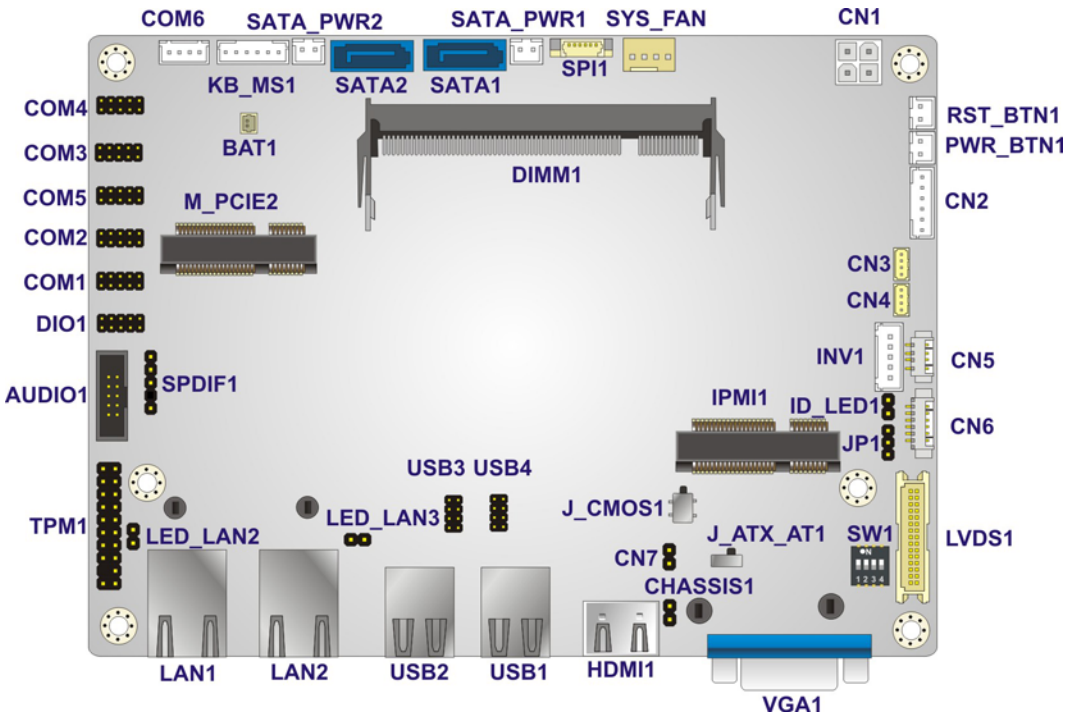


Figure 3-1: Connector and Jumper Locations

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
12V DC-IN power connector	4-pin Molex	CN1
Audio connector	10-pin box header	AUDIO1
Battery connector	2-pin wafer	BAT1
Brightness button connector	6-pin wafer	CN6

Chassis intrusion connector	2-pin header	CHASSIS1
DDR3 SO-DIMM slot	DDR3 SO-DIMM slot	DIMM1
Digital I/O connector	10-pin header	DIO1
Front panel connector	6-pin wafer	CN2
I2C connector	4-pin wafer	CN4
IPMI LED connector	2-pin header	ID_LED1
iRIS-1010 module slot	iRIS-1010 module slot	IPMI1
Keyboard and mouse connector	6-pin wafer	KB_MS1
LAN LED connectors	2-pin header	LED_LAN2, LED_LAN3
LVDS backlight inverter connector	5-pin wafer	INV1
LVDS LCD connector	30-pin crimp	LVDS1
LVDS LED connector	4-pin wafer	CN5
PCIe mini card slot	PCIe Mini card slot	M_PCIE2
Power button connector	2-pin wafer	PWR_BTN1
Reset button connector	2-pin wafer	RST_BTN1
RS-232 serial port connectors	10-pin header	COM1, COM2, COM3, COM4, COM5
RS-422/485 serial port connector	4-pin wafer	COM6
SATA 6Gb/s drive connectors	7-pin SATA connector	SATA1, SATA2
SATA power connectors	2-pin wafer	SATA_PWR1, SATA_PWR2
SMBus connector	4-pin wafer	CN3
SPDIF connector	5-pin header	SPDIF1
SPI flash connector (BIOS)	6-pin wafer	SPI1

SPI flash connector (EC)	2-pin header	CN7
System fan connector	4-pin wafer	SYS_FAN
TPM connector	20-pin connector	TPM1
USB 2.0 connectors	8-pin header	USB3, USB4

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
HDMI connector	HDMI Type A port	HDMI1
LAN connectors	RJ-45	LAN1, LAN2
USB 3.0 connectors	USB 3.0	USB1
USB 2.0 connectors	USB 2.0	USB2
VGA connector	15-pin female	VGA1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the NANO-KBN-i1.

3.2.1 12V DC-IN Power Connector

CN Label: **CN1**

CN Type: 4-pin Molex, p=4.2 mm

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

The connector supports the 12V power supply.

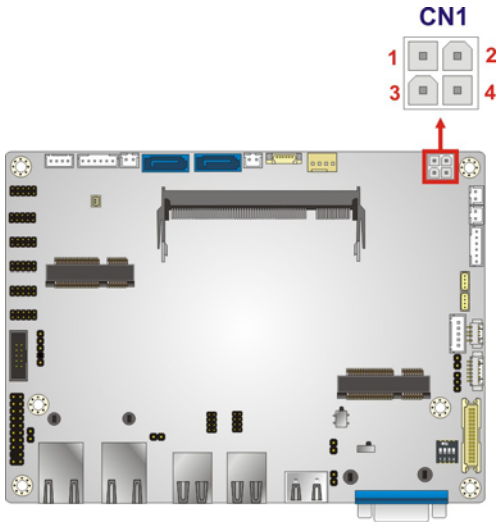


Figure 3-2: 12V DC-IN Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	12V-IN	4	12V-IN

Table 3-3: 12V DC-IN Power Connector Pinouts

3.2.2 Audio Connector

CN Label:	**AUDIO1**
CN Type:	10-pin box header, p=2.0 mm
CN Location:	See **Figure 3-3**
CN Pinouts:	See **Table 3-4**

The audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.

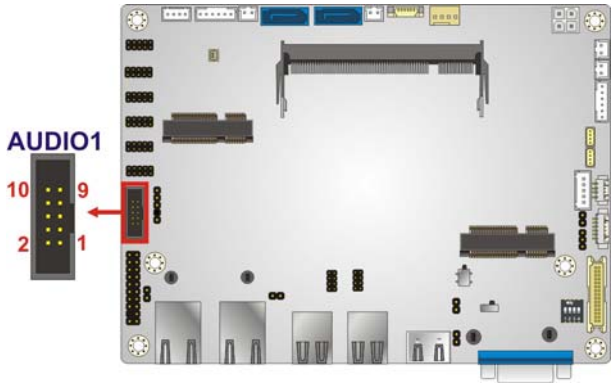


Figure 3-3: Audio Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LINEOUT1R	2	LINE1R
3	GND	4	GND
5	LINEOUT1L	6	LINE1L
7	GND	8	GND
9	FMIC1R	10	FMIC1L

Table 3-4: Audio Connector Pinouts

3.2.3 Battery Connector

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

CN Label:	**BAT1**
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-4**
CN Pinouts:	See **Table 3-5**

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.

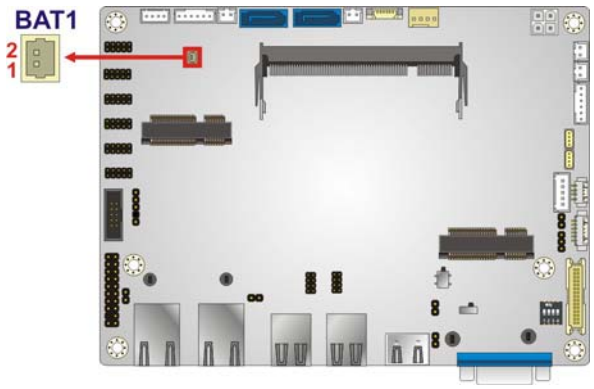


Figure 3-4: Battery Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VBATT	2	GND

Table 3-5: Battery Connector Pinouts

3.2.4 Brightness Button Connector

CN Label: **CN6**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The brightness button connector is connected to the brightness button.

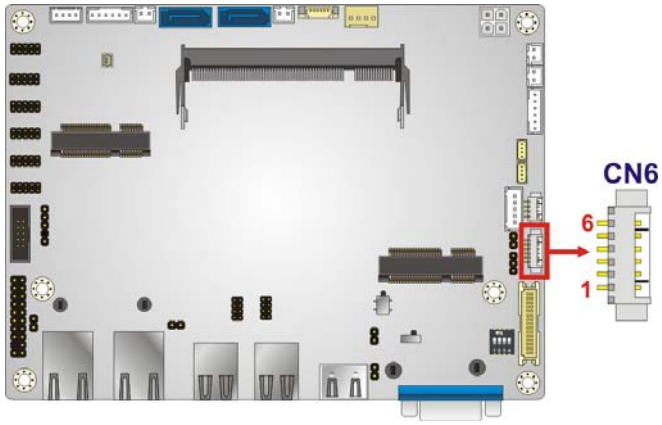


Figure 3-5: Brightness Button Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	PWRON	2	GND
3	BLUP	4	GND
5	BLDN	6	GND

Table 3-6: Brightness Button Connector Pinouts

3.2.5 Chassis Intrusion Connector

CN Label: **CHASSIS1**

CN Type: 2-pin header, p=2.0 mm

CN Location: See **Figure 3-6**

CN Pinouts: See **Table 3-7**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

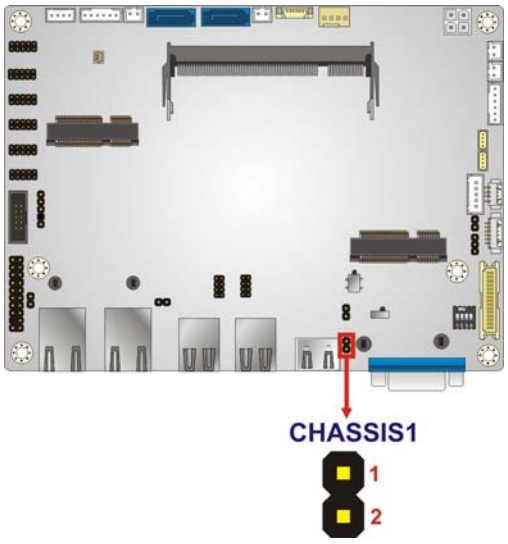


Figure 3-6: Chassis Intrusion Connector Location

Pin	Description
1	+V3.3A_EC
2	CHASSIE_EC

Table 3-7: Chassis Intrusion Connector Pinouts

3.2.6 DDR3 SO-DIMM Slot

CN Label: **DIMM1**

CN Type: DDR3 SO-DIMM slot

CN Location: See **Figure 3-7**

The DDR3 SO-DIMM slot is for DDR3 SO-DIMM memory module.

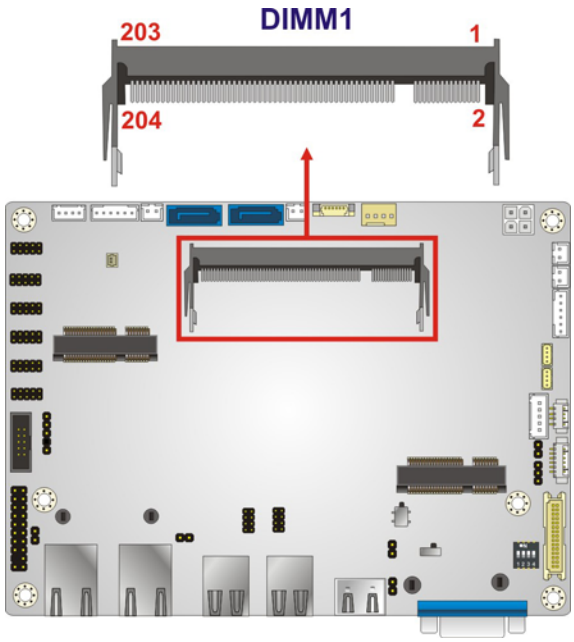


Figure 3-7: DDR3 SO-DIMM Slot Location

3.2.7 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header, p=2.0 mm

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-8**

The digital I/O connector provides programmable input and output for external devices. The digital I/O provides 4-bit output and 4-bit input.

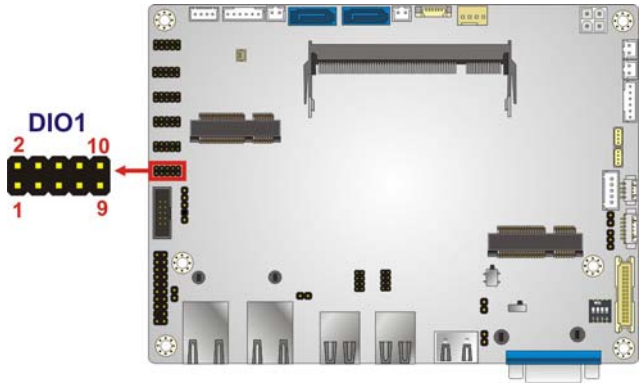


Figure 3-8: Digital I/O Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+5V
3	DOUT3	4	DOUT2
5	DOUT1	6	DOUT0
7	DIN3	8	DIN2
9	DIN1	10	DIN0

Table 3-8: Digital I/O Connector Pinouts

3.2.8 Front Panel Connector

CN Label: **CN2**

CN Type: 6-pin wafer, p=2.0 mm

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-10**

The front panel connector connects to the indicator LEDs on the system front panel.

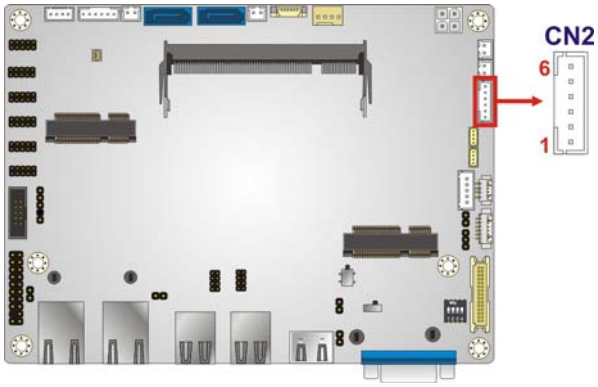


Figure 3-9: Front Panel Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	PWR_LED+	4	PWR_LED-
5	HDD_LED+	6	HDD_LED-

Table 3-9: Front Panel Connector Pinouts

3.2.9 I²C Connector

CN Label: **CN4**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-10**

CN Pinouts: See **Figure 3-10**

The I²C connector is for system debug.

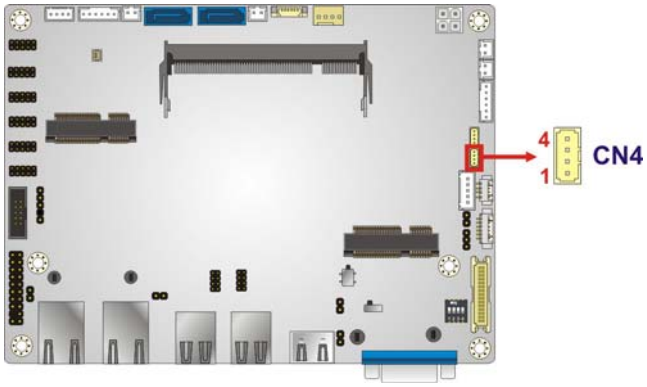


Figure 3-10: I²C Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	SDATA1
3	SCLK1	4	+5V

Table 3-10: I2C Connectors Pinouts

3.2.10 IPMI LED Connector

CN Label: **ID_LED1**

CN Type: 2-pin header, p=2.0 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-11**

The IPMI LED connector is used to connect to the IPMI LED indicator on the chassis.

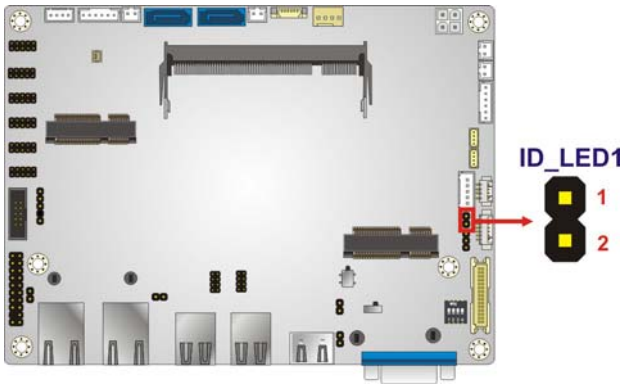


Figure 3-11: IPMI LED Connector Location

Pin	Description
1	ID_LED+
2	ID_LED-

Table 3-11: IPMI LED Connector Pinouts

3.2.11 iRIS-1010 Module Slot

CN Label:	**IPMI1**
CN Type:	IPMI 2.0 slot
CN Location:	See **Figure 3-12**

The iRIS-1010 module slot allows installation of the iRIS-1010 module.

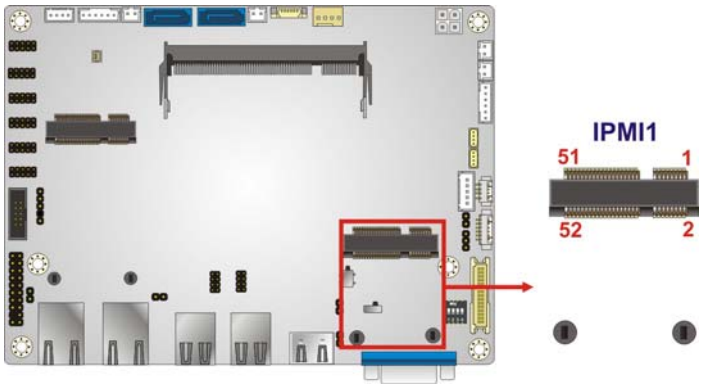


Figure 3-12: iRIS-1010 Module Slot Location

WARNING:

The iRIS-1010 module slot is designed to install the IEI iRIS-1010 IPMI 2.0 module. DO NOT install other modules into the iRIS-1010 module slot. Doing so may cause damage to the NANO-KBN-i1.

3.2.12 Keyboard and Mouse Connector

CN Label:	**KB_MS1**
CN Type:	6-pin wafer, p=2.0 mm
CN Location:	See **Figure 3-13**
CN Pinouts:	See **Table 3-12**

The keyboard/mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.

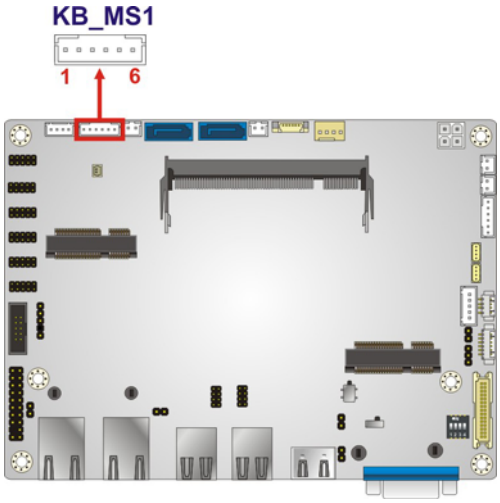


Figure 3-13: Keyboard and Mouse Location

Pin	Description
1	VCC
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

Table 3-12: Keyboard and Mouse Connector Pinouts

3.2.13 LAN LED Connectors

CN Label: **LED_LAN2, LED_LAN3**

CN Type: 2-pin header, p=2.54 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-13**

The LAN LED connectors connect to the LAN link LEDs on the system.

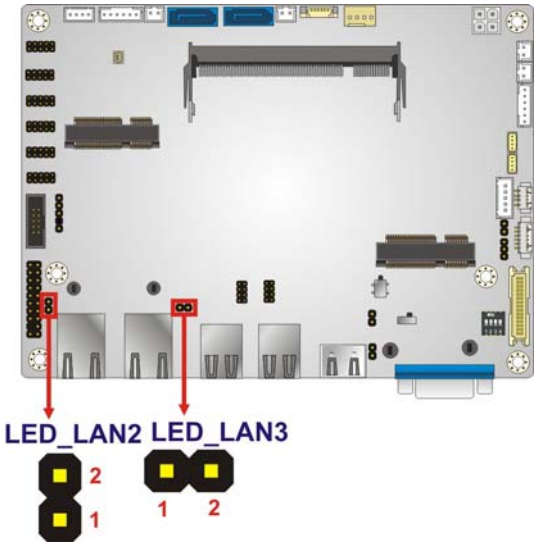


Figure 3-14: LAN LED Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	+3.3V	2	LAN_LED_LINK#_ACT

Table 3-13: LAN LED Connectors Pinouts

3.2.14 LVDS Backlight Inverter Connector

CN Label: **INV1**

CN Type: 5-pin wafer, p=2.0 mm

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-14**

The backlight inverter connector provides power to an LCD panel.

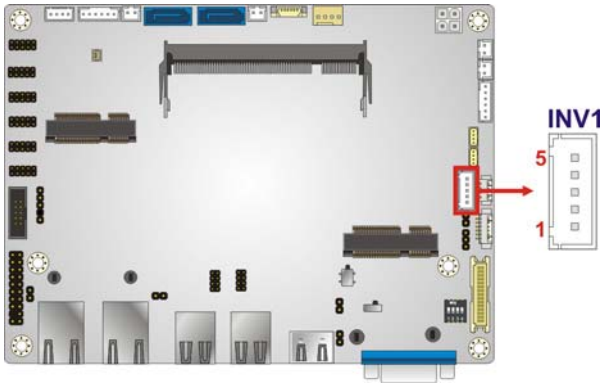


Figure 3-15: Backlight Inverter Connector Location

Pin	Description
1	BRIGHTNESS2
2	GND
3	12V
4	GND
5	ENABKL2

Table 3-14: Backlight Inverter Connector Pinouts

3.2.15 LVDS LCD Connector

CN Label: **LVDS1**

CN Type: 30-pin crimp, p=1.25 mm

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-15**

The LVDS connector is for an LCD panel connected to the board.

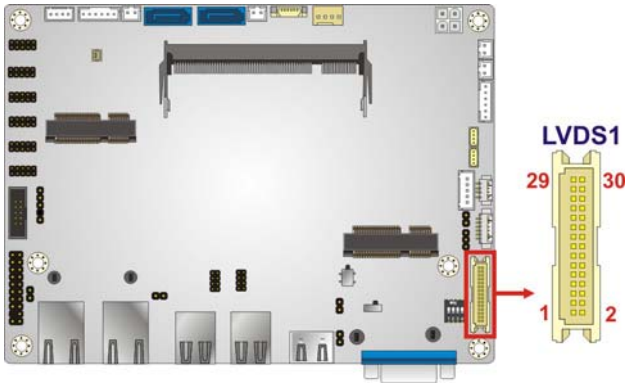


Figure 3-16: LVDS Connector Location

Pin	Description	Pin	Description
1	GROUND	2	GROUND
3	LVDS_A_TX0-P	4	LVDS_A_TX0-N
5	LVDS_A_TX1-P	6	LVDS_A_TX1-N
7	LVDS_A_TX2-P	8	LVDS_A_TX2-N
9	LVDS_A_TXCLK-P	10	LVDS_A_TXCLK-N
11	LVDS_A_TX3-P	12	LVDS_A_TX3-N
13	GROUND	14	GROUND
15	LVDS_B_TX0-P	16	LVDS_B_TX0-N
17	LVDS_B_TX1-P	18	LVDS_B_TX1-N
19	LVDS_B_TX2-P	20	LVDS_B_TX2-N
21	LVDS_B_TXCLK-P	22	LVDS_B_TXCLK-N
23	LVDS_B_TX3-P	24	LVDS_B_TX3-N
25	GROUND	26	GROUND
27	+LCD VCC	28	+LCD VCC
29	+LCD VCC	30	+LCD VCC

Table 3-15: LVDS Connector Pinouts

3.2.16 LVDS LED Connector

CN Label: **CN5**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-17**

CN Pinouts: See **Table 3-16**

The backlight inverter connector provides power to an LCD panel.

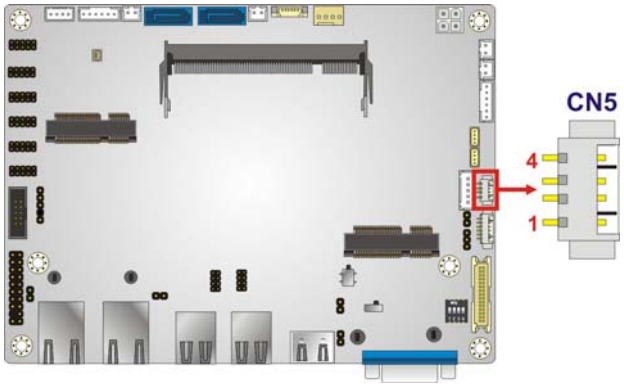


Figure 3-17: LVDS LED Connector Location

Pin	Description
1	VCC33
2	OLED
3	VCC33
4	GLED

Table 3-16: LVDS LED Connector Pinouts

3.2.17 PCIe Mini Card Slot

CN Label: **M_PCIE2**

CN Type: PCIe Mini card slot

CN Location: See **Figure 3-18**

The PCIe Mini card slot is for installing a PCIe Mini expansion card.

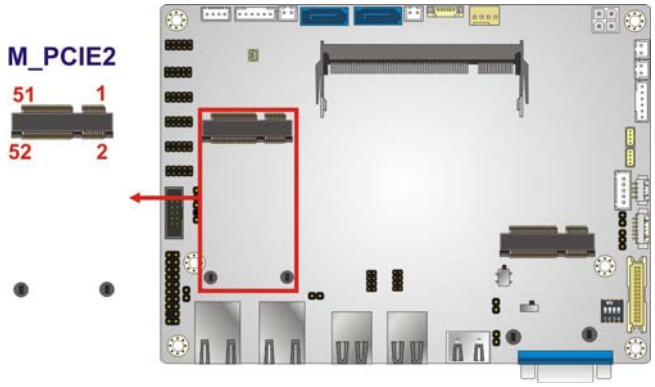


Figure 3-18: PCIe Mini Card Slot Location

3.2.18 Power Button Connector

CN Label: **PWR_BTN1**

CN Type: 2-pin wafer, p=2.0 mm

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-17**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

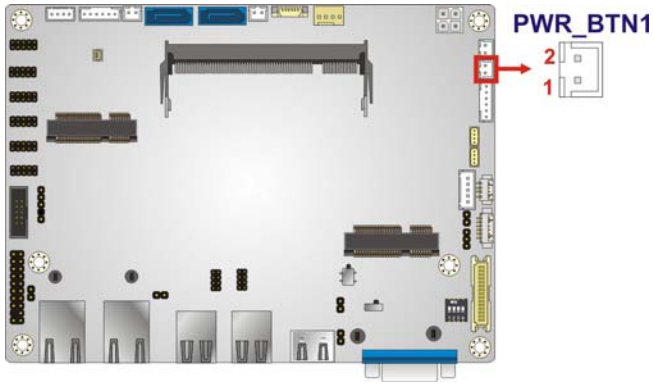


Figure 3-19: Power Button Connector Location

Pin	Description
1	PWRBTSW#
2	GND

Table 3-17: Power Button Connector Pinouts

3.2.19 Reset Button Connector

CN Label: **RST_BTN1**

CN Type: 2-pin wafer, p=2.0 mm

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-18**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

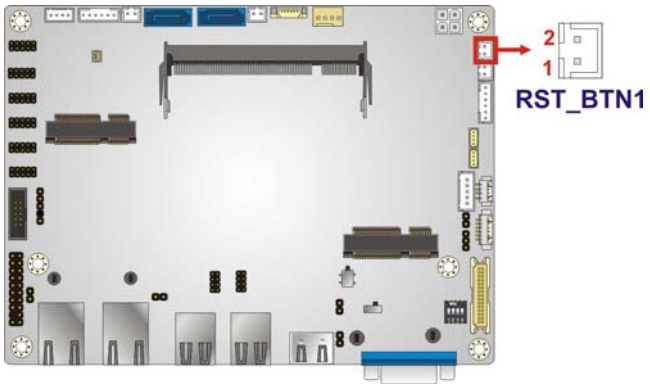


Figure 3-20: Reset Button Connector Location

Pin	Description
1	PM_SYSRST#
2	GND

Table 3-18: Reset Button Connector Pinouts

3.2.20 RS-232 Serial Port Connector

CN Label: **COM1, COM2, COM3, COM4, COM5**

CN Type: 10-pin header, p=2.0 mm

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-19**

The serial connector provides RS-232 connection.

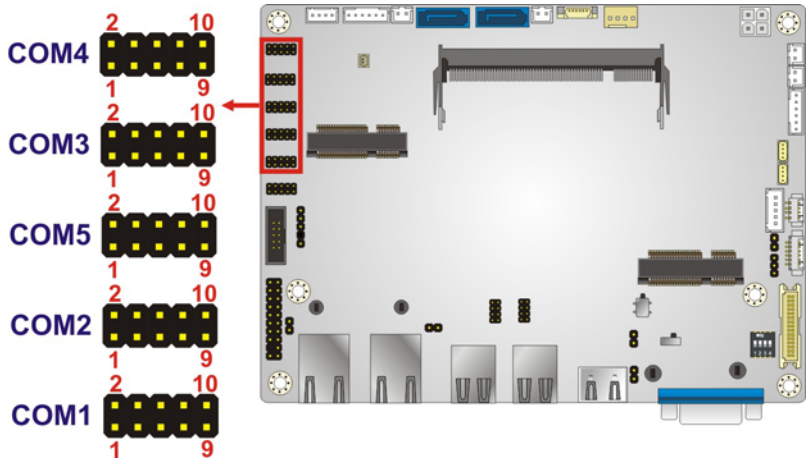


Figure 3-21: RS-232 Serial Port Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	NDCD	2	NDSR
3	NRX	4	NRTS
5	NTX	6	NCTS
7	NDTR	8	NRI
9	GND	10	GND

Table 3-19: RS-232 Serial Port Connector Pinouts

3.2.21 RS-422/485 Serial Port Connector

CN Label: **COM6**

CN Type: 4-pin wafer, p=2.0 mm

CN Location: See **Figure 3-22**

CN Pinouts: See **Table 3-20**

This connector provides RS-422 or RS-485 communications.

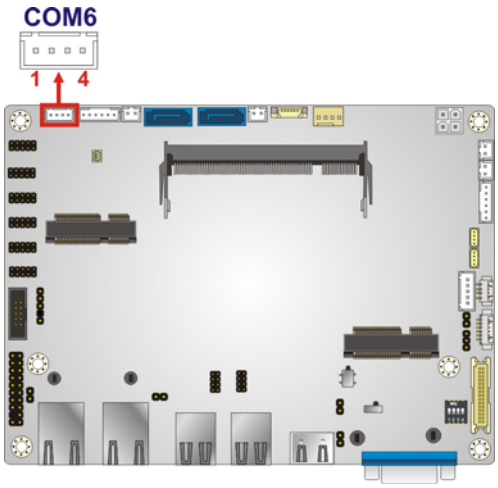


Figure 3-22: RS-422/485 Connector Location

Pin	Description	Pin	Description
1	RXD422-	2	RXD422+
3	TXD422+/TXD485+	4	TXD422-/TXD485-

Table 3-20: RS-422/485 Connector Pinouts

Use the optional RS-422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

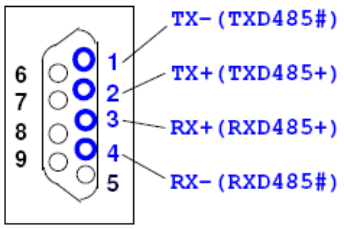
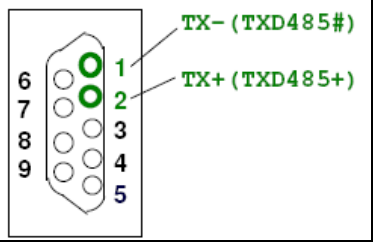
RS-422 Pinouts	RS-485 Pinouts
	

Table 3-21: DB-9 RS-422/485 Pinouts

3.2.22 SATA 6Gb/s Drive Connector

CN Label: **SATA1, SATA2**

CN Type: 7-pin SATA connector

CN Location: See **Figure 3-23**

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

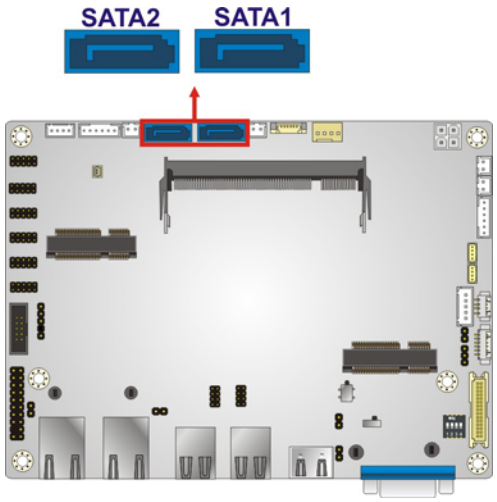


Figure 3-23: SATA 6Gb/s Drive Connector Location

3.2.23 SATA Power Connector

CN Label:	**SATA_PWR1, SATA_PWR2**
CN Type:	2-pin wafer, p=2.0 mm
CN Location:	See **Figure 3-24**
CN Pinouts:	See **Table 3-22**

The SATA power connector provides +5V power output to the SATA connector.

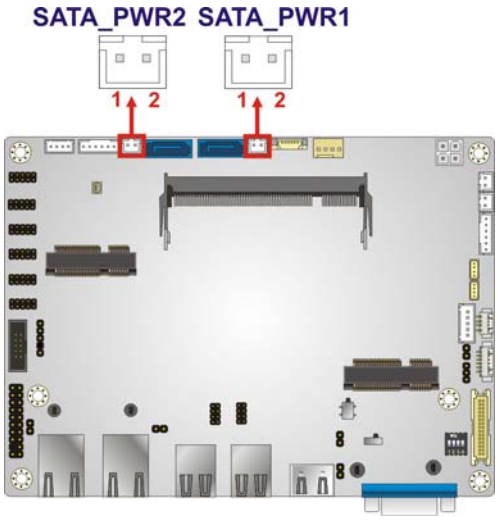


Figure 3-24: SATA Power Connector Location

PIN NO.	DESCRIPTION
1	+5V
2	GND

Table 3-22: SATA Power Connector Pinouts

3.2.24 SMBus Connector

CN Label: **CN3**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-23**

The SMBus (System Management Bus) connector provides low-speed system management communications.

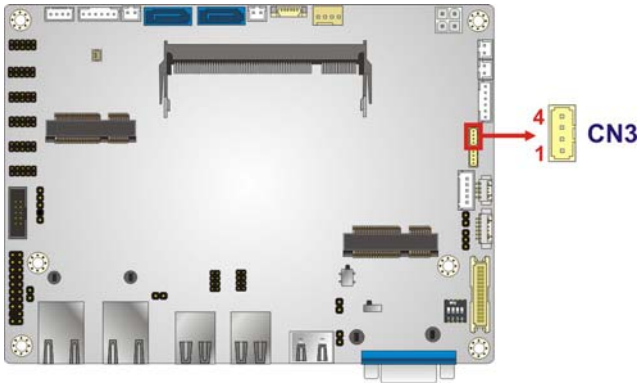


Figure 3-25: SMBus Connectors Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	SDATA0
3	SCLK0	4	+5V

Table 3-23: SMBus Connectors Pinouts

3.2.25 SPDIF Connector

CN Label: **SPDIF1**

CN Type: 5-pin header, p=2.54 mm

CN Location: See **Figure 3-26**

CN Pinouts: See **Table 3-24**

Use the SPDIF connector to connect digital audio devices to the system.

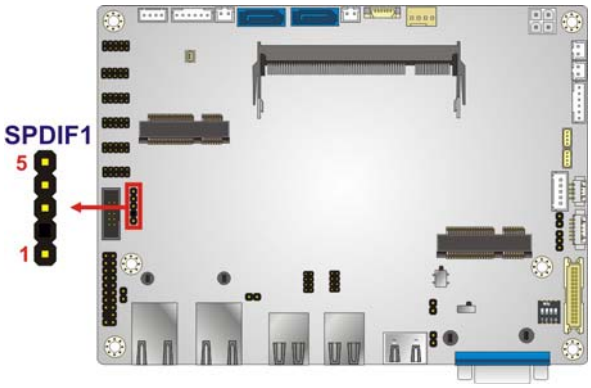


Figure 3-26: SPDIF Connector Location

PIN	DESCRIPTION
1	+5V
2	NC
3	SPDIF OUT
4	GND
5	SPDIF IN

Table 3-24: SPDIF Connector Pinouts

3.2.26 SPI Flash Connector (BIOS)

CN Label: **SPI1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-25**

The SPI Flash connector is used to flash the BIOS.

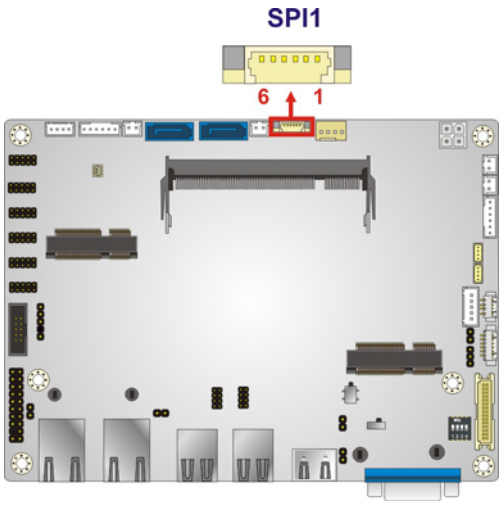


Figure 3-27: SPI Flash Connector Location

Pin	Description
1	SPI_POWER
2	SPI_CS#
3	SPI_DATAIN

Pin	Description
4	SPI_CLK
5	SPI_DATAOUT
6	GND

Table 3-25: SPI Flash Connector (BIOS) Pinouts

3.2.27 SPI Flash Connector (EC)

CN Label: **CN7**

CN Type: 2-pin header, p=2.0 mm

CN Location: See **Figure 3-28**

CN Pinouts: See **Table 3-26**

The SPI Flash connector is used to flash the Embedded Controller.

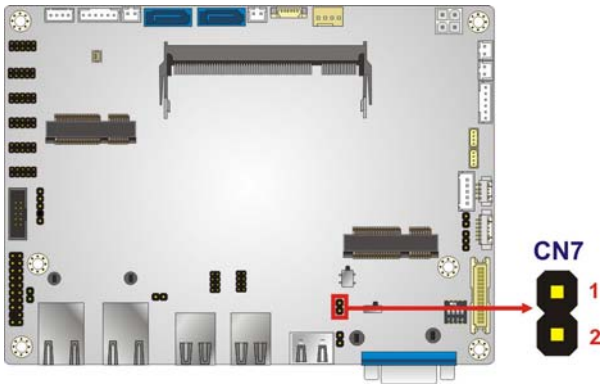


Figure 3-28: SPI Flash Connector Location

Pin	Description	Pin	Description
1	SMCLK1_EC	2	SMDAT1_EC

Table 3-26: SPI Flash Connector (EC) Pinouts

3.2.28 System Fan Connector

CN Label: **SYS_FAN**

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-27**

The fan connector attaches to a system cooling fan.

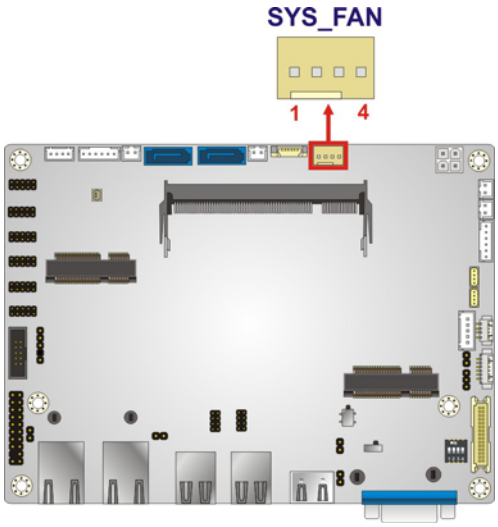


Figure 3-29: System Fan Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+12V
3	FANIN	4	FANOUT

Table 3-27: System Fan Connector Pinouts

3.2.29 TPM Connector

CN Label: **TPM1**

CN Type: 20-pin connector, p=2.54 mm

CN Location: See **Figure 3-30**

CN Pinouts: See **Table 3-28**

The Trusted Platform Module (TPM) connector secures the system on bootup.

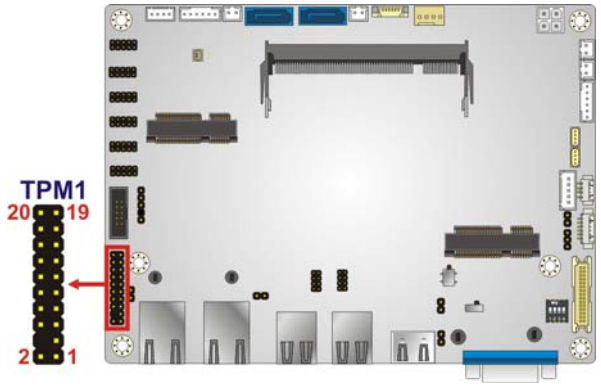


Figure 3-30: TPM Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LPC_CLK1	2	GND
3	LFRAME#	4	NC
5	LPC_RST#	6	+5V
7	LAD3	8	LAD2
9	+3.3V	10	LAD1
11	LAD0	12	GND
13	SCLK0	14	SDATA0
15	+3.3V_DUAL	16	SERIRQ
17	GND	18	LPC_CLKRUN#
19	LPCPD#	20	LDRQ#0

Table 3-28: TPM Connector Pinouts

3.2.30 USB Connector

CN Label: **USB3, USB4**

CN Type: 8-pin header, p=2.0 mm

CN Location: See **Figure 3-31**

CN Pinouts: See **Table 3-29**

The USB connector provides two USB 2.0 ports by dual-port USB cable.

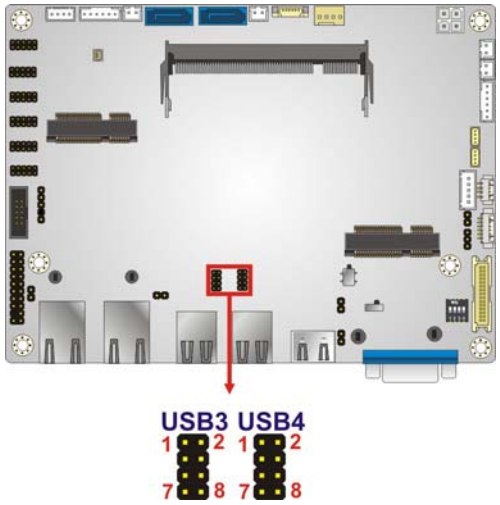


Figure 3-31: USB Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

Table 3-29: USB Connector Pinouts

3.3 External Peripheral Interface Connector Panel

Figure 3-32 shows the NANO-KBN-i1 external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 1 x HDMI connector
- 2 x RJ-45 LAN connectors
- 2 x USB 3.0 connectors
- 2 x USB 2.0 connectors
- 1 x VGA connector

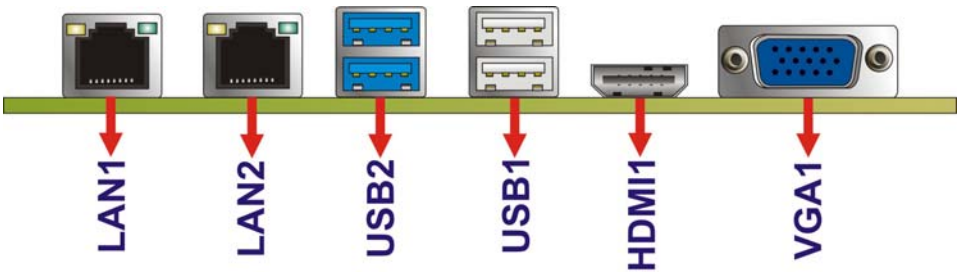


Figure 3-32: External Peripheral Interface Connector

3.3.1 HDMI Connector

CN Label: **HDMI1**

CN Type: HDMI type A connector

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-30**

The HDMI (High-Definition Multimedia Interface) connector connects to digital audio or video sources.

PIN	DESCRIPTION	PIN	DESCRIPTION
1	HDMI_TMDS_C_DATA2	2	GND
3	HDMI_TMDS_C_DATA2#	4	HDMI_TMDS_C_DATA1
5	GND	6	HDMI_TMDS_C_DATA1#
7	HDMI_TMDS_C_DATA0	8	GND
9	HDMI_TMDS_C_DATA0#	10	HDMI_TMDS_C_CLK
11	GND	12	HDMI_TMDS_C_CLK#
13	NC	14	NC
15	HDMI_DDC_SCLK	16	HDMI_DDC_SDATA
17	GND	18	+5V_HDMI
19	HDMI_HPD		

Table 3-30: HDMI Connector Pinouts

3.3.2 LAN Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-32**

CN Pinouts: See **Figure 3-33** and **Table 3-31**

The LAN connector connects to a local network.

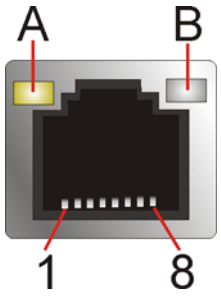


Figure 3-33: LAN Connector

Pin	Description	Pin	Description
1	MDI0+	2	MDI0-
3	MDI1+	4	MDI1-
5	MDI2+	6	MDI2-
7	MDI3+	8	MDI3-

Table 3-31: LAN Pinouts

LED	Description	LED	Description
A	on: linked blinking: data is being sent/received	B	off: 10 Mb/s green: 100 Mb/s orange: 1000 Mb/s

Table 3-32: Connector LEDs

3.3.3 USB Connectors

CN Label: **USB1, USB2**

CN Type: USB 2.0 ports, USB 3.0 ports

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-33** and **Table 3-34**

The NANO-KBN-i1 has two external USB 2.0 ports and two external USB 3.0 ports.

The pinouts of USB 2.0 connectors are shown below.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	POWER	2	DATA0_N
3	DATA0_P	4	GND
5	POWER	6	DATA1_N
7	DATA1_P	8	GND

Table 3-33: USB 2.0 Port Pinouts (USB1)

The pinouts of USB 3.0 connectors are shown below.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	USB_3P0_VCC1	2	USB2P8_DM0_L
3	USB2P8_DP0_L	4	GND
5	USB3P0_RXDN0_C	6	USB3P0_RXDP0_C
7	GND	8	USB3P0_TXDN0_C
9	USB3P0_TXDP0_C	10	USB_3P0_VCC2
11	USB2P9_DM1_L	12	USB2P9_DP1_L
13	GND	14	USB3P0_RXDN1_C
15	USB3P0_RXDP1_C	16	GND
17	USB3P0_TXDN1_C	18	USB3P0_TXDP1_C

Table 3-34: USB 3.0 Port Pinouts (USB2)

3.3.4 VGA Connector

CN Label: **VGA1**

CN Type: 15-pin Female

CN Location: See **Figure 3-32**

CN Pinouts: See **Table 3-35**

The VGA connector connects to a monitor that accepts a standard VGA input.

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	GND
7	GND	8	GND
9	CRT_VCC	10	GND
11	NC	12	5VDDCDA
13	VGA_HSYNC	14	VGA_VSYNC
15	5VDDCLK		

Table 3-35: VGA Connector Pinouts

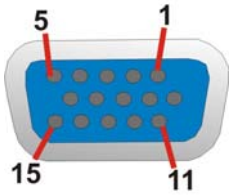


Figure 3-34: VGA Connector

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the NANO-KBN-i1 may result in permanent damage to the NANO-KBN-i1 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the NANO-KBN-i1. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the NANO-KBN-i1 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***: Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the NANO-KBN-i1, place it on an anti-static pad. This reduces the possibility of ESD damaging the NANO-KBN-i1.
- ***Only handle the edges of the PCB***: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the NANO-KBN-i1, NANO-KBN-i1 components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the NANO-KBN-i1 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the NANO-KBN-i1 on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the NANO-KBN-i1 off:
  - When working with the NANO-KBN-i1, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the NANO-KBN-i1 **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 SO-DIMM Installation

WARNING:

Using incorrectly specified SO-DIMM may cause permanently damage the NANO-KBN-i1. Please make sure the purchased SO-DIMM complies with the memory specifications of the NANO-KBN-i1. SO-DIMM specifications compliant with the NANO-KBN-i1 are listed in the specification table of Chapter 1.

To install an SO-DIMM, please follow the steps below and refer to Figure 4-1.

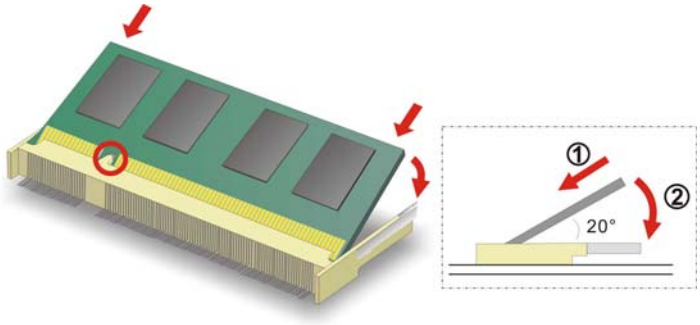


Figure 4-1: SO-DIMM Installation

Step 1: **Locate the SO-DIMM socket**. Place the board on an anti-static mat.

Step 2: **Align the SO-DIMM with the socket**. Align the notch on the memory with the notch on the memory socket.

Step 3: **Insert the SO-DIMM**. Push the memory in at a 20º angle. (See Figure 4-1)

Step 4: **Seat the SO-DIMM**. Gently push downwards and the arms clip into place. (See Figure 4-1)

4.4 System Configuration

The system configuration is controlled by buttons, jumpers and switches. The system configuration should be performed before installation.

4.4.1 AT/ATX Mode Select Switch

CN Label: **J_ATX_AT1**

CN Type: Switch

CN Location: See **Figure 4-2**

CN Settings: See **Table 4-1**

The AT/ATX mode select switch specifies the systems power mode as AT or ATX. AT/ATX mode select switch settings are shown in **Table 4-1**.

Setting	Description	
Short A-B	AT Mode	
Short B-C	ATX Mode	Default

Table 4-1: AT/ATX Mode Select Switch Settings

The location of the AT/ATX mode select switch is shown in **Figure 4-2** below.

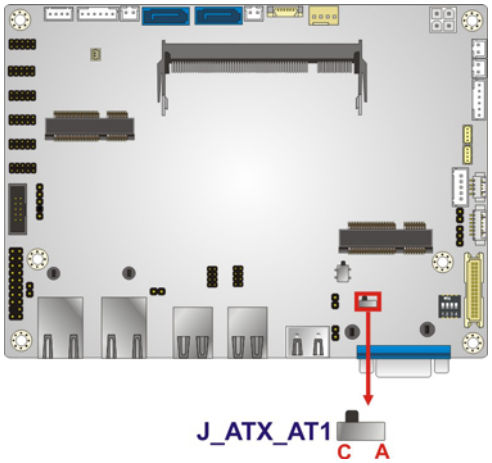


Figure 4-2: AT/ATX Mode Select Switch Location

4.4.1 Clear CMOS Button

CN Label: **J_CMOS1**

CN Type: Push button

CN Location: See **Figure 4-3**

CN Settings: See **Table 4-2**

If the NANO-KBN-i1 fails to boot due to improper BIOS settings, use the button to clear the CMOS data and reset the system BIOS information.

The clear CMOS button settings are shown in **Table 4-2**.

Setting	Description	
Open	Normal Operation	Default
Push	Clear CMOS Setup	

Table 4-2: Clear CMOS Button Settings

The location of the clear CMOS button is shown in **Figure 4-3**.

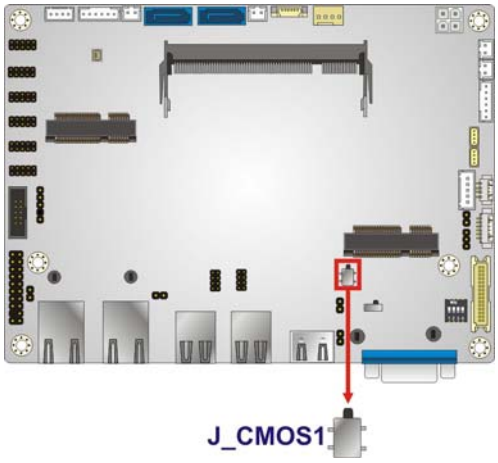


Figure 4-3: Clear CMOS Button Location

4.4.2 LVDS Panel Resolution Selection

Jumper Label: **SW1**

Jumper Type: DIP switch

Jumper Settings: See **Table 4-3**

Jumper Location: See **Figure 4-4**

Selects the resolution of the LCD panel connected to the LVDS connector.

* ON=0, OFF=1; Single=S, Dual=D

SW1 (4-3-2-1)	Description
0000	800x600 18-bit S (default)
0001	1024x768 18-bit S
0010	1024x768 24-bit S
0011	1280x768 18-bit S
0100	1280x800 18-bit S
0101	1280x960 18-bit S
0110	1280x1024 24-bit D
0111	1366x768 18-bit S
1000	1366x768 24-bit S
1001	1440x960 24-bit D
1010	1400x1050 24-bit D
1011	1600x900 24-bit D
1100	1680x1050 24-bit D
1101	1600x1200 24-bit D
1110	1920x1080 24-bit D
1111	1920x1200 24-bit D

Table 4-3: LVDS Panel Resolution Selection

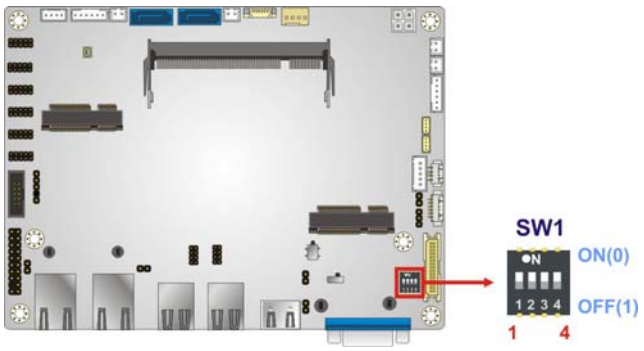


Figure 4-4: LVDS Panel Resolution Selection Switch Location

4.4.3 LVDS Voltage Selection

WARNING:

Permanent damage to the screen and NANO-KBN-i1 may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that came with the monitor to select the correct voltage.

Jumper Label:	**JP1**
Jumper Type:	3-pin header, p=2.0 mm
Jumper Settings:	See **Table 4-4**
Jumper Location:	See **Figure 4-5**

The LVDS voltage selection jumper allows setting the voltage provided to the monitor connected to the LVDS connector.

Setting	Description
Short 1-2	+3.3V
Short 2-3	+5V (Default)

Table 4-4: LVDS Voltage Selection Jumper Settings

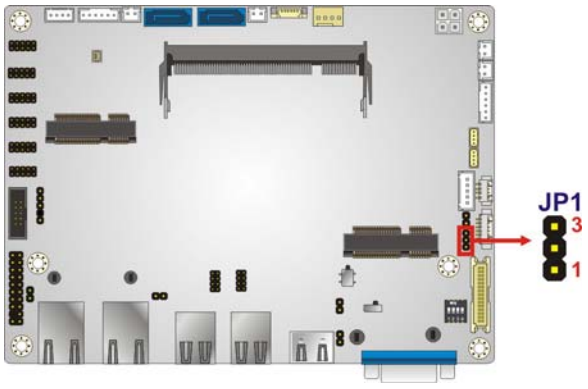


Figure 4-5: LVDS Voltage Selection Jumper Location

4.5 Chassis Installation

4.5.1 Heat Sink Enclosure

WARNING:

Never run the NANO-KBN-i1 without the heat sink secured to the board. The heat sink ensures the system remains cool and does not need addition heat sinks to cool the system.

WARNING:

When running the NANO-KBN-i1, do not put the NANO-KBN-i1 directly on a surface that can not dissipate system heat, especially the wooden or plastic surface. It is highly recommended to run the NANO-KBN-i1

→ on a heat dissipation surface or

→ using copper pillars to hold the board up from the chassis

When the NANO-KBN-i1 is shipped, it is secured to a heat sink with eight retention screws. If the NANO-KBN-i1 must be removed from the heat sink, the eight retention screws must be removed.

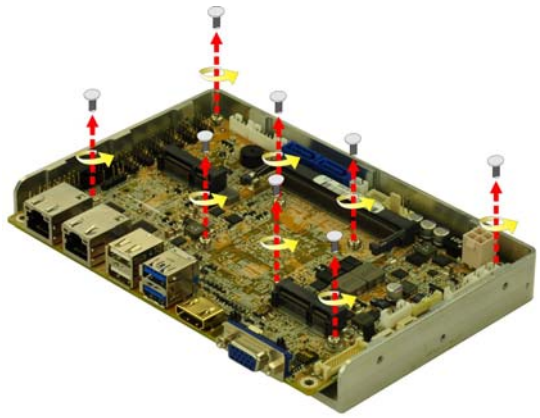


Figure 4-6: Heat Sink Retention Screws

4.5.2 Motherboard Installation

Each side of the heat sink enclosure has several screw holes allowing the NANO-KBN-i1 to be mounted into a chassis (please refer to Figure 1-3 for the detailed dimensions). The user can design or select a chassis that has screw holes matching up with the holes on the heat sink enclosure for installing the NANO-KBN-i1. The following diagram shows an example of motherboard installation.

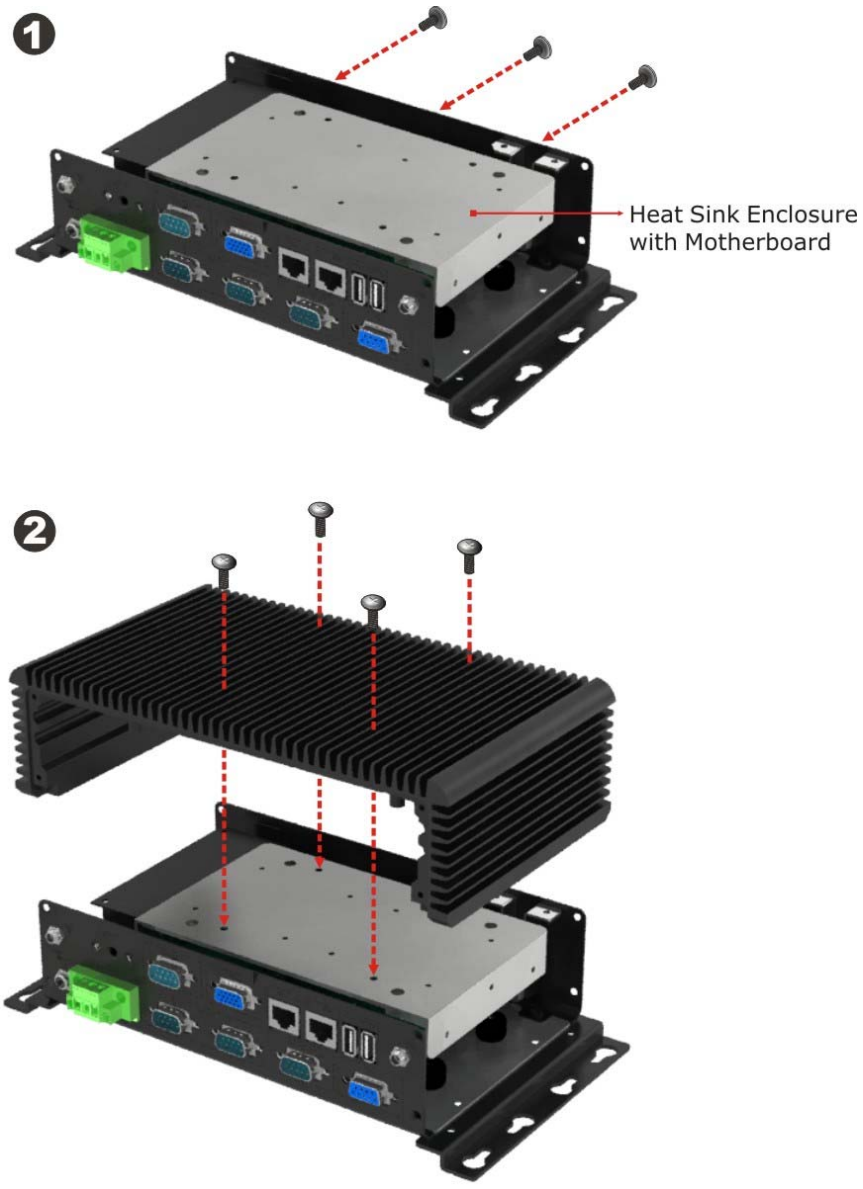


Figure 4-7: Motherboard Installation Example

4.6 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

4.6.1 Audio Kit Installation

The Audio Kit that came with the NANO-KBN-i1 connects to the audio connector on the NANO-KBN-i1. The audio kit consists of three audio jacks. Mic-in connects to a microphone. Line-in provides a stereo line-level input to connect to the output of an audio device. Line-out, a stereo line-level output, connects to two amplified speakers. To install the audio kit, please refer to the steps below:

Step 1: **Locate the audio connector**. The location of the 10-pin audio connector is shown in **Chapter 3**.

Step 2: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit connector. Pin 1 on the audio kit connector is indicated with a white dot. See **Figure 4-8**.

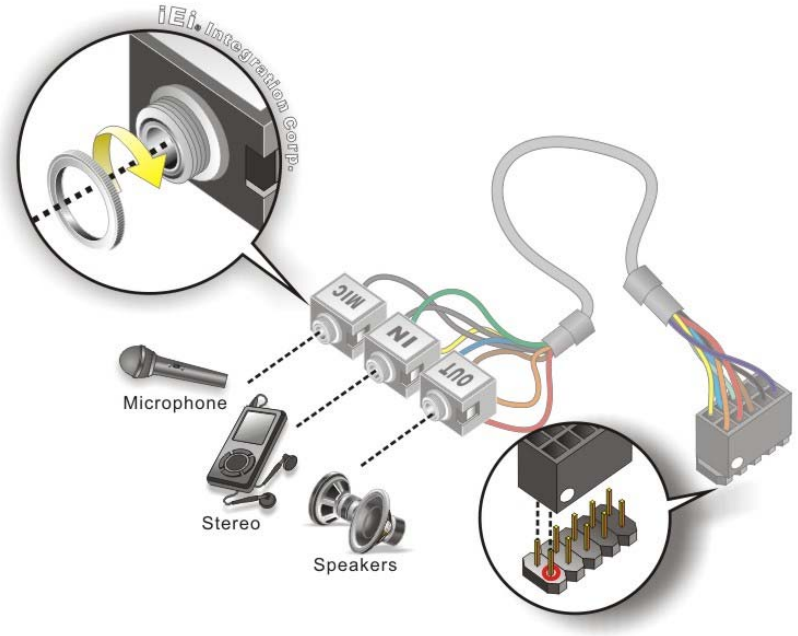


Figure 4-8: Audio Kit Cable Connection

Step 3: **Connect the audio devices**. Connect speakers to the line-out audio jack. Connect the output of an audio device to the line-in audio jack. Connect a microphone to the mic-in audio jack.

4.6.2 SATA Drive Connection

The NANO-KBN-i1 is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

Step 1: **Locate the SATA connector and the SATA power connector**. The locations of the connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-9**.

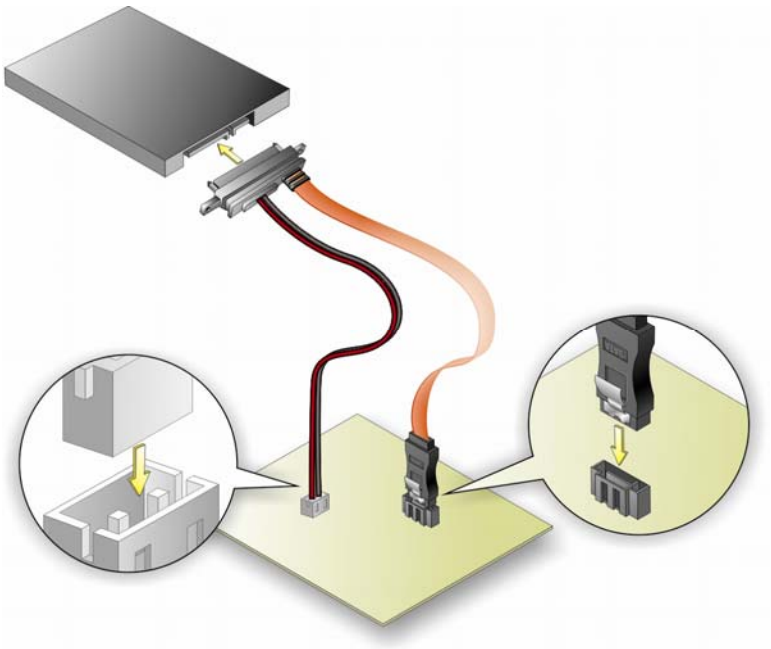


Figure 4-9: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-9**.

Step 4: To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

4.6.3 Single RS-232 Cable

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

Step 1: **Locate the connector**. The location of the RS-232 connector is shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the connector into the serial port box header. See Figure 4-10. A key on the front of the cable connectors ensures the connector can only be installed in one direction.

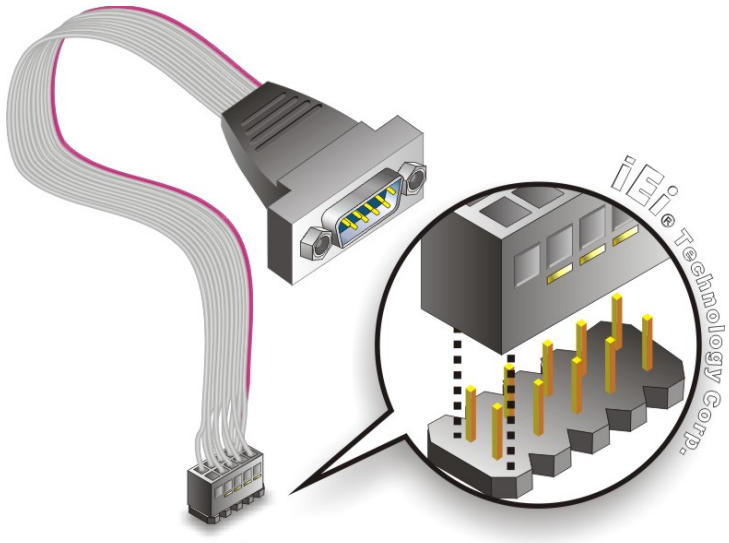


Figure 4-10: Single RS-232 Cable Installation

Step 3: **Secure the bracket**. The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.

Step 4: **Connect the serial device**. Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** or **F2** key as soon as the system is turned on or
2. Press the **DELETE** or **F2** key when the "**Press Del to enter SETUP**" message appears on the screen.

If the message disappears before the **DELETE** or **F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to the item above
Down arrow	Move to the item below
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes

Key	Function
-	Decrease the numeric value or make changes
Page up	Move to the next page
Page down	Move to the previous page
Esc	Main Menu – Quit and do not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F9	Load optimized defaults
F10	Save changes and Exit BIOS

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in Chapter **3**.

5.1.5 BIOS Menu Bar

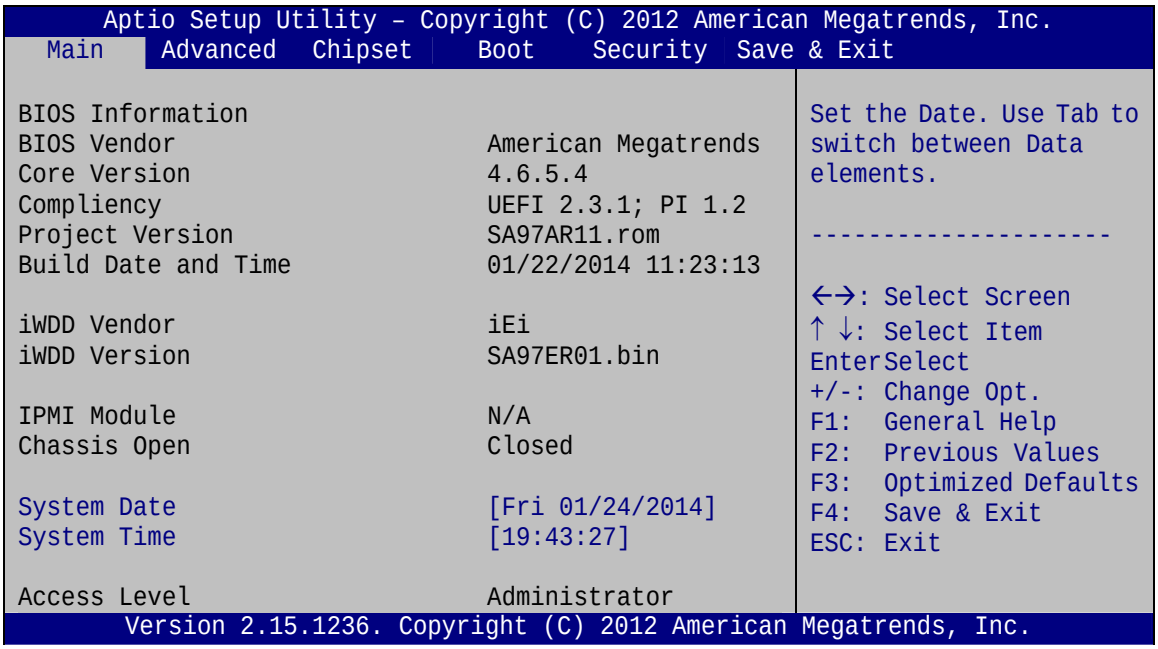
The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Boot – Changes the system boot configuration.
- Security – Sets User and Supervisor Passwords.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main

➔ BIOS Information

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliency:** Current compliant version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made

➔ **iWDD Vendor**

- The **iWDD Vendor** displays the installed iWDD vendor. The fields in **iWDD Vendor** cannot be changed.

➔ **iWDD Version**

- The **iWDD Version** displays the current iWDD version. The fields in **iWDD Version** cannot be changed.

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

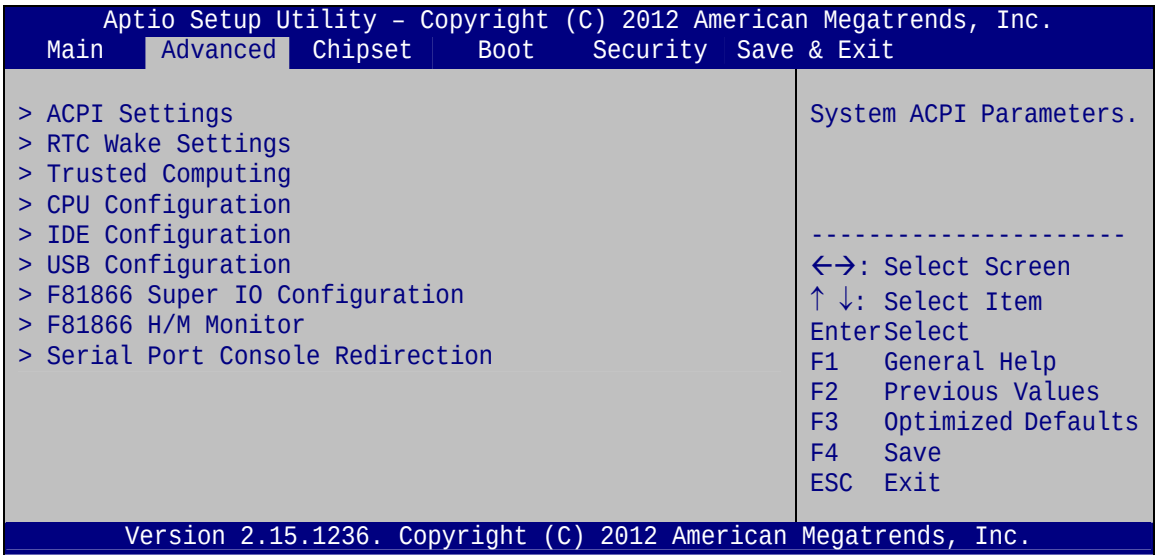
Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

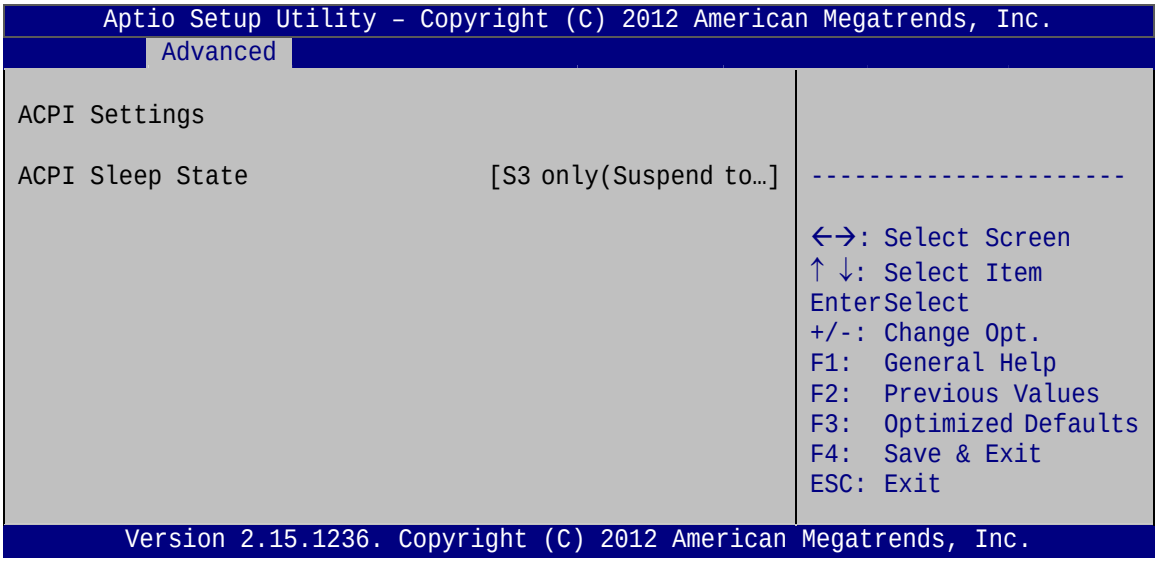
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



BIOS Menu 2: Advanced

5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



BIOS Menu 3: ACPI Configuration

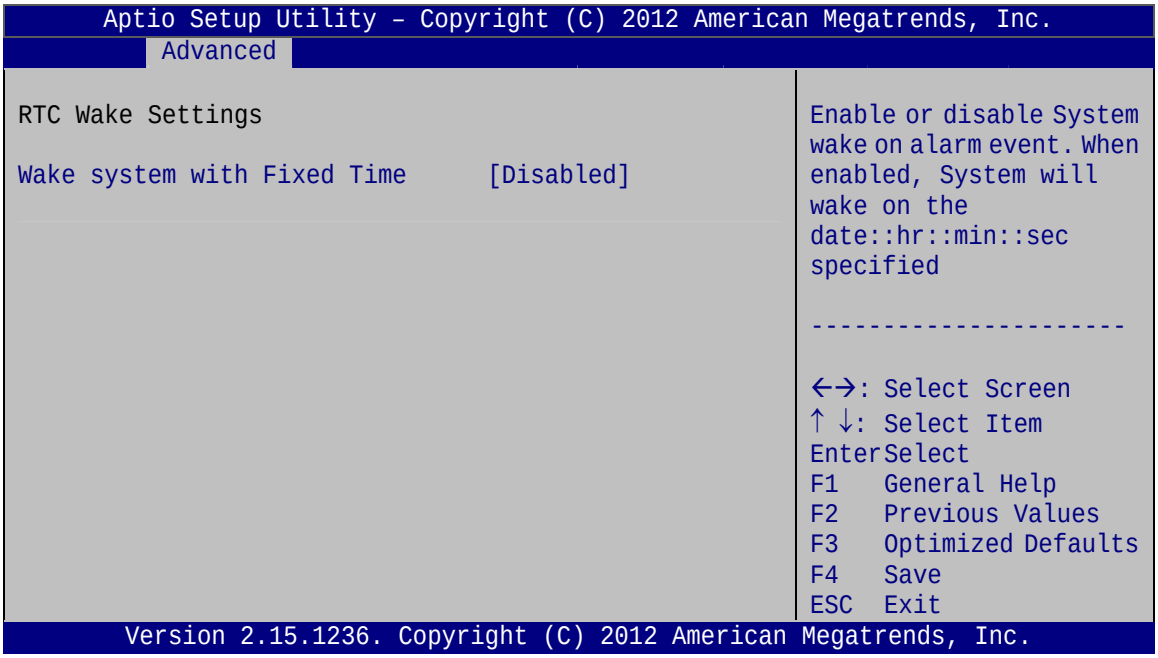
➔ **ACPI Sleep State [S3 only (Suspend to RAM)]**

The fields in **ACPI Sleep State** option cannot be changed.

➔ **S3 only (Suspend to RAM)** **DEFAULT** The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.2 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 4**) configures RTC wake event.



BIOS Menu 4: RTC Wake Settings

➔ **Wake system with Fixed Time [Disabled]**

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

➔ **Disabled** **DEFAULT** The real time clock (RTC) cannot generate a wake event

➔ **Enabled** If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be

selected:

Wake up date

Wake up hour

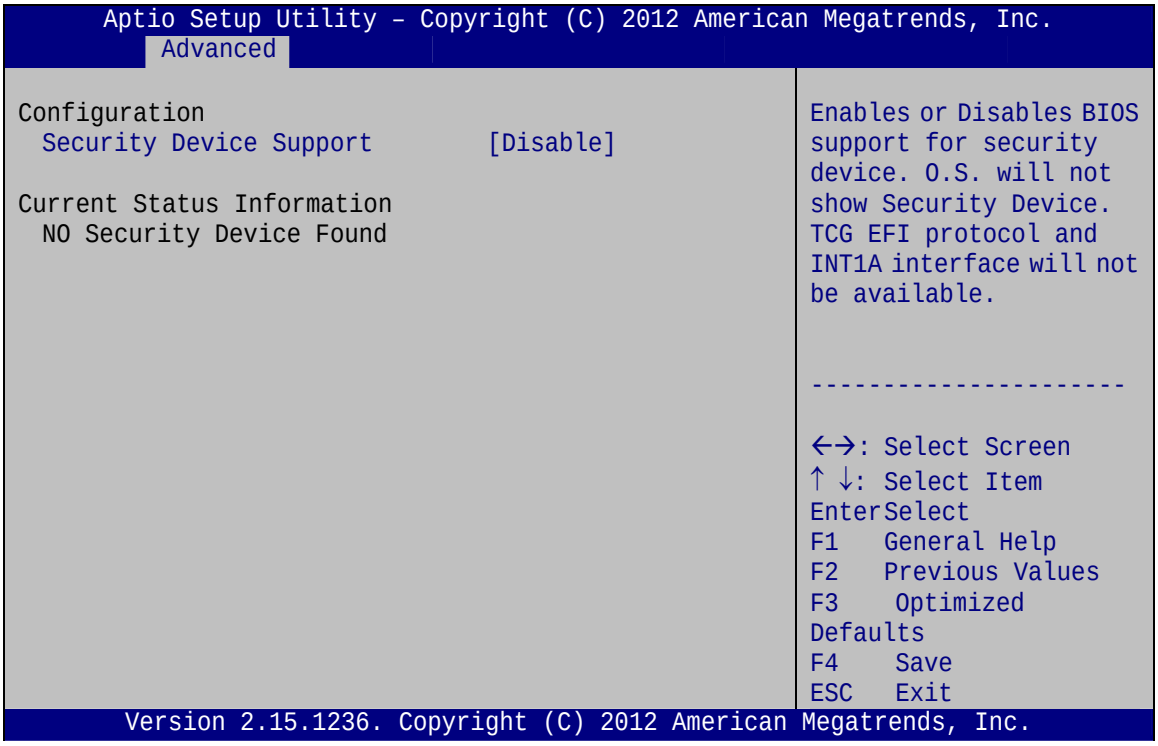
Wake up minute

Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.3 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 5**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).



BIOS Menu 5: Trusted Computing

➔ **Security Device Support [Disable]**

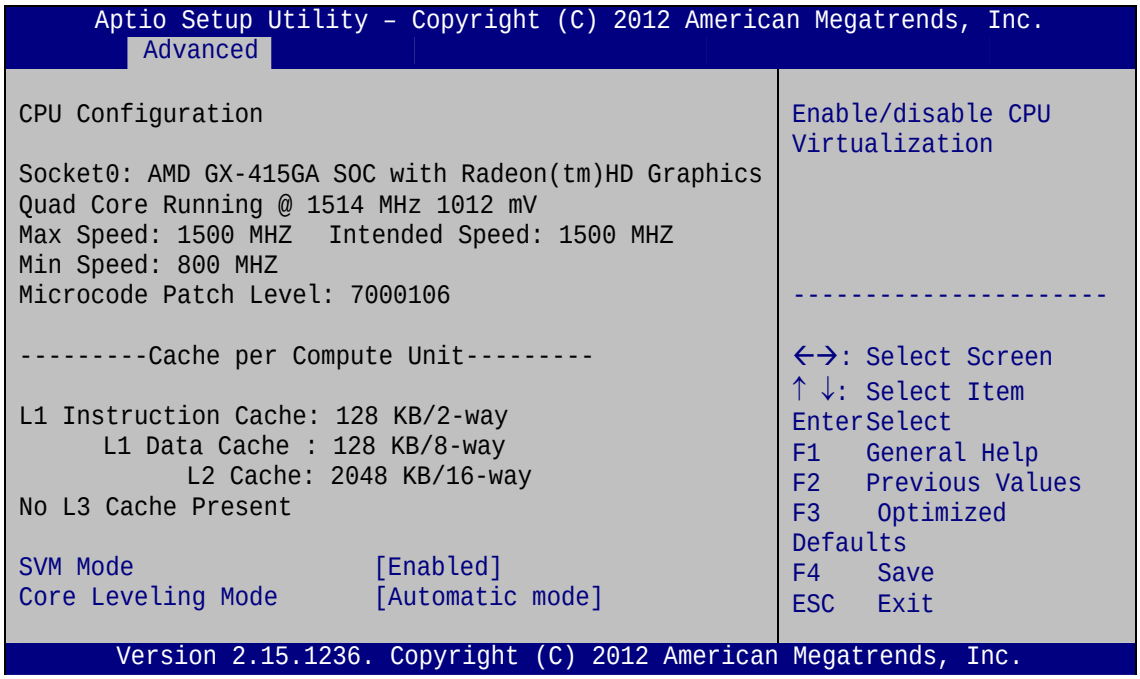
Use the **Security Device Support** option to configure support for the security device.

➔ **Disable** **DEFAULT** Security device support is disabled.

➔ **Enable** Security device support is enabled.

5.3.4 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 6**) to view detailed CPU specifications and configure the CPU.



BIOS Menu 6: CPU Configuration

➔ **SVM Mode [Enabled]**

Use the **SVM Mode** option to enable or disable the CPU virtualization function.

➔ **Disabled** Disables the CPU virtualization function

➔ **Enabled** **DEFAULT** Enables the CPU virtualization function

➔ **Core Leveling Mode [Automatic mode]**

Use the **Core Leveling Mode** option to configure the number of the active processor cores.

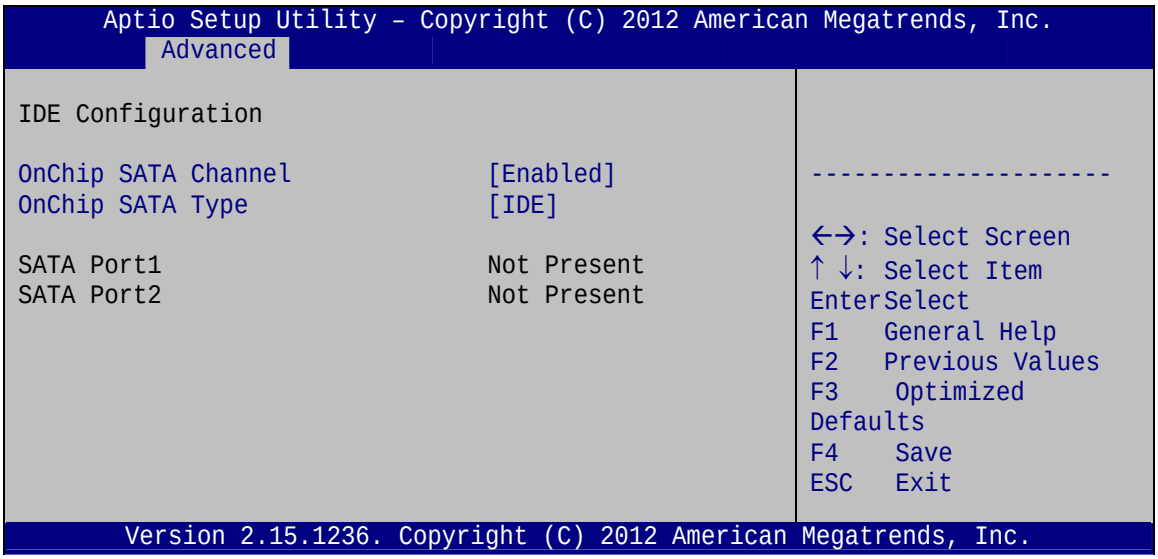
➔ **Automatic mode** **DEFAULT** Active the processor cores by automatic mode

➔ **Two cores per processor** Active two of the processor cores

➔ **One core per processor** Active one of the processor cores

5.3.5 IDE Configuration

Use the **IDE Configuration** menu (**BIOS Menu 7**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 7: IDE Configuration

➔ **OnChip SATA Channel [Enabled]**

Use the **OnChip SATA Channel** option to configure Onchip SATA channel.

➔ **Disabled** Disables Onchip SATA channel.

➔ **Enabled** **DEFAULT** Enables Onchip SATA channel.

➔ **OnChip SATA Type [IDE]**

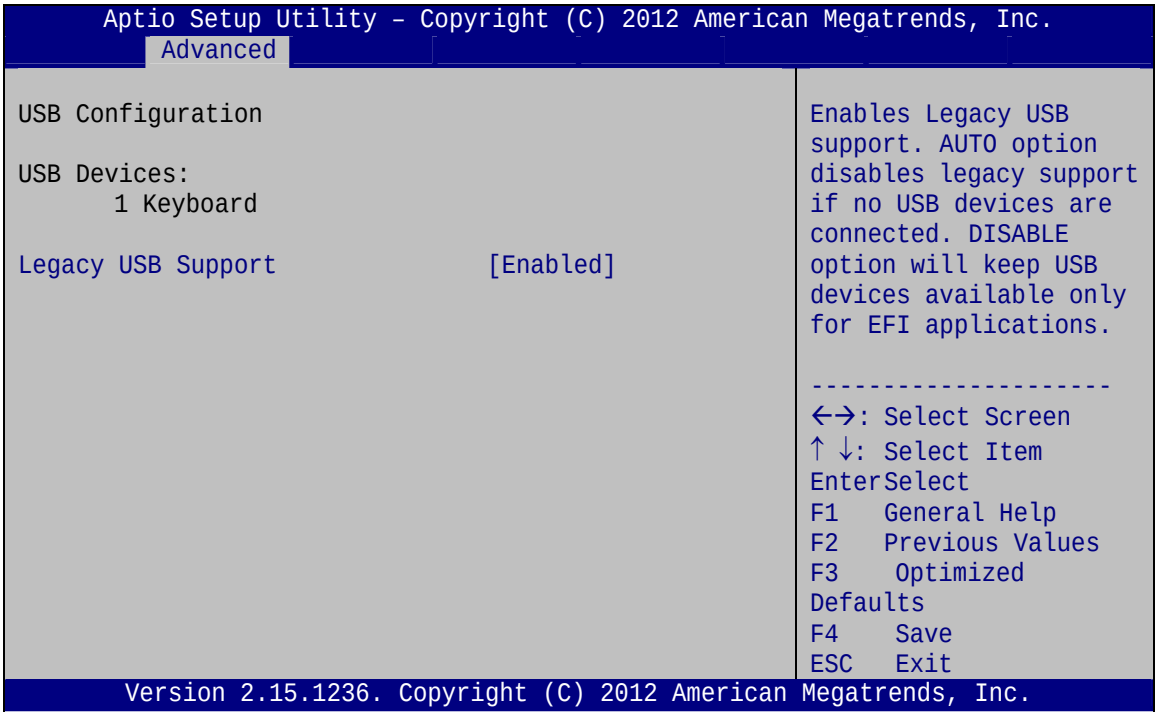
Use the **OnChip SATA Type** option to configure Onchip SATA type.

➔ **IDE** **DEFAULT** Configures SATA devices as normal IDE device.

➔ **AHCI** Configures SATA devices as AHCI device.

5.3.6 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 10**) to read USB configuration information and configure the USB settings.



BIOS Menu 8: USB Configuration

➔ **USB Devices**

The **USB Devices Enabled** field lists the USB devices that are enabled on the system

➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard

does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔	**Enabled**	**DEFAULT**	Legacy USB support enabled
➔	**Disabled**		Legacy USB support disabled
➔	**Auto**		Legacy USB support disabled if no USB devices are connected

5.3.7 F81866 Super IO Configuration

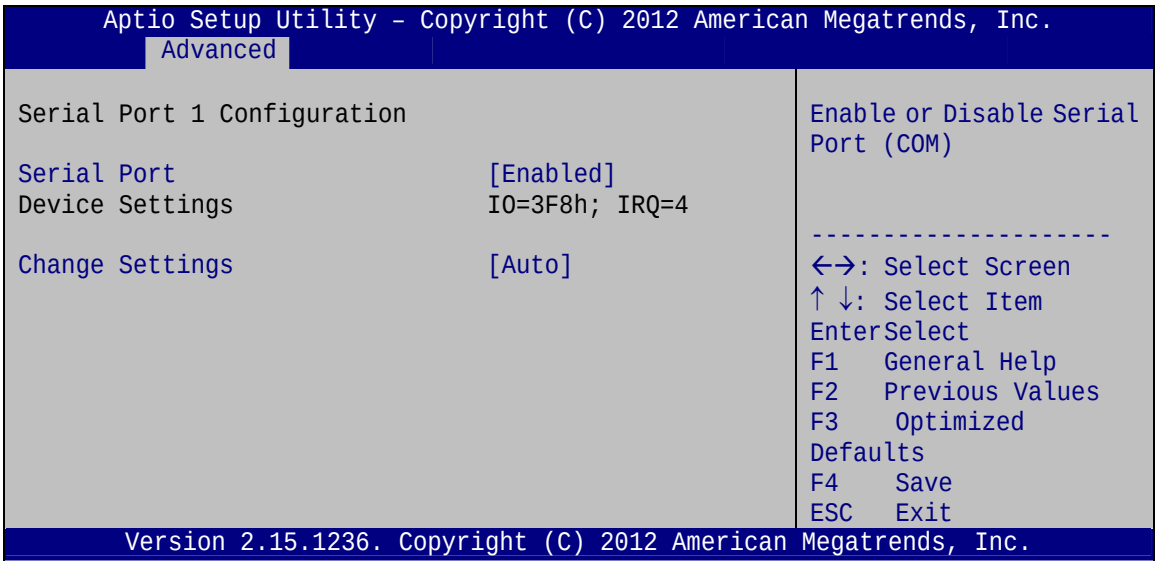
Use the **F81866 Super IO Configuration** menu (**BIOS Menu 9**) to set or change the configurations for the serial ports.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced
F81216 Super IO Configuration                  Set Parameters of Serial
                                               Port 1 (COMA)
Super IO Chip                    Fintek F81866
> Serial Port 1 Configuration                  ---------------------
> Serial Port 2 Configuration                  ←→: Select Screen
> Serial Port 3 Configuration                  ↑ ↓: Select Item
> Serial Port 4 Configuration                  EnterSelect
> Serial Port 5 Configuration                  F1   General Help
> Serial Port 6 Configuration                  F2   Previous Values
                                               F3    Optimized
                                               Defaults
                                               F4    Save
                                               ESC   Exit
        Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 9: Super IO Configuration

5.3.7.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 10**) to configure the serial port n.



BIOS Menu 10: Serial Port n Configuration

5.3.7.1.1 Serial Port 1 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** — Disable the serial port
- ➔ **Enabled** **DEFAULT** — Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **Auto** **DEFAULT** — The serial port IO port address and interrupt address are automatically detected.
- ➔ **IO=3F8h; IRQ=4** — Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

➔ **IO=3F8h; IRQ=3, 4,5,6,7,10,11,12**	Serial Port I/O port address is 3F8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2F8h; IRQ=3, 4,5,6,7,10,11,12**	Serial Port I/O port address is 2F8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**	Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**	Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.7.1.2 Serial Port 2 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2F8h; IRQ=3**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3
➔ **IO=3F8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3F8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2F8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2F8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.7.1.3 Serial Port 3 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=3E8h; IRQ=10**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ10
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D0h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.7.1.4 Serial Port 4 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2E8h; IRQ=10**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ10
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D0h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.7.1.5 Serial Port 5 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2D0h; IRQ=10**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ10
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D0h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.7.1.6 Serial Port 6 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

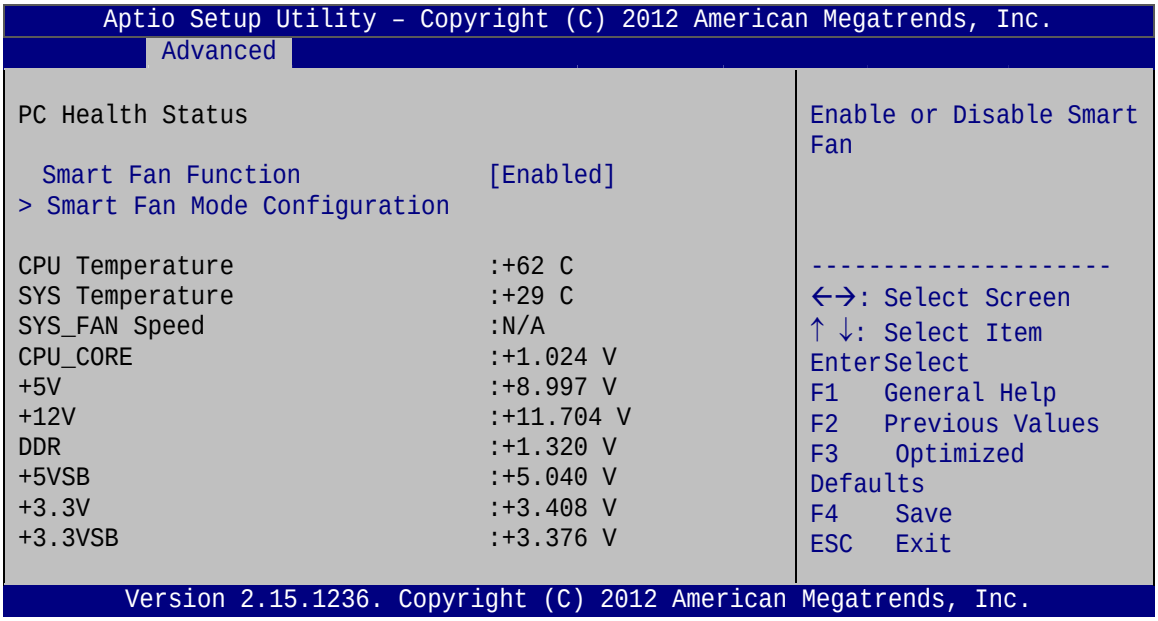
➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**	**DEFAULT**	The serial port IO port address and interrupt address are automatically detected.
➔ **IO=2D8h; IRQ=10**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ10
➔ **IO=3E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2E8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D0h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D0h and the interrupt address is IRQ3,4,5,6,7,10,11,12
➔ **IO=2D8h; IRQ=3, 4,5,6,7,10,11,12**		Serial Port I/O port address is 2D8h and the interrupt address is IRQ3,4,5,6,7,10,11,12

5.3.8 F81866 H/W Monitor

The **F8186 H/W Monitor** menu (**BIOS Menu 11**) shows the operating temperature, fan speeds and system voltages.



BIOS Menu 11: Hardware Health Configuration

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - CPU Temperature
  - SYS Temperature
- Fans Speeds:
  - SYS FAN Speed
- Voltages:
  - CPU_CORE
  - +5V
  - +12V
  - DDR
  - +5VSB

- +3.3V
- +3.3VSB

➔ **Smart Fan Function [Enabled]**

Use the **Smart Fan Function** option to enable or disable the smart fan function.

➔ **Disabled**		Disables the smart fan function.
➔ **Enabled**	**DEFAULT**	Enables the smart fan function.

5.3.8.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 12**) to configure the smart fan temperature and speed settings.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced
Smart Fan Mode Configuration                    Smart Fan Mode Select

SYS_FAN Smart Fan Control       [Auto Duty-Cycle Mode]
SYS Temperature 1               60
SYS Temperature 2               50
SYS Temperature 3               40
SYS Temperature 4               30

                                                ---------------------
                                                ←→: Select Screen
                                                ↑ ↓: Select Item
                                                EnterSelect
                                                + -   Change Opt.
                                                F1    General Help
                                                F2    Previous Values
                                                F3    Optimized Defaults
                                                F4    Save & Exit
                                                ESC   Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 12: Smart Fan Configuration

➔ **SYS_FAN Smart Fan Control [Auto Duty-Cycle Mode]**

Use the **SYS_FAN Smart Fan Control** option to configure the System Smart Fan.

➔ **Manual Duty Mode** The fan spins at the speed set in Manual by Duty Cycle settings

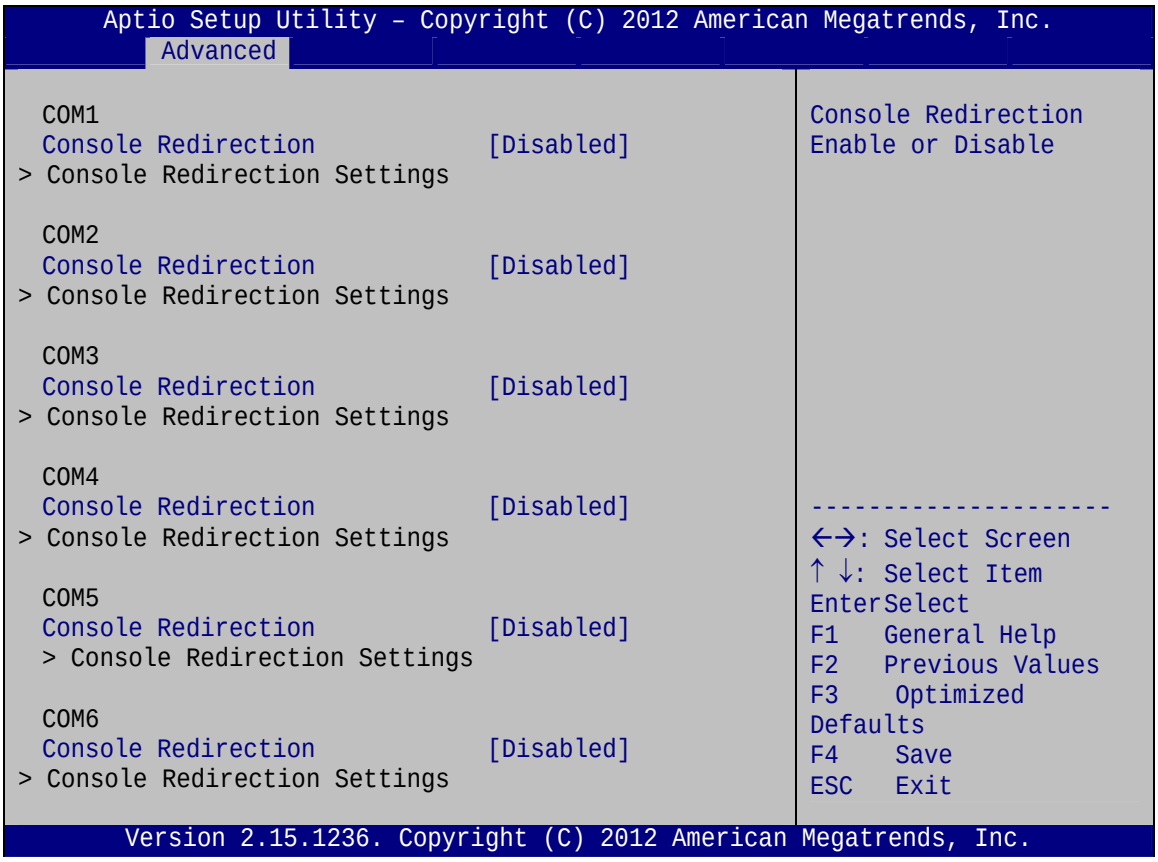
➔ **Auto Duty-Cycle Mode** **DEFAULT** The fan adjusts its speed using Auto by Duty-Cycle settings

➔ **SYS Temperature n**

Use the + or – key to change the fan **SYS Temperature n** value. Enter a decimal number between 1 and 100.

5.3.9 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 13**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 13: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

➔	**Disabled**	**DEFAULT**	Disabled the console redirection function
➔	**Enabled**		Enabled the console redirection function

5.3.9.1 Console Redirection Settings

The **Console Redirection Settings** menu (**BIOS Menu 14**) allows the console redirection options to be configured. The option is active when Console Redirection option is enabled.

```
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
        Advanced

COM1                                          Emulation: ANSI:
Console Redirection Settings                  Extended ASCII char set.
                                              VT100: ASCII char set.
Terminal Type                    [ANSI]       VT100+: Extends VT100 to
Bits per second                  [115200]     support color, function
Data Bits                        [8]          keys, etc. VT-UTF8: Uses
Parity                           [None]       UTF8 encoding to map
Stop Bits                        [1]          Unicode chars onto 1 or
                                              more bytes.

                                              ----------------------
                                              ←→: Select Screen
                                              ↑ ↓: Select Item
                                              EnterSelect
                                              F1   General Help
                                              F2   Previous Values
                                              F3    Optimized
                                              Defaults
                                              F4    Save
                                              ESC   Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.
```

BIOS Menu 14: Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔	**VT100**	The target terminal type is VT100
➔	**VT100+**	The target terminal type is VT100+

- ➔ **VT-UTF8** The target terminal type is VT-UTF8
- ➔ **ANSI** **DEFAULT** The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

- ➔ **9600** Sets the serial port transmission speed at 9600.
- ➔ **19200** Sets the serial port transmission speed at 19200.
- ➔ **38400** Sets the serial port transmission speed at 38400.
- ➔ **57600** Sets the serial port transmission speed at 57600.
- ➔ **115200** **DEFAULT** Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

- ➔ **7** Sets the data bits at 7.
- ➔ **8** **DEFAULT** Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- ➔ **None** **DEFAULT** No parity bit is sent with the data bits.
- ➔ **Even** The parity bit is 0 if the number of ones in the data bits is even.
- ➔ **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- ➔ **Mark** The parity bit is always 1. This option does not provide error detection.

➔ **Space** The parity bit is always 0. This option does not provide error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔ **1** **DEFAULT** Sets the number of stop bits at 1.

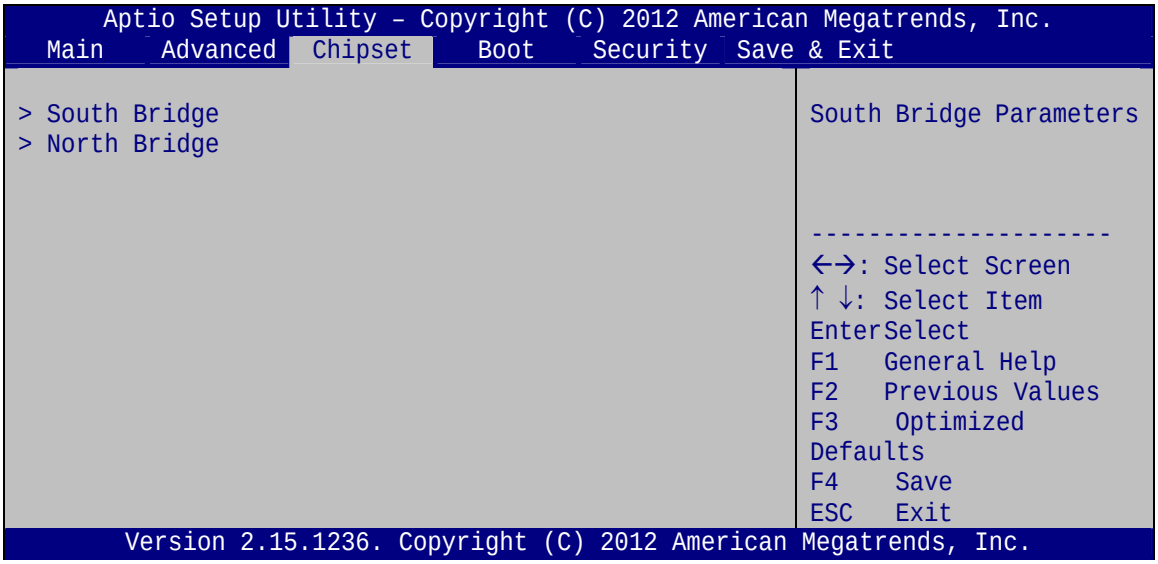
➔ **2** Sets the number of stop bits at 2.

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 15**) to access the South Bridge and North Bridge configuration menus.

WARNING!

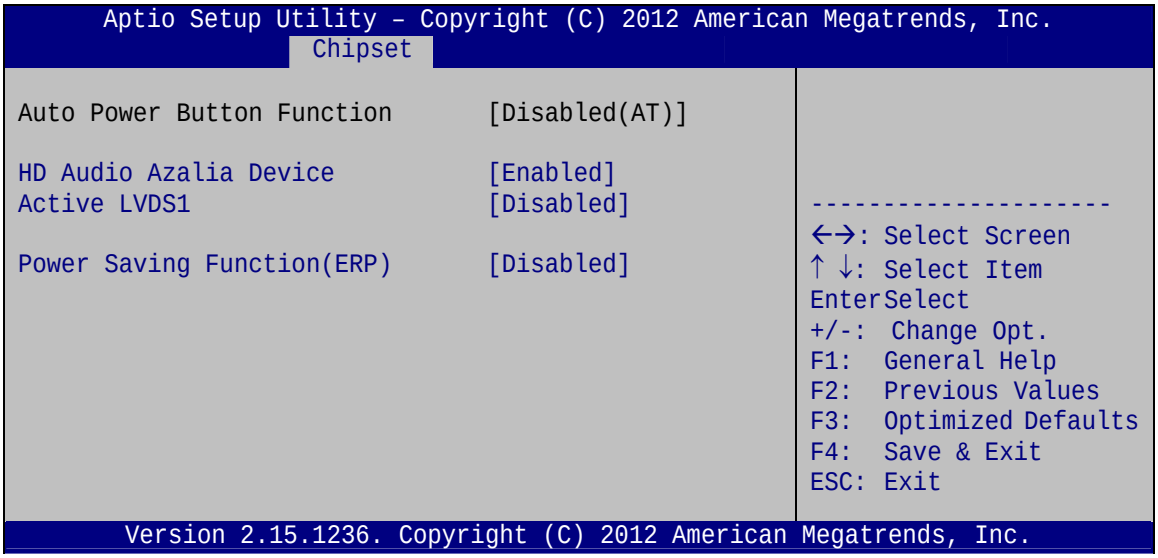
Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.



BIOS Menu 15: Chipset

5.4.1 South Bridge Configuration

Use the **South Bridge Configuration** menu (**BIOS Menu 16**) to configure the South Bridge chipset.



BIOS Menu 16: South Bridge Configuration

➔ **HD Audio Azalia Device [Enabled]**

Use the **HD Audio Azalia Device** option to enable or disable the High Definition Audio controller.

➔ **Auto**		The onboard High Definition Audio controller will be enabled if present, disabled otherwise.
➔ **Disabled**		The onboard High Definition Audio controller is disabled
➔ **Enabled**	**DEFAULT**	The onboard High Definition Audio controller is detected automatically and enabled

➔ **Active LVDS1 [Disabled]**

Use the **Active LVDS1** BIOS option to enable or disable LVDS.

➔ **Enabled**		LVDS is enabled
➔ **Disabled**	**DEFAULT**	LVDS is disabled

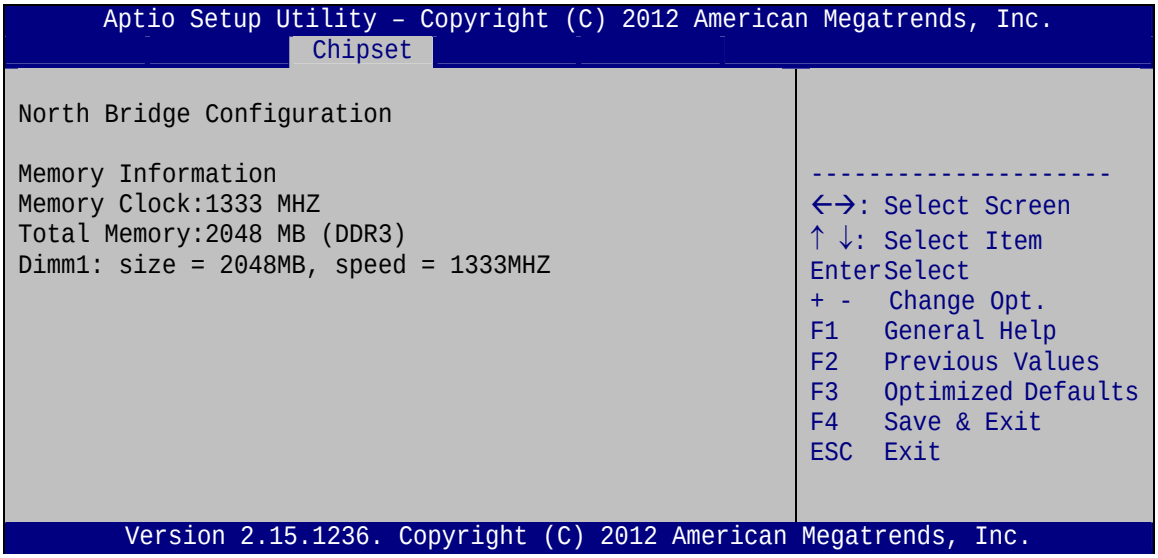
➔ **Power Saving Function (ERP) [Disabled]**

Use the **Power Saving Function (ERP)** BIOS option to enable or disable the power saving function.

➔ **Disabled**	**DEFAULT**	Power saving function is disabled.
➔ **Enabled**		Power saving function is enabled. It will reduce power consumption when the system is off.

5.4.2 North Bridge Configuration

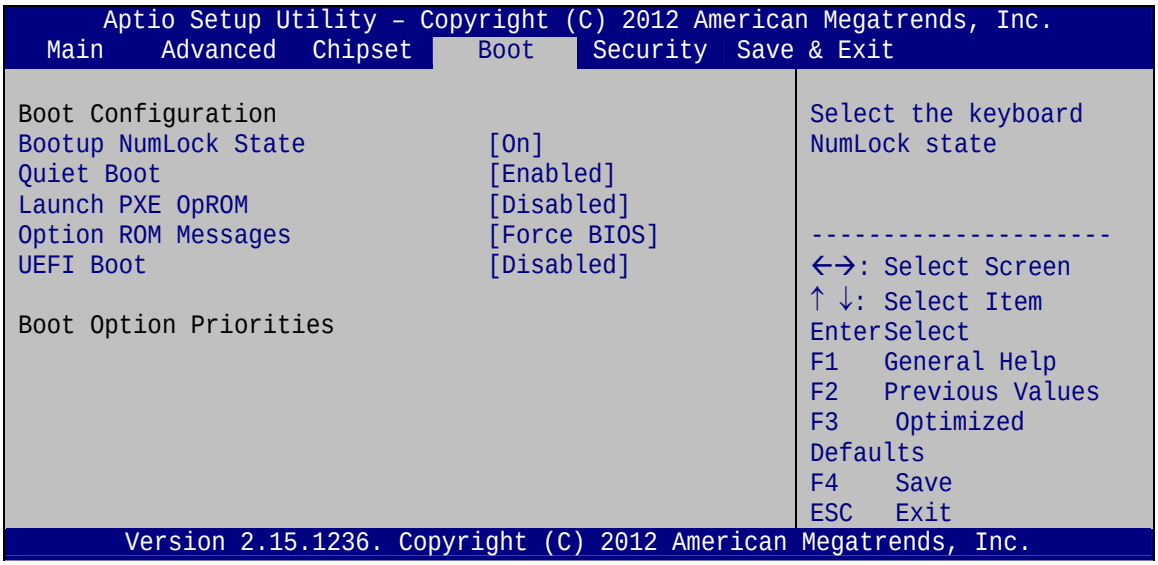
Use the **North Bridge** menu (**BIOS Menu 17**) to view the memory information.



BIOS Menu 17: North Bridge Configuration

5.5 Boot

Use the **Boot** menu (**BIOS Menu 17**) to configure system boot options.



BIOS Menu 18: Boot

➔ **Bootup NumLock State [On]**

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

➔ **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled**		Normal POST messages displayed
➔ **Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔ **Disabled**	**DEFAULT**	Ignore all PXE Option ROMs
➔ **Enabled**		Load PXE Option ROMs.

➔ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

➔ **Force BIOS**	**DEFAULT**	Sets display mode to force BIOS.
➔ **Keep Current**		Sets display mode to current.

➔ **UEFI Boot [Disabled]**

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

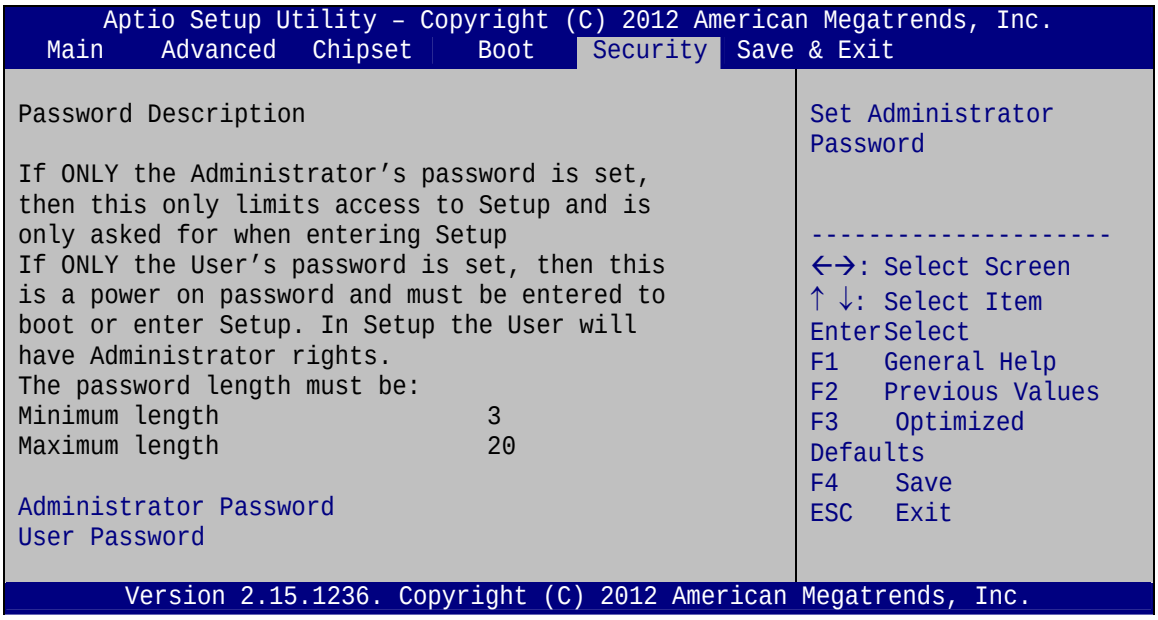
➔ **Auto**		If the first boot HDD is GPT then enable UEFI boot options, otherwise disable,
➔ **Enabled**		Boot from UEFI devices is enabled.
➔ **Disabled**	**DEFAULT**	Boot from UEFI devices is disabled.

➔ **Boot Option Priority**

Use the **Boot Option Priority** function to set the system boot sequence from the available devices. The drive sequence also depends on the boot sequence in the individual device section.

5.6 Security

Use the **Security** menu (**BIOS Menu 19**) to set system and user passwords.



BIOS Menu 19: Security

➔ **Administrator Password**

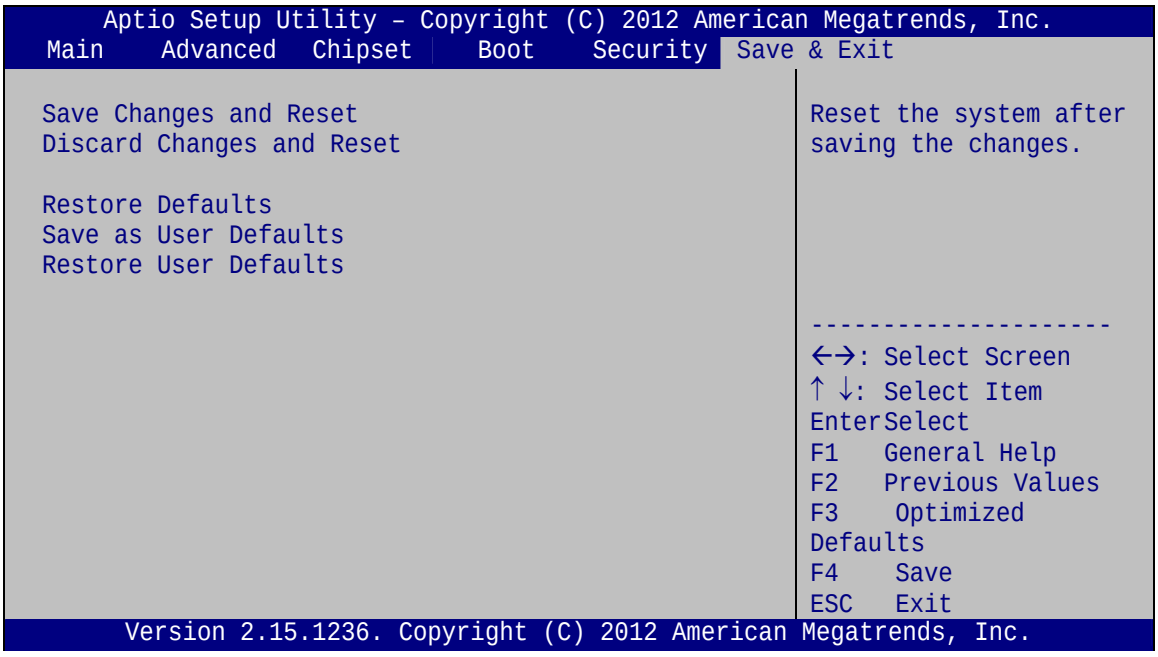
Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.7 Exit

Use the **Exit** menu (**BIOS Menu 20**) to load default BIOS values, optimal failsafe values and to save configuration changes.



BIOS Menu 20: Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and to reset the BIOS configuration setup program.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to reset the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

BIOS Menu Options

Appendix

C

Digital I/O Interface

C.1 Introduction

The DIO connector on the NANO-KBN-i1 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 4-bit digital inputs and 4-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH
Sub-function: AL – 8 :Set the digital port as INPUT AL :Digital I/O input value

C.2 Assembly Language Sample 1

```
MOV     AX, 6F08H       ;setting the digital port as input
INT     15H             ;
```

AL low byte = value

AH – 6FH
Sub-function: AL – 9 :Set the digital port as OUTPUT BL :Digital I/O input value

C.3 Assembly Language Sample 2

```
MOV     AX, 6F09H       ;setting the digital port as output
MOV     BL, 09H         ;digital value is 09H
INT     15H             ;
```

Digital Output is 1001b

Appendix

D

Terminology

AC ’97	Audio Codec 97 (AC’97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
APM	The Advanced Power Management (APM) application program interface (API) enables the inclusion of power management in the BIOS.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude (“volume”) of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is a type of integrated circuit used in chips like static RAM and microprocessors.
COM	COM is used to refer to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal

	computer is usually a male DE-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system memory.
DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
MAC	The Media Access Control (MAC) protocol enables several terminals or network nodes to communicate in a LAN, or other multipoint networks.

PCIe	PCI Express (PCIe) is a communications bus that uses dual data lines for full-duplex (two-way) serial (point-to-point) communications between the SBC components and/or expansion cards and the SBC chipsets. Each line has a 2.5 Gbps data transmission rate and a 250 MBps sustained data transfer rate.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
QVGA	Quarter Video Graphics Array (QVGA) refers to a display with a resolution of 320 x 240 pixels.
RAM	Random Access Memory (RAM) is a form of storage used in computer. RAM is volatile memory, so it loses its data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.
SATA	Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA 3Gb/s bus has data transfer speeds of up to 3.0 Gbps.
S.M.A.R.T	Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.
UART	Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.
UHCI	The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.
USB	The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates, while

	USB 2.0 supports 480Mbps data transfer rates.
VGA	The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

E

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. IEI support is contacted or the IEI website visited for specific drivers for more sophisticated operating systems, e.g., Windows and Linux.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMI or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer:

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table E-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. While the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the Watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

Example program:

```
; INITIAL TIMER PERIOD COUNTER
;
W_LOOP:

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30H             ;time-out value is 48 seconds
        INT      15H
 ;
; ADD THE APPLICATION PROGRAM HERE
;
        CMP      EXIT_AP, 1         ;is the application over?
        JNE      W_LOOP     ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT      15H
;
; EXIT ;
```

Appendix

F

Hazardous Materials Disclosure

F.1 Hazardous Material Disclosure Table for IPB Products Certified as RoHS Compliant Under 2002/95/EC Without Mercury

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated “Environmentally Friendly Use Period” (EFUP). This is an estimate of the number of years that these substances would “not leak out or undergo abrupt change.” This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
显示	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 标准规定的限量要求。