MITAC 3.5” SBC M/B PD10AS
Product Guide

Desktop Board Features

This chapter briefly describes the features of 3.5" SBC M/B PD10AS. Below to summarizes the major features of the 3.5" SBC M/B.

Feature Summary

TABLE: MITAC 3.5" SBC M/B PD10AS FEATURES

Form Factor	• 3.5" SBC (102mm x 147mm (4" x 5.8"))	
Processor Chipset	Intel Apollo Lake Processor with integrated graphics (Compatible with N3350 and N4200)	
Main Memory	• up to 8 GB of system memory	
	• 204-pin DDR3L SO-DIMM	1
Audio Controller	• Realtek ALC662 audio codec	
Expansion Capability	• PCI Express Full-Length Mini Card slot (PCIe / SATA)	1
	• M.2 (2230) with PCIe x 1 and USB 2.0 signal for wireless	1
External I/O	• USB 3.0	4
	• HDMI	1
	• VGA	1
	• RJ45	2
Internal I/O	• LVDS Connector (40Pin)	1
	• eDP Connector (40Pin)	1
	• 7-pin SATA connector	1
	• Dual-port USB 2.0 header	1
	• Chassis main panel header (2 x 5)	1
	• BIOS Clear Header / Jumper	1
	• Audio header (front panel mic / hp)	1
	• 3-pin SATA power (For DOM)	1
	• Serial Port Headers	3
	• RS-232/422/485	1
	• Jumper for AT / ATX mode	2
	• SIM Card holder	1
	• MiAPI: Programmable header	1
S I/O Controller	NCT6116D	
LAN Support	Intel I210 (10/100/1000 Mb/s) Ethernet LAN controller	
BIOS	• BIOS resident in a Serial Peripheral Interface (SPI) Flash device	
	• UEFI mode only (Does not support Legacy mode)	
	• Support for Advanced Configuration and Power Interface (ACPI), and System Management BIOS (SMBIOS)	
Hardware Management	Nuvoton NCT6116D based subsystem, including:	
	• Voltage sense to detect out of range power supply voltages	

	• Thermal sense to detect out of range thermal values
Environment	• Operating Temperature: 0°C to +70°C • Wide Operating Temperature: -40°C to +85°C (option)
	• Storage Temperature: -40°C to +85°C
Safety	• CE
	• FCC

Desktop Board Components

Figure shows the approximate location of the major components on the top side of MiTAC 3.5” SBC M/B PD10AS

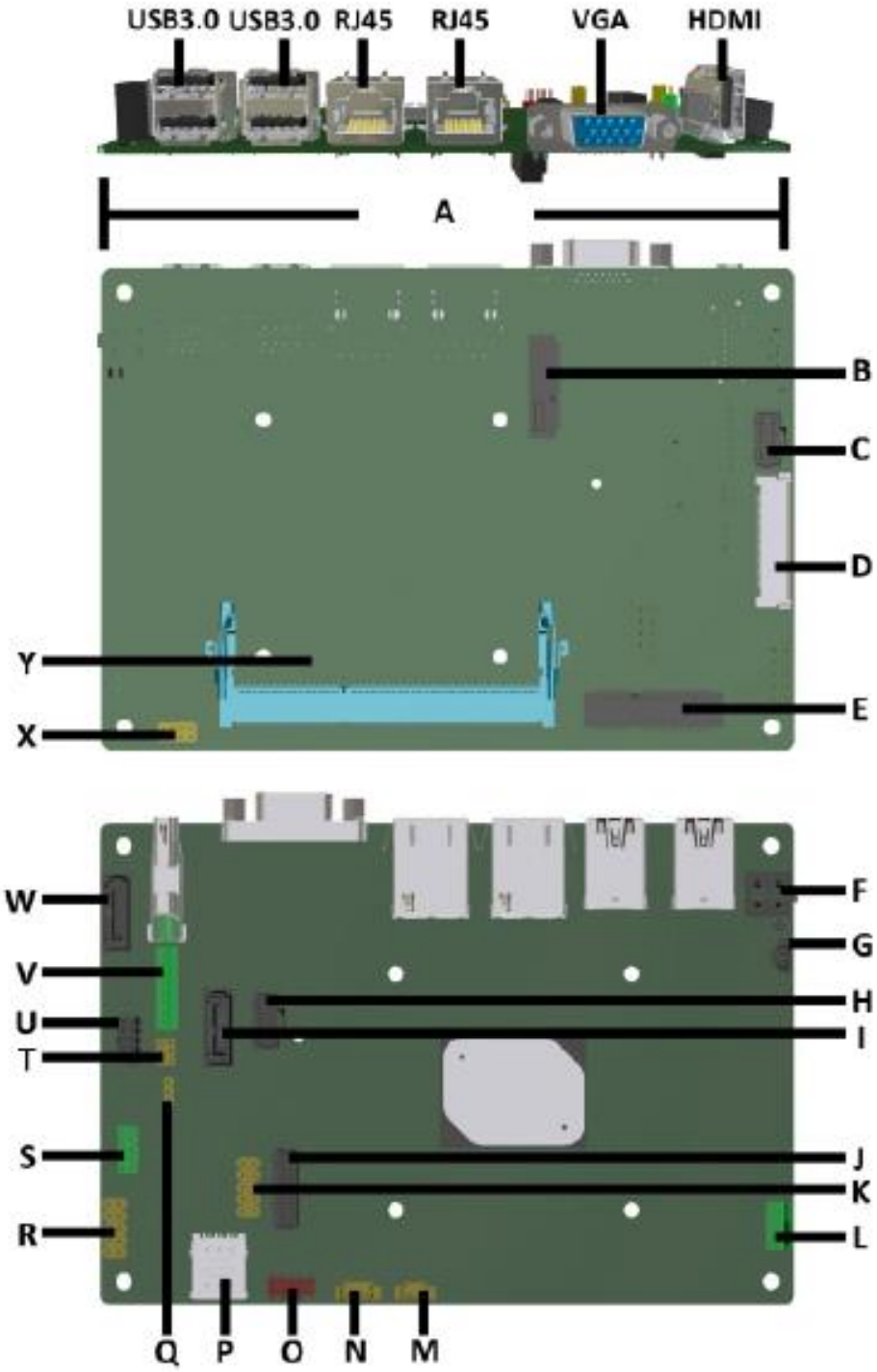


Figure: MiTAC 3.5” SBC M/B PD10AS Components (Top)

TABLE: MITAC 3.5" SBC M/B PD10AS COMPONENTS

A	**Back Panel Connectors**
B	**M.2 Key-E connector**
C	**MiAPI (SMBUS, GPIO)**
D	**eDP connector**
E	**Mini PCIE (3G module, mSATA, Wifi)**
F	**ATX PWR 4P**
G	**Battery 2P header**
H	**Dual COM1/COM3 RS232**
I	**SATA0(optional)**
J	**LVDS header**
K	**Front IO (RST#,PWT_BUT etc...)**
L	**CPU FAN**
M	**SATA 3P PWR (5V)**
N	**SATA 4P PWR (3V/5V/12V)**
O	**USB2.0 header**
P	**SIM card slot**
Q	**Backlight Inverter Voltage Selection Header**
R	**Front Audio header**
S	**COM4 RS232/RS422/RS485**
T	**Panel Voltage Selection Header**
U	**COM2 RS232_Debug Port**
V	**FPD PWR/Brightness Header**
W	**SATA1**
X	**AT/ATX, CMOS , mSATA header**
Y	LPDDR3 SO-DIMM socket

Processor

MITAC 3.5” SBC M/B PD10AS includes a passively-cooled, Intel Apollo Lake N3350/N4200 processor with integrated graphics and memory controller. The processor is soldered to the 3.5” SBC M/B and is not customer upgradeable.

NOTE

The board is designed to be passively cooled in a properly ventilated chassis. Chassis venting locations are recommended above the processor heatsink area for maximum heat dissipation effectiveness.

System Memory

NOTE

To be fully compliant with all applicable SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, you will see a notification to this effect on the screen at power up. The BIOS will attempt to configure the memory controller for normal operation.

The Desktop Board has two 204-pin DDR3L SO-DIMM sockets with gold-plated contacts. These sockets support:

- Support for DDR3L SO-DIMMs
- Serial Presence Detect (SPD) memory only
- Non-ECC memory
- Up to 8 GB of memory

HDMI feature: High-Definition Multimedia Interface (HDMI*)

- HD – HDMI1.4 flush mount graphics connector: backpanel video

- The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.
- HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.
- Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.
- The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface.

Type A Connector Pin Assignment

PIN	Signal Assignment
1	TMDS Data2+
3	TMDS Data2–
5	TMDS Data1 Shield
7	TMDS Data0+
9	TMDS Data0–
11	TMDS Clock Shield
13	CEC
15	SCL
17	DDC/CEC Ground
19	Hot Plug Detect

PIN	Signal Assignment
2	TMDS Data2 Shield
4	TMDS Data1+
6	TMDS Data1–
8	TMDS Data0 Shield
10	TMDS Clock+
12	TMDS Clock–
14	Reserved (N.C. on device)
16	SDA
18	+5V Power

VGA feature: High-Definition Multimedia Interface (HDMI*)

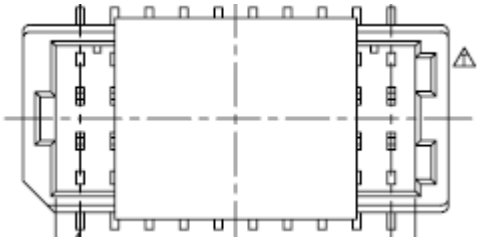
- HD – HDMI1.4 flush mount graphics connector: backpanel video

The CH7517 can support analog RGB output up to 1920x1200@60Hz or 2048x1152@60Hz with reduced blanking through triple video DACs, and the DAC supports pixel rate up to 200MHz. The de-serialized data from the DisplayPort Receiver, after proper decoding and image enhancement process, are transported to the video DACs. This operating mode uses 8-bits of the DAC's 9-bit range, and provides a nominal signal swing of 0.7V(depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied.

1.1.1 LVDS panel pin Header –

TF-CON;LVDS,SBU,INTEL,15Pin*2,1.0mm,MA,ST,Gold Flash,WHITE (ACES ELECTRONIC: 87216-3016-06)

LVDS feature:



No	Symbol	Description	No	Symbol	Symbol
1	FR0M	Minus signal of odd channel 0 (LVDS)	2	SR0M	Minus signal of odd channel 0 (LVDS)
3	FR0P	Plus signal of odd channel 0 (LVDS)	4	SR0P	Plus signal of odd channel 0 (LVDS)
5	FR1M	Minus signal of odd channel 1 (LVDS)	6	SR1M	Minus signal of odd channel 1 (LVDS)
7	FR1P	Plus signal of odd channel 1 (LVDS)	8	SR1P	Plus signal of odd channel 1 (LVDS)
9	FR2M	Minus signal of odd channel 2 (LVDS)	10	GND	Ground
11	FR2P	Plus signal of odd channel 2 (LVDS)	12	SR2M	Minus signal of odd channel 2 (LVDS)
13	GND	Ground	14	SR2P	Plus signal of odd channel 2 (LVDS)
15	FCLKINM	Minus signal of odd clock channel (LVDS)	16	SCLKINM	Minus signal of odd clock channel (LVDS)
17	FCLKINP	Plus signal of odd clock channel (LVDS)	18	SCLKINP	Plus signal of odd clock channel (LVDS)
19	FR3M	Minus signal of odd channel 3 (LVDS)	20	SR3M	Minus signal of odd channel 3 (LVDS)
21	FR3P	Plus signal of odd channel 3 (LVDS)	22	SR3P	Plus signal of odd channel 3 (LVDS)
23	GND	Ground	24	GND	Ground
25	NC	NC	26	NC	NC
27	VLCD	Power Supply +12.0V	28	VLCD	Power Supply +12.0V
29	VLCD	Power Supply +12.0V	30	VLCD	Power Supply +12.0V

Table 1: LVDS 15Px2 panel main header signals

1.1.2 eDP panel pin Header

TF-CON;LVDS,SBU,40Pin,0.5mm,FM,R/A,Gold Flash,BLACK (ACES ELECTRONIC: 50203-04001-001)

eDP feature:

Additional requirements for eDP panel interface:

40-pin eDP connector must be right-angled, single-row shrouded colored black, as shown in Figure 2 (part number reference: ACES 50203-04001-001). Connector must support four lanes of eDP traffic, AUX channel, panel logic power as well as backlight power and control signals, compliant with the VESA Embedded DisplayPort™ (eDP™) Standard for 40-pin eDP pin assignment, Connector must be located on the backside of the board, preferably under the LVDS connector.

Figure 2: Panel 40-pin eDP connector

Pin	Signal
1	NC_Reserved
2	High-speed_GND
3	Lane3_N (DDPD_[3]N)
4	Lane3_P (DDPD_[3]P)
5	High-speed_GND
6	Lane2_N (DDPD_[2]N)
7	Lane2_P (DDPD_[2]P)
8	High-speed_GND
9	Lane1_N (DDPD_[1]N)
10	Lane1_P (DDPD_[1]P)
11	High-speed_GND
12	Lane0_N (DDPD_[0]N)
13	Lane0_P (DDPD_[0]P)
14	High-speed_GND
15	AUX_CH_P (DDPD_AUXP)
16	AUX_CH_N (DDPD_AUXN)
17	High-speed_GND
18	LCD_VCC
19	LCD_VCC
20	LCD_VCC

Pin	Signal
21	LCD_VCC
22	LCD_Self_Test-or-NC
23	LCD_GND
24	LCD_GND
25	LCD_GND
26	LCD_GND
27	HPD (DDPD_HPD)
28	BKLT_GND
29	BKLT_GND
30	BKLT_GND
31	BKLT_GND
32	BKLT_ENABLE
33	BKLT_PWM_DIM
34	NC_Reserved
35	NC_Reserved
36	BKLT_PWR
37	BKLT_PWR
38	BKLT_PWR
39	BKLT_PWR
40	NC_Reserved

Table 2: 40-pin eDP connector pin-out

• Interface must be fully validated with WUXGA/1920x1200@60Hz 24bpp eDP panel connected by 2-lane link at 2.7Gbps as well as four-lane link at 1.62Gbps.

eDP connector must be validated to support maximum current rating for LCD panel power at 3.3V, 5V and 12V as well as for backlight inverter power at 5V and 12V.

• Output voltage for LCD panel at eDP connector pins 18-21 must be selectable between 3.3V (default), 5V and 12V by a 2x3, 2.54mm pitch header capable of 3A per pin and colored red with black jumper, as defined in Figure 4 and Table 3.

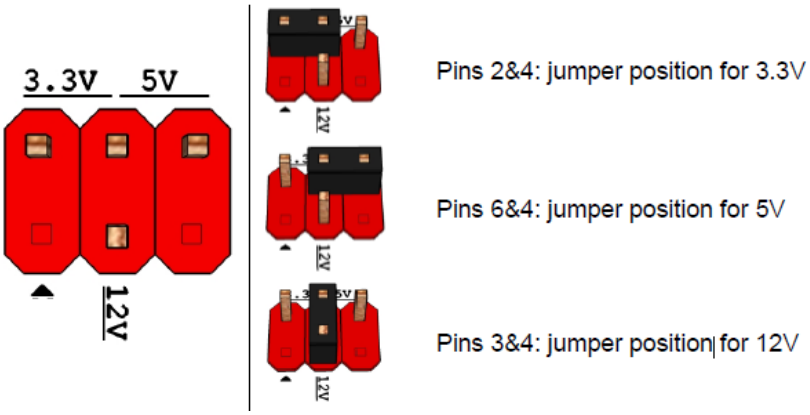


Figure 3: Panel LCD voltage selection header

Pin	Signal	Description
1	Key	No pin
2	3.3V	3.3V option
3	12V	12V option
4	LCD_VCC	Send voltage to connector
5	Key	No pin
6	5V	5V option (default)

Table 3-1: Panel LCD voltage selection header pin-out (R0C)

Pin	Signal	Description
1	Key	No pin
2	3.3V	3.3V option (default)
3	12V	12V option
4	LCD_VCC	Send voltage to connector
5	Key	No pin
6	5V	5V option

Table 3-2: Panel LCD voltage selection header pin-out (R01)

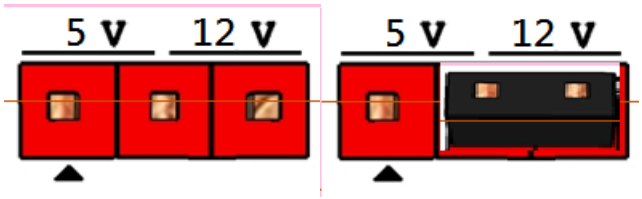


Figure 4: Backlight inverter voltage selection header

Pin	Signal	Description
1	5V	5V option
2	BKLT_PWR	BKLT_PWR
3	12V	12V option (default)

Table 4: Backlight inverter voltage selection header pin-out

Shared requirements for LVDS and eDP interfaces:

Board must provide separate backlight inverter connectivity via an “FPD Brightness” connector. 8-pin FPD brightness connector must be 1x8 shrouded, 2.00mm pitch with 2A rating per pin and colored red, as shown in Figure 5 (part number reference: Foxconn HF5508). Connector must provide backlight inverter control signals (same as routed to LVDS and eDP connectors, for customer convenience) as well as panel brightness control signals, as defined in Table 5.

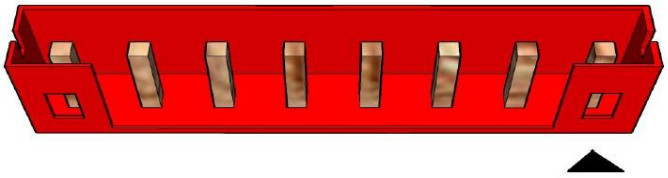


Figure 5: 8-pin FPD power connector

Pin	Signal	Description
1	BKLT_EN	Backlight enable
2	BKLT_PWM	Backlight control
3	BKLT_PWR	Backlight inverter power
4	BKLT_PWR	Backlight inverter power
5	BKLT_GND/Brightness_GND	Ground (shared)
6	BKLT_GND/Brightness_GND	Ground (shared)
7	Brightness_Up	Panel brightness increase
8	Brightness_Down	Panel brightness decrease

Table 5: 8-pin FPD power connector pin-out

- Brightness control signals must be GPIO inputs; specific GPIO addresses must be determined by ODM.

- Backlight brightness must be dynamically controlled via discrete panel brightness buttons (on the front panel bezel) enabling tactile interface for end-user screen brightness adjustments.

8-pin FPD power connector must be validated to support maximum power delivery at all voltage levels, as well

as to correctly support backlight control signals.

An assortment of LVDS and eDP panels with CCFL and LED backlights must be used for validating backlight power and control features.

eDP and LVDS functionality must be multiplexed by BIOS setting at boot time.

1.1.3 Audio

Implemented using the nuvoTon NAU88L25YGB

Board must support 3-channel audio output from the rear analog ports, with jack detection as indicated. An additional 2-channel analog port is required for front panel audio, with jack detection and independent multi-streaming support for separate front vs back panel audio streams (i.e. simultaneous VoIP and 8.1/10 audio streams).

Front panel audio header must be 2x5, 2.54mm pitch, colored yellow (Pantone color code 123C) and keyed at pin 8, as shown in Figure .

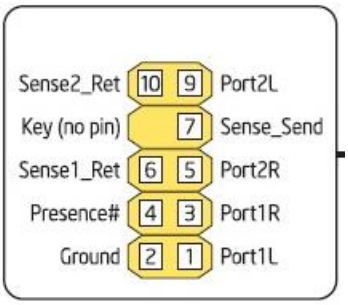
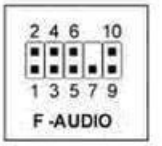


Figure 6: HD Front panel audio header

High Definition Audio



Pin	Pin Assignment	Pin	Pin Assignment
1	MIC2 L (Microphone 2 Left)	2	AGND (Analog Ground)
3	MIC2 R (Microphone 2 Right)	4	AVCC (Analog VCC Power)
5	FRO-R (Front Right)	6	MIC2_JD (Microphone 2 Jack Detect)
7	F_IO_SEN (Front I/O Sensor)		
9	FRO-L (Front Left)	10	LINE2_JD (Line 2 Jack Detect)

Table 6: HD headphone/mic front panel audio port pin assignments

1.1.4 2ea LAN port

Board must implement a LAN solution supporting 10/100/1000 Mb/s with the following features:

Onboard RJ45 connectors must have integrated magnetics and support dual status LEDs per port, as shown in Table 2.

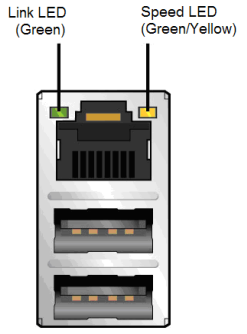
Diagram	LED	Color	State	Condition
	Link	N/A	Off	LAN link is not established
		Green	On	LAN link is established
			Blinking	LAN activity occurring
	Speed	N/A	Off	10 Mb/s data rate
		Green	On	100 Mb/s data rate
		Yellow	On	1000 Mb/s data rate

Table 7: RJ45 LED behavior

Note: LAN subsystem must be tested for IEEE802.3 conformance on each port.

1.1.5 SATA

SATA PORT0: This is optional port from mini PCI-E and SATA0 Connector

Board must also support the following Serial ATA Gen 3 compliant ports

- One fully-shrouded right angle internal SATA gen 3 ports (colored GREY)

SATA PORT1

Board must also support the following Serial ATA Gen 3 compliant

- one fully-shrouded right angle internal SATA gen 3 ports (colored BLACK)
-

Note: All SATA must be compliant with the Serial ATA Revision 3.0 Specification, as noted in the Reference Documentation section.

1.1.6 Super I/O

Board must support the following features through a SuperIO controller device:

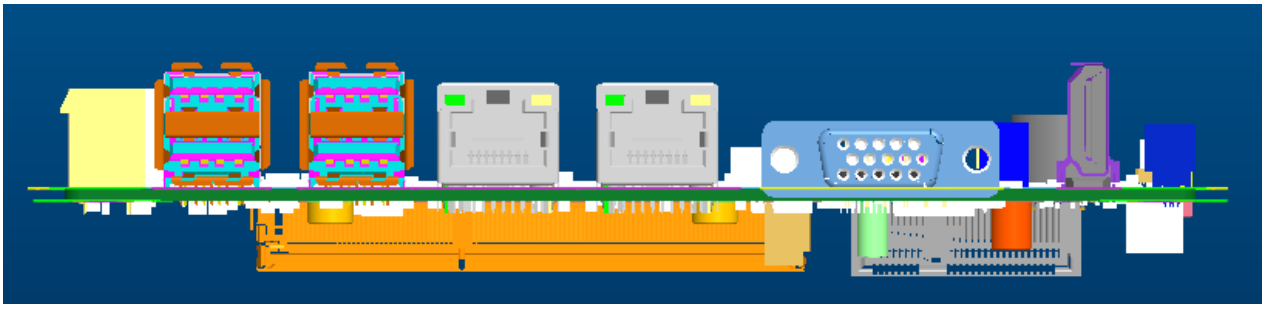
- SMBUS/SMLink support for SOC temp
- Support for as one fan headers as required in section 1.4.2 - Fan Header Requirements
- Support minimum of 2 temperature inputs per PWM Controller for duty cycle determination
- Support for non-ACPI based fan control (thermal responsiveness independent of system software)
- Support 4ea serial port: 3ea RS232, 1ea RS485/RS422/RS232
- Legacy I/O (for applicable ports)

1.2 Expansion I/O

1.2.1 Back Panel I/O

Backpanel must be designed with horizontal keepout space between ports exceeding specifications for ease of cable connectivity/removal. A minimum of 2 mm between cable connectors is required when all ports are being used with commonly available "off-the-shelf" cables.

Board must have a back panel layout similar to Figure , 5:



USB3 USB3	USB3 USB3	LAN1 (PCIE P1)	LAN2 (PCIE P3)	VGA	HDMI

Figure 7: Back panel layout

1.2.2 USB

Board must support the following Universal Serial Bus ports:

Port Summary

- 2 total USB2.0 Ports (2 internal)
- 1 total USB2.0 Ports (m2 key-E Connector)
- 1 total USB2.0 Ports (Mini PCIE Connector)
- 4 total USB 3.0 Ports (2 back-panel with standard USB3.0 I/O port)

Front panel USB2.0 headers must be 2x5, 2.0mm pitch, colored black and keyed at pin 9, as defined in Figure and Table . Follow the Intel Front Panel I/O Connectivity Design Guide for front panel USB solutions.

(SUPERIOR TECH : PHDD-SS010G1ABONE-N088)

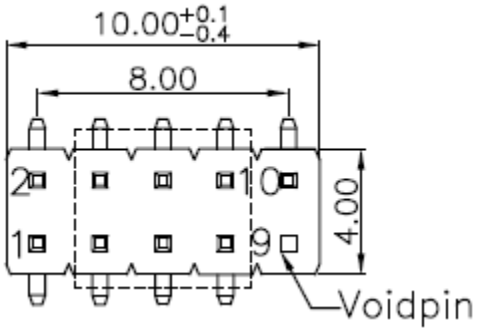


Figure 8: Front panel USB header pin-out

Pin	Signal	Pin	Signal
1	+5V DC	2	+5V DC
3	Data (negative)	4	Data (negative)
5	Data (positive)	6	Data (positive)
7	Ground	8	Ground
9	Key (no pin)	10	No Connect

Table 8: Front panel USB header signals

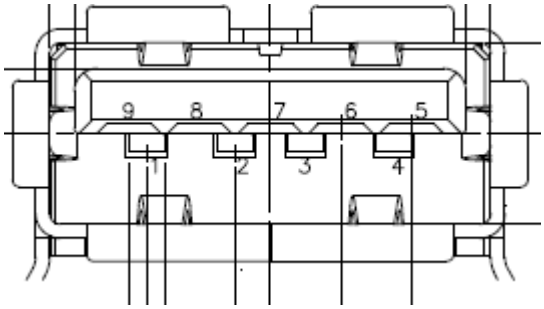
Notes: Front panel USB headers must be placed within a keep-out-zone no smaller than 1 inch (half-inch to the left and half-inch to the right of the header) so as to support commonly available USB connectors.

Thermistor protection is required for all back panel and front panel USB ports.

ESD protection is required for all D+ and D- signals. Signal routing/layout for all front panel and backpanel ports must include pads for ESD protection; protection components must be stuffed. ESD protection circuitry must meet respective signal qualification, functionality and performance.

Common mode choke footprint must be routed for all back panel and front panel USB ports (to be stuffed on back panel ports shall EMI test fail with less than 4dB margin).

Rear USB3.0 I/O port



USB 3.0 Standard-A Connector Pin Assignments

Pin Number	Signal Name	Description	Mating Sequence
1	VBUS	Power	Second
2	D-	USB 2.0 differential pair	Third
3	D+		
4	GND	Ground for power return	Second
5	StdA_SSRX-	SuperSpeed receiver differential pair	Last
6	StdA_SSRX+		
7	GND_DRAIN	Ground for signal return	
8	StdA_SSTX-	SuperSpeed transmitter differential pair	
9	StdA_SSTX+		
Shell	Shield	Connector metal shell	First

Note: Tx and Rx are defined from the host perspective

Table 9: Rear USB3.0 I/O signals

1.2.3 SPI Programing Header – None

1.2.4 PCI Express Expansion Slots

Board's PCI Express slot(s) must be PCI Express Specification v2.0 compliant and compatible with PCI Express v2.0 and v1.1 add-in cards.

PCI Express x16 slot must be compatible with x16/x8/x4/x1 PCI Express add-on cards. PCIe x16 slot's retention mechanism must be consistent across Intel desktop boards.

PCI Express x4 slot(s) must be compatible with PCI Express x4 and x1 add-on cards. Slot power capability must comply with 25W requirement as defined in the PCI Express Card Electromechanical 3.0 Specification.

PCI Express x1 slot(s) must be compatible with x1 PCI Express add-on cards.

Route WAKE# to support ACPI wake events.

Design must provide SMBus routed to all PCI Express slots, with individual/per slot de-stuffing option via strapping resistor (strapping resistor must be stuffed by default).

Follow the ATX specification and Industrial DFA (Design for Assembly) standard requirements for connector placement and spacing.

Keep-out zone of PCI Express v3.0 x16 slot must allow use of double-width and long graphics cards without blocking access to any connectors (i.e. SATA ports, DIMM connector tabs, front panel audio header, …).

1.2.5 Expansion Slot Layout

Board must have the following expansion slot layout:

Slot Configuration	Electrical	Physical Connector	Color
J43	M.2 key M socket	M.2 Key E socket	Black
J25	PCI Express 3.0 x1	Mini PCIE	Black

- **M.2 Suport key-E 3 Type2230 for WLAN/USB2.0 feature**
- **Mini PCIE for mSATA feature support SATA SSD or PCIE SSD module**

1.3 Additional Headers

1.3.1 Front Panel

The front panel main header must be shrouded 2x5, 2.54mm pitch, multi-colored, keyed at pin 10 and with silkscreen text as defined in Figure 8 and Table 4. Polarity markings on pins 1 & 2 and color-coding on all pins are required. Refer to Intel PN 2100C888-121 and other Intel® Desktop Boards for front panel header connectivity references.

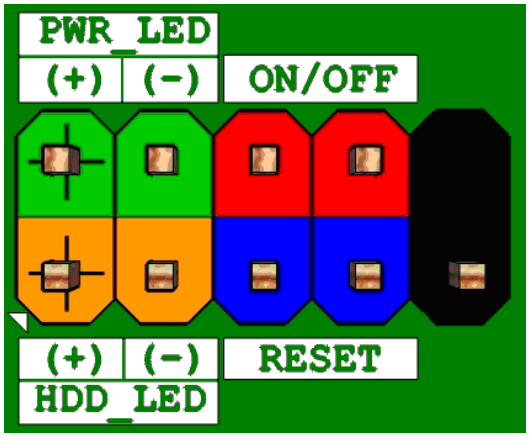


Figure 9: Front panel main header pin-out

Pin	Signal Name	Description	Pin	Signal Name	Description
1	HDD_POWER_LED	Pull-up resistor (750Ω) to +5V	2	POWER_LED_MAIN	[Out] Front panel LED (main color)
3	HDD_LED#	[Out] Hard disk activity LED	4	POWER_LED_ALT	[Out] Front panel LED (alt color)
5	GROUND	Ground	6	POWER_SWITCH#	[In] Power switch
7	RESET_SWITCH#	[In] Reset switch	8	GROUND	Ground
9	+5V_DC	Power	10	KEY	No pin

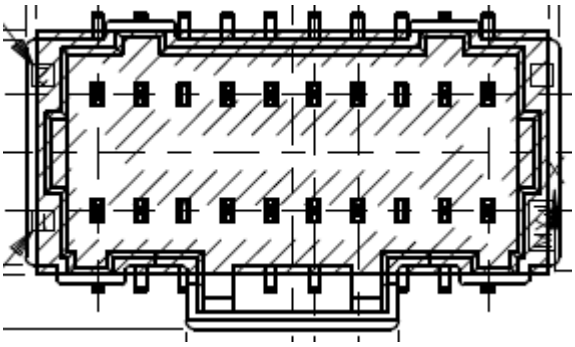
Table 10: Front panel main header signals

1.3.2 Chassis Intrusion Detection-NONe

1.3.3 MiAPI feature

The MiAPI port header must be 2x10, 1.mm pitch, colored black and keyed at pin 20

Dual COM port header: Molex 5011902017_sd



Pin	Signal Name	Pin	Signal Name
1	MAPI_GPIO1	2	VCC
3	MAPI_GPIO2	4	MAPI_GPIO6
5	MAPI_GPIO3	6	MAPI_GPIO7
7	MAPI_GPIO4	8	MAPI_GPIO8
9	MAPI_GPIO5	10	MAPI_GPIO9
11	Watchdog Timer	12	MAPI_GPIO10
13	Power Button	14	SMB_MAIN_DATA
15	UART_TX	16	SMB_MAIN_CLK
17	UART_RX	18	5VSB

	19	GND	20	N/C

Table 11: MiAPI header signals

1.3.4 Serial Port

The serial port header must be 2x5, 2.00mm pitch, colored green and keyed at pin 10, as defined in Figure 10

Table 13: RS232/RS422/RS485 Serial port header signals

Internal I/O header: Standard 9 pin RS232 or RS485, RS422 port

COM port 2 header : J_RS232_P2 is RS232 feature only

(SUPERIOR TECH : PHDD-SS010G1AGONX-N092)

COM port 4 header: RS485/RS422/RS232 feature

(SUPERIOR TECH : PHDD-SS010G1ABONE-N092)

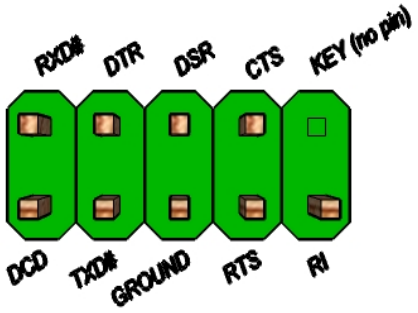
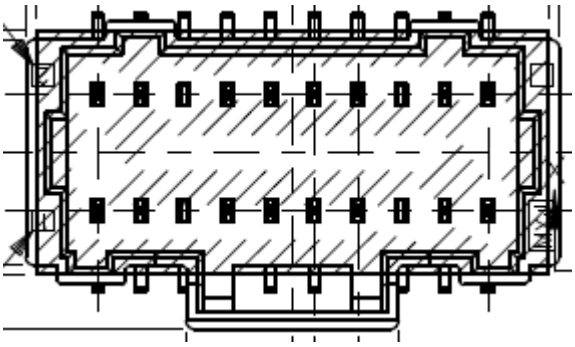


Figure 10: RS232, RS485, RS232 Serial port header pin-out

Internal I/O header: 10Px2, 1.0mm, ST: dual RS232 port

Dual COM port header: Molex 5011902017_sd



COM port #1,#3 header: RS485/RS422/RS232 feature

Serial Port #1, #3: RS232_P1P3 pin defintion

	Signal	Pin	Signal
	RS232		**RS232**
1	DCD (Data Carrier Detect)	2	RXD# (Receive Data)
3	TXD# (Transmit Data)	4	DTR (Data Terminal Ready)
5	Ground	6	DSR (Data Set Ready)
7	RTS (Request To Send)	8	CTS (Clear To Send)
9	RI (Ring Indicator)	10	NC
11	DCD (Data Carrier Detect)	12	RXD# (Receive Data)
13	TXD# (Transmit Data)	14	DTR (Data Terminal Ready)
15	Ground	16	DSR (Data Set Ready)
17	RTS (Request To Send)	18	CTS (Clear To Send)
19	RI (Ring Indicator)	20	NC

Table 14: Dual Serial port header signals

1.3.5 AT/ATX, CMOS , mSATA header in silkscreen / feature

JUMPER	J_AT_CMOS1
(1-2)	Clear CMOS
(1-3)	Normal
(4-6)	ATX
(8-6)	AT
(5-7)	PCIE
(5-7) NA	mSATA

JUMPER	(1-2)	(1-3)
Clear CMOS	Clear CMOS	Normal

CMOS clear
Normal: 1-3
Clear CMOS: 1-2

JUMPER	(8-6)	(4-6)
AT/ATX	AT Mode	ATX (Default)

mSATA detection function:

Base on some PCIE/USB 3G module pin51 suport PCM_SYNC
Base on old SATA module pin43 can't meet datasheet NC pin

JUMPER	(5-7) IN	(5-7) NA
mSATA/PCIE	PCIE 3G Module (Default)	mSATA

1.3.6 SATA power 1.25mm cable pin header

Support SATADOM power current is 1A max at V_5P power rail

Support external 5V SATA power with 1A max current.

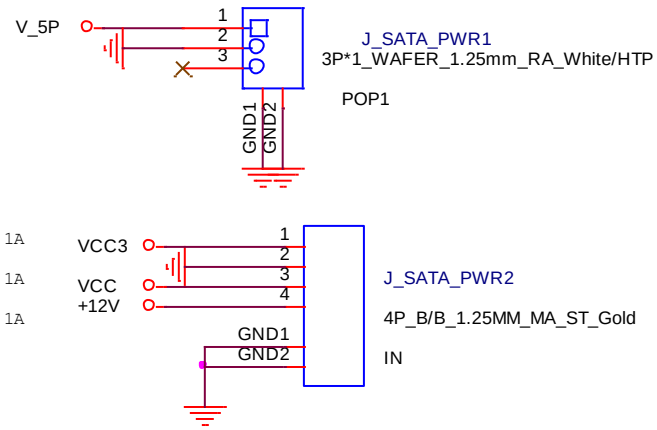
Support external 12V SATA power with 1A max current.

Support external VCC3 SATA power with 1A max current.

Pin	signal
1	5V
2	GND
3	NC

Pin	signal
1	VCC3
2	GND
3	VCC
4	+12V

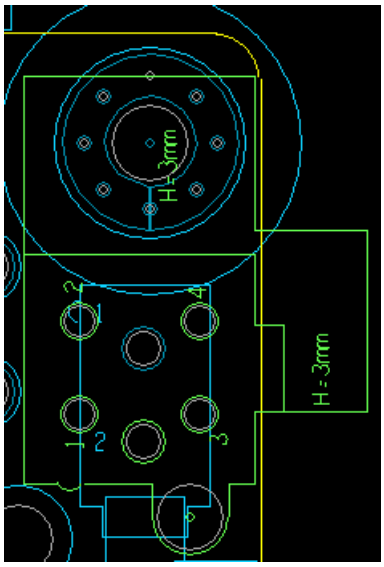
Table 15: SATA power 1.25mm cable pin header signals

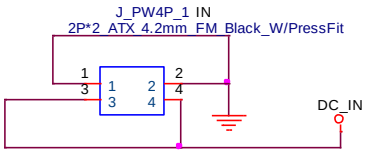


Connector:
TF-CON;SBU,B/B,3P,1.25MM,MA,ST,GOLD,1A,SMT
ACES ELECTRONIC CO.,LTD 85205-03701

TF-CON;SBU,B/B,4P,1.25MM,MA,ST,GOLD,1A,SMT
ACES ELECTRONIC CO.,LTD 85205-04701

1.3.7 ATX power 4P/DC power 4.2mm pin header





Pin	signal
1	GND
2	GND

3	Power 8V~24V
4	Power 8V~24V

Connector part 2Px2, 4.2mm, ST
LOTES CHIA TSE TERMINAL INDUST ABA-POW-003-K78

1.4 Thermal Management and Fan Control

- Nuvoton NCT6104D SuperIO: backup alternate solution as it leverages existing hardware in the designs, but software infrastructure must be put in place to support this solution.

Regardless of solution chosen, BIOS/driver/tools support and subsystem validation is required, even if solution is not needed by pilot.

Board must use SuperIO solution for hardware monitoring and thermal management. SuperIO implementation must be supported by BIOS, tools and drivers necessary for custom thermal profile management no later than by fab B samples.

BIOS/tools/driver support and subsystem validation is required.

The thermal management capability must support temperature sensors near CPU VR FETs as well as near or on the memory components; shall only one temperature sensor be feasible it must be located near the CPU VR FETs.

The following thermal management features must be supported:

- Temperature monitoring at the following locations:
  - remote diode near CPU VR FETs
  - remote diode near or on the memory components
- Voltage monitoring (in priority order): +12V, V_SM, CPU VCC_VCGI, CPU VNN_SVID

1.4.1 CPU Fans

Board must implement a 4-pin fan header for the processor/heatsink 4-wire fan. Processor/heatsink fan must be tachometer/PWM controlled and header color must be white, as shown in Figure 3.

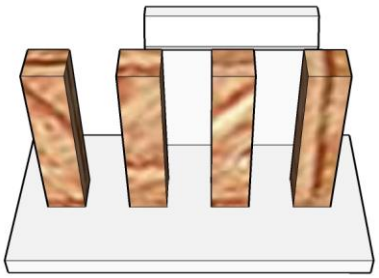
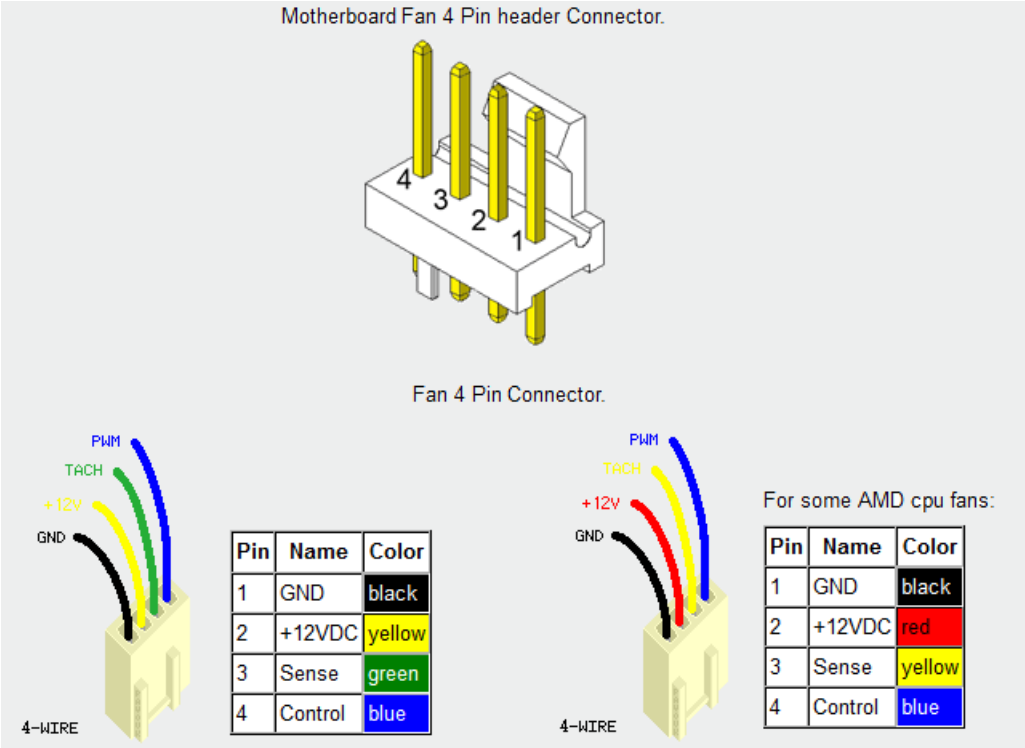


Figure 11: Processor fan header



1.4.2 Fan Header Requirements

The below requirements must be met for the 4-pin processor/heatsink fan (CPU FAN) header:

- Closed loop fan speed control via the FANPWM0 signal routed to pin-4
- Route fan tachometer signal to FANTACH0 input
- Support 2A continuous draw
- Clearly label as “CPU FAN”
- Locate closest to the CPU as required by the CDPG boxed CPU

MITAC Desktop Board PD10AI
BIOS Specifiction

1. **MAIN PAGE**

Main	Advanced	Chipset	Security	Boot	Save & Exit	
BIOS Information						**Item help**
BIOS Version		D7740X01				
Build Date		02/02/2017				
Processor Information						
Genuine Intel® CPU @ 1.50GHz						
						→←: Select Screen
SATA Devices						↑↓: Select Item
SATA Port0						Enter: Select
[Not Installed]						+/- : Change Opt
SATA Port1						F1: General Help
[Not Installed]						F2: Previous Values
						F3: Optimized Defaults
Memory Information						F4: Save & Reset
Total Memory		8192 MB				ESC: Exit
Memory speed		1600MHz				
System Date		[Mon, mm/dd/yyyy]				
System Time		[hh:mm:ss]				
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.						

Field Name	BIOS Version
Default Value	Display the version of the BIOS
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Build Date
Default Value	Display build time of the BIOS
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Processor Information
Value	Display the installed CPU brand.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	SATA Port 0
Value	Display the installed SATA port 0 devices.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	SATA Port 1
Value	Display the installed SATA port 0 devices.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Total Memory
Value	Display the installed memory size.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Memory Speed
Default Value	Display the installed memory speed
Comment	This field is not selectable. There is no help text associated with it.

Field Name	System Date
Default Value	[xxx, mm dd yyyy]
Possible Value	[xxx, xx:xx:xxxx]
Help	Set the Date. Use Tab to switch between Date elements. Default Ranges: Year: 2005-2099 Months: 1-12 Days: dependent on month

Field Name	System Time
Default Value	[hh :mm :ss]
Possible Value	[xx :xx :xx]
Help	Set the Time. Use Tab to switch between Time elements.

2. ADVANCED PAGE

Main	Advanced	Chipset	Security	Boot	Save & Exit	
LAN1				[Enable]		**Item help**
LAN2				[Enable]		
Mini PCIe				[Enable]		
M.2				[Enable]		
▶Intel(R) I210 Gigabit Network Connection – 00:22:4D:4D:...						
▶Intel(R) I210 Gigabit Network Connection – 00:22:4D:4D:...						
▶Driver Health						
▶Trusted Computing						
▶SMART settings						
▶NCT6116D Super IO Configuration						
▶S5 RTC Wake Settings						
▶CPU Configuration						**→←: Select Screen**
▶Network Stack Configuration						**↑↓: Select Item**
▶Platform Trust Technology						**Enter: Select**
						+/- : Change Opt
						F1: General Help
						F2: Previous Values
						F3: Optimized Defaults
						F4: Save & Reset
						ESC: Exit

Field Name	**LAN1**
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enable/Disable LAN Device

Field Name	**LAN2**
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enable/Disable LAN Device

Field Name	**Mini PCIe**
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enable/Disable mini PCIE

Field Name	**M.2**

Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enable/Disable M.2

Field Name	**Intel(R) I210 Gigabit Network Connection – 00:22:4D:4D:00:01**
Help	Configure Gigabit Ethernet device parameters
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Intel(R) I210 Gigabit Network Connection – 00:22:4D:4D:00:02**
Help	Configure Gigabit Ethernet device parameters
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Driver Health**
Help	Provides Health Status for the Drivers/Controllers
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Trusted Computing**
Help	Trusted Computing settings
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**SMART Settings**
Help	System SMART settings.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**NCT6104D Super IO Configuration**
Help	System Super IO Chip Parameters.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**S5 RTC Wake Settings**
Help	Enable system to wake from S5 using RTC alarm
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**CPU Configuration**
Help	CPU Configuration Parameters.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Network Stack Configuration**
Help	Network stack Settings.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Platform Trust Technology**
Help	Platform Trust Technology
Comment	Press Enter when selected to go into the associated Sub-Menu.

2.1 INTEL(R) I210 GIGABIT NETWORK CONNECTION – 00:22:4D:4D:00:01

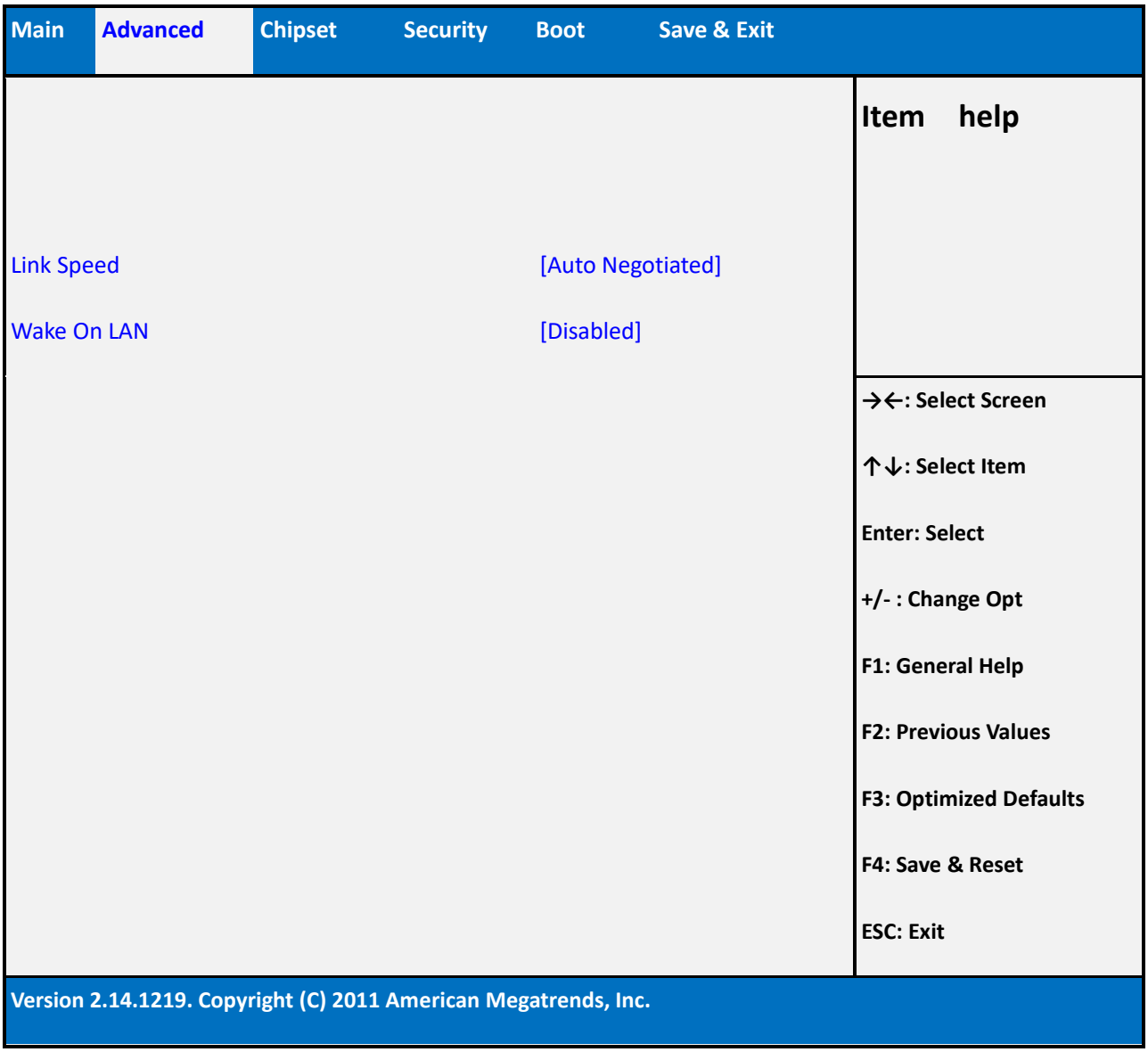
Main	Advanced	Chipset	Security	Boot	Save & Exit	
▶NIC Configuration						**Item help**
Blink LEDs			0			
UEFI Driver			Inter(R) PRO/1000 7.3…			
Adapter PBA			000300-000			
Device Name			Intel(R) I210 Gigabit…			
Chip Type			Intel i210			**→←: Select Screen**
PCI Device ID			1533			**↑↓: Select Item**
PCI Address			01:00:00			**Enter: Select**
						+/- : Change Opt
Link Status			[Disconnected]			**F1: General Help**
						F2: Previous Values
MAC Address			00:22:4D:4D:00:01			**F3: Optimized Defaults**
Virtual MAC Address			00:00:00:00:00:00			**F4: Save & Reset**
						ESC: Exit
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.						

Field Name	**NIC Configuration**
Help	Click to configure the network device port.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Blink LEDs**

Default Value	0
Possible Value	0-15
Help	Identify the physical network port by blinking the associated LED.

2.3.1 NIC CONFIGURATION



Field Name	**Link Speed**
Default Value	Auto Negotiated
Possible Value	Auto Negotiated 10Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full

Help	Specifies the port speed used for the selected boot protocol.

Field Name	**Wake On LAN**
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enables the server to be powered on using an in-band magic packet.

2.2 INTEL(R) I210 GIGABIT NETWORK CONNECTION – 00:22:4D:4D:00:02

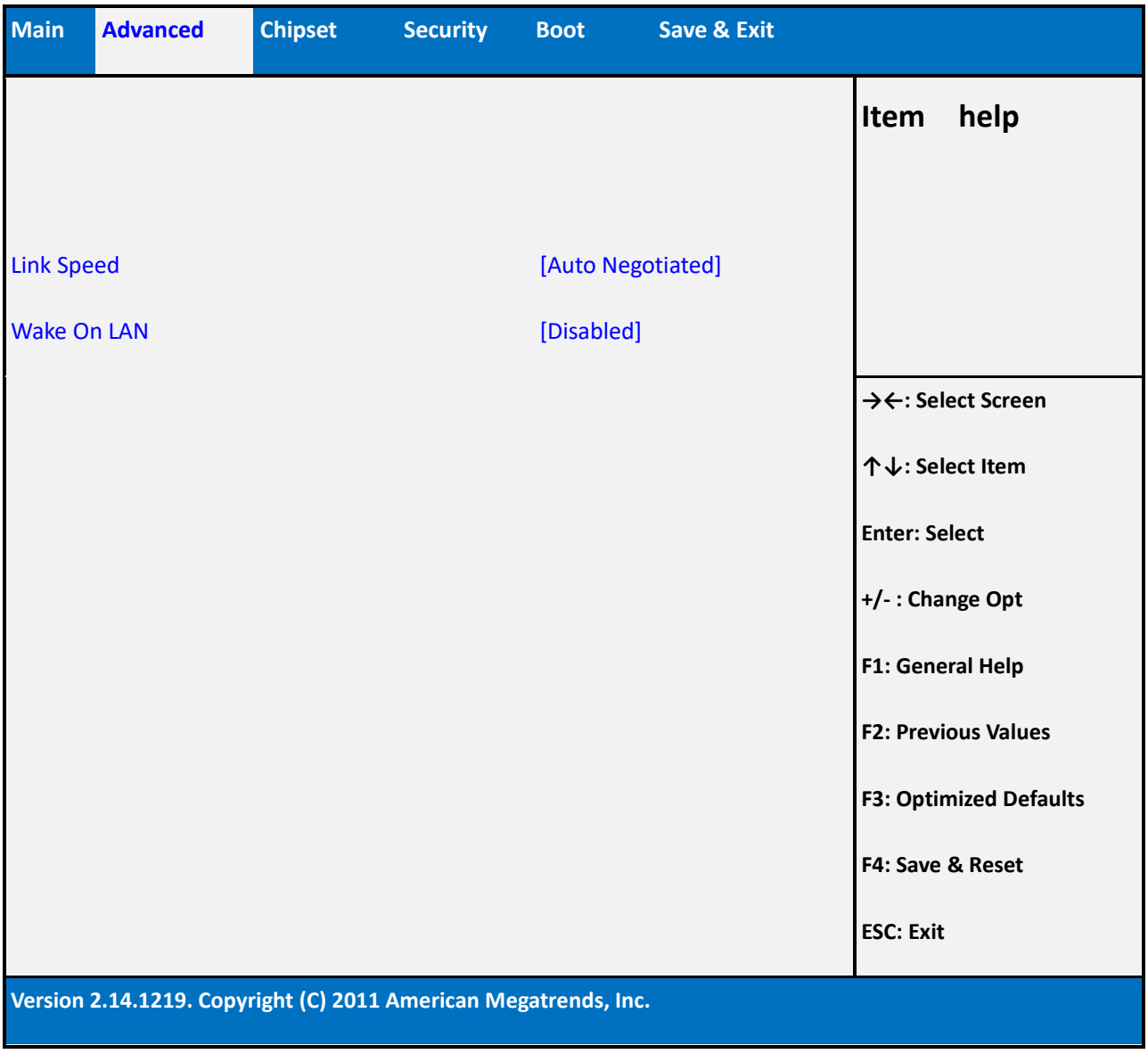
Main	Advanced	Chipset	Security	Boot	Save & Exit	
▶NIC Configuration						**Item help**
Blink LEDs			0			
UEFI Driver			Inter(R) PRO/1000 7.3…			
Adapter PBA			000300-000			
Device Name			Intel(R) I210 Gigabit…			
Chip Type			Intel i210			**→←: Select Screen**
PCI Device ID			1533			**↑↓: Select Item**
PCI Address			01:00:00			**Enter: Select**
						+/- : Change Opt
Link Status			[Disconnected]			**F1: General Help**
						F2: Previous Values
MAC Address			00:22:4D:4D:00:02			**F3: Optimized Defaults**
Virtual MAC Address			00:00:00:00:00:00			**F4: Save & Reset**
						ESC: Exit
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.						

Field Name	**NIC Configuration**
Help	Click to configure the network device port.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**Blink LEDs**

Default Value	0
Possible Value	0-15
Help	Identify the physical network port by blinking the associated LED.

2.1.1 NIC CONFIGURATION

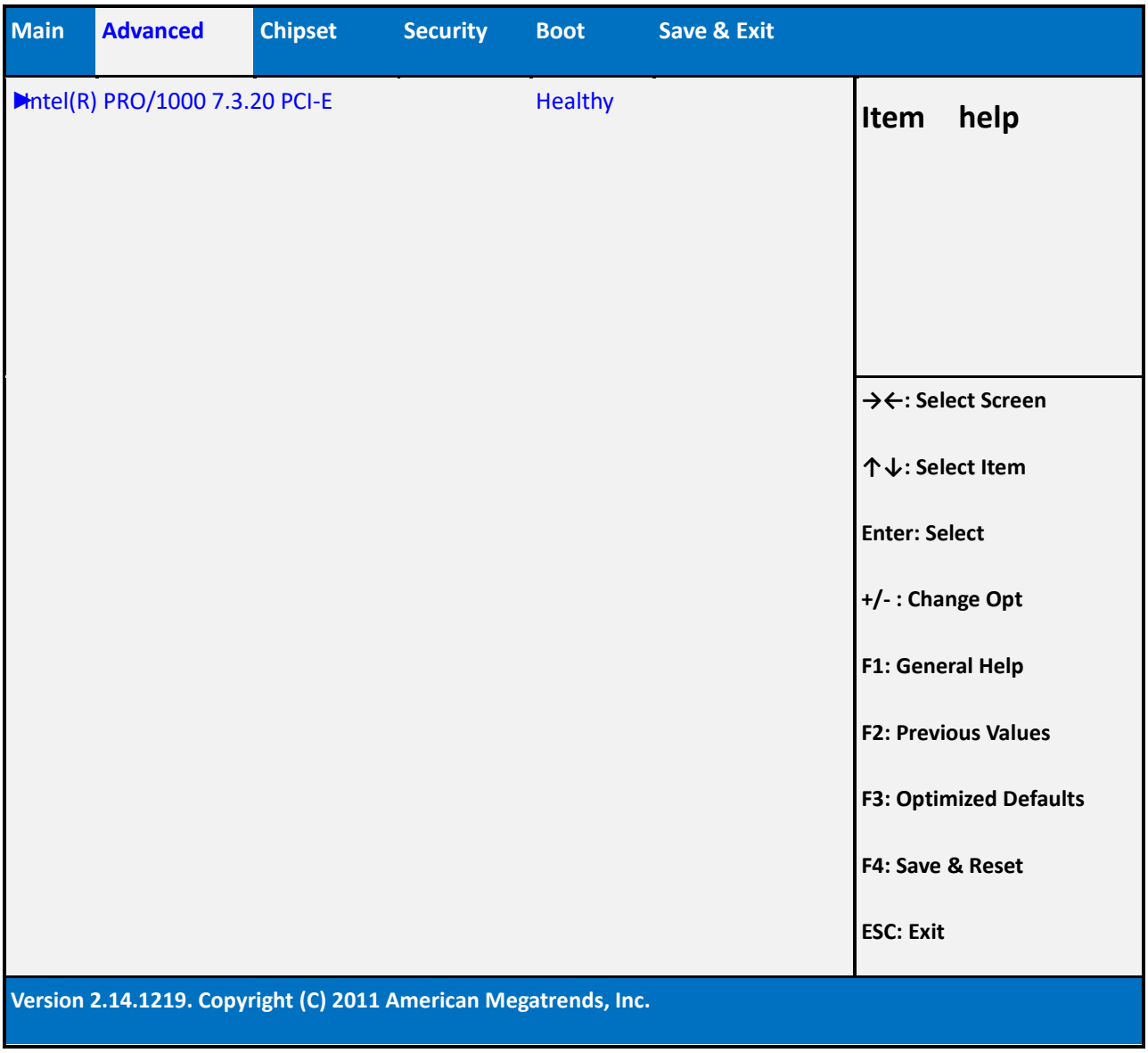


Field Name	**Link Speed**
Default Value	Auto Negotiated
Possible Value	Auto Negotiated 10Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full

Help	Specifies the port speed used for the selected boot protocol.

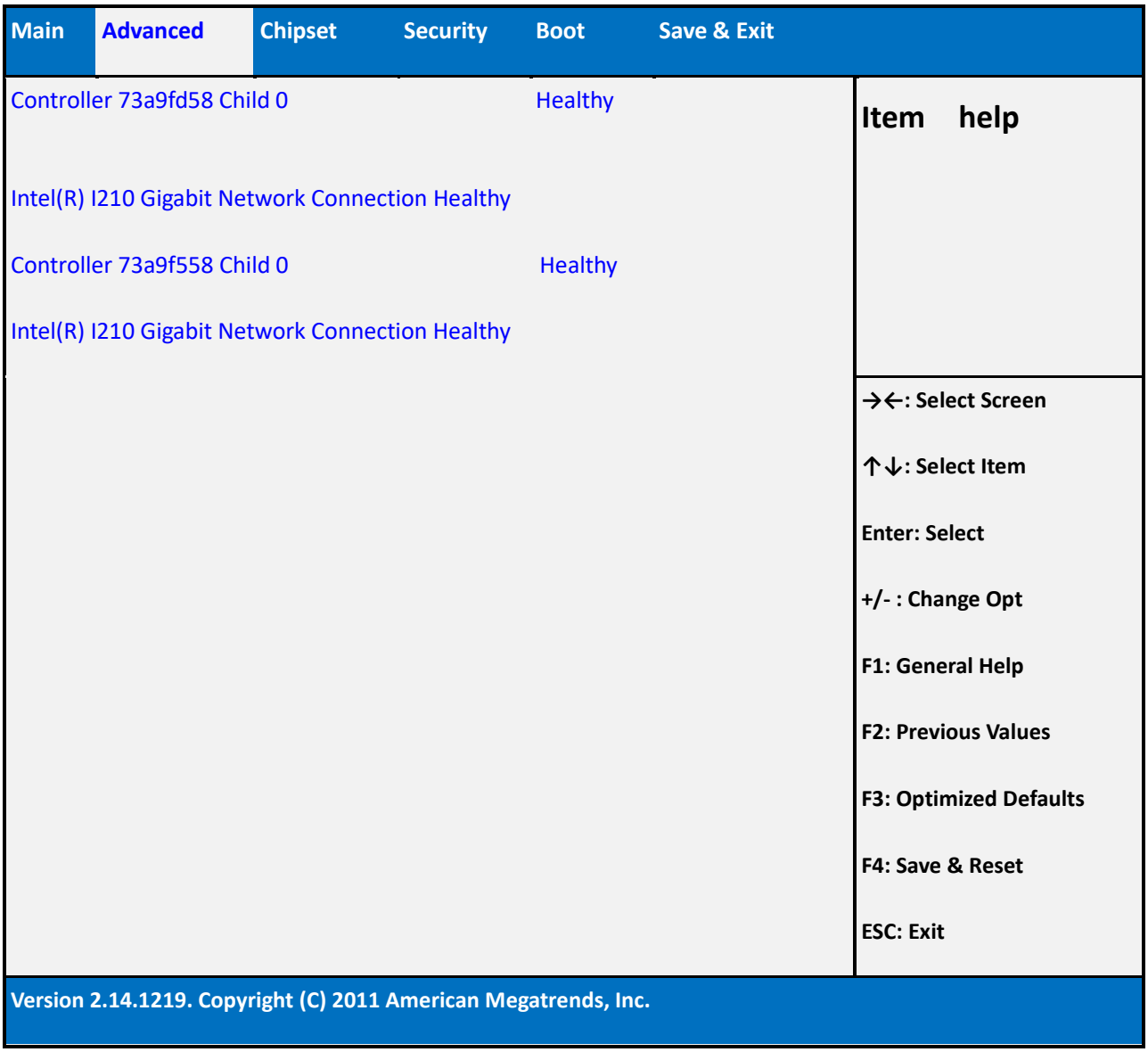
Field Name	**Wake On LAN**
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enables the server to be powered on using an in-band magic packet.

2.3 DRIVER HEALTH



Field Name	**Intel(R) PRO/1000 7.3.20 PCI-E**
Help	Provides Health Status for the Drivers/Controllers
Comment	Press Enter when selected to go into the associated Sub-Menu.

2.3.1 INTEL(R) PRO/1000 7.3.20 PCI-E



Field Name	**Controller 73a9fd58 Child 0**
Help	Provides Health Status for the Drivers/Controllers
Comment	Show driver/controller status

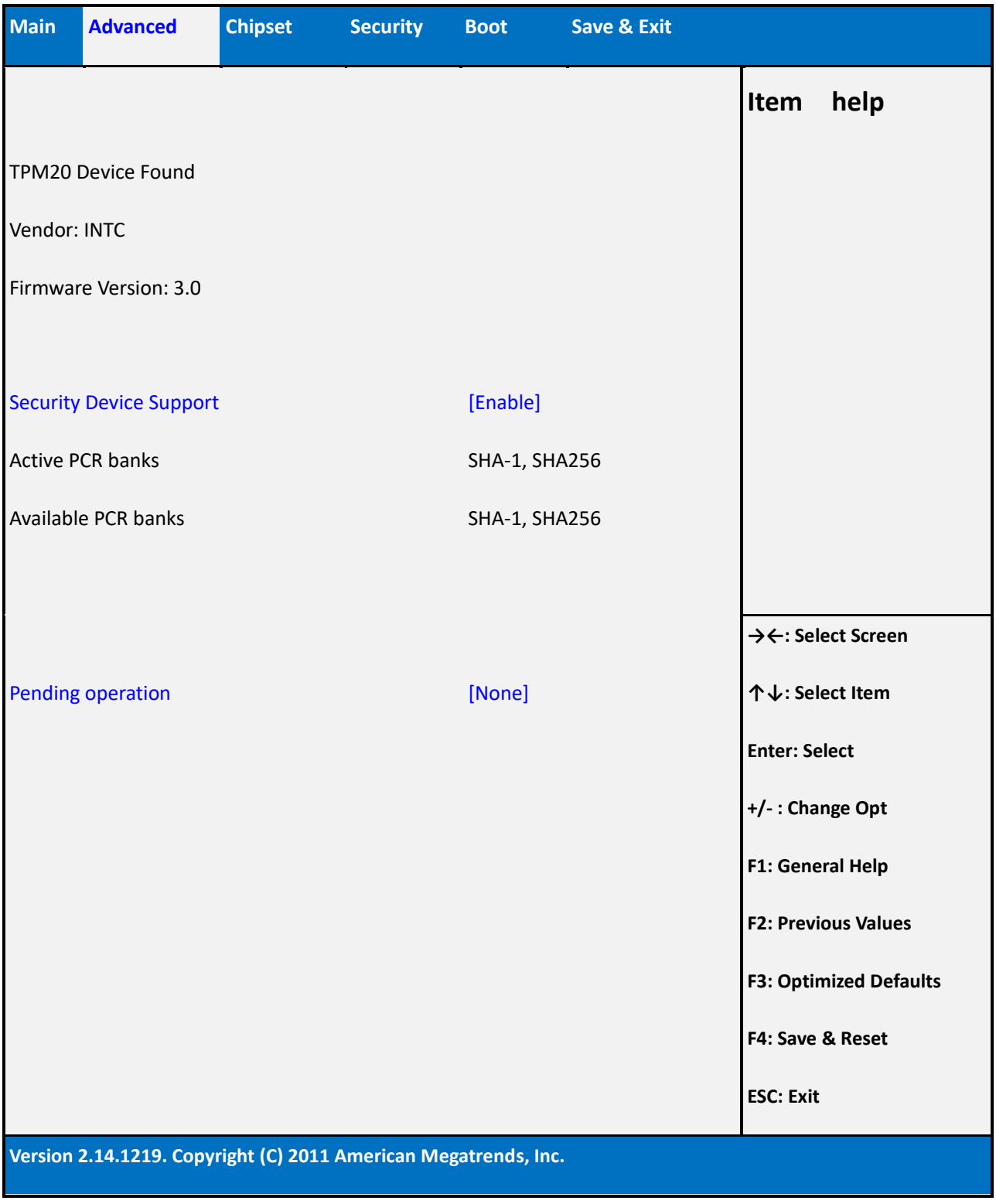
Field Name	**Intel(R) I210 Gigabit Network Connection**
Help	Provides Health Status for the Drivers/Controllers

Comment	Show driver/controller status

Field Name	**Controller 73a9f558 Child 0**
Help	Provides Health Status for the Drivers/Controllers
Comment	Show driver/controller status

Field Name	**Intel(R) I210 Gigabit Network Connection**
Help	Provides Health Status for the Drivers/Controllers
Comment	Show driver/controller status

2.4 TRUSTED COMPUTING

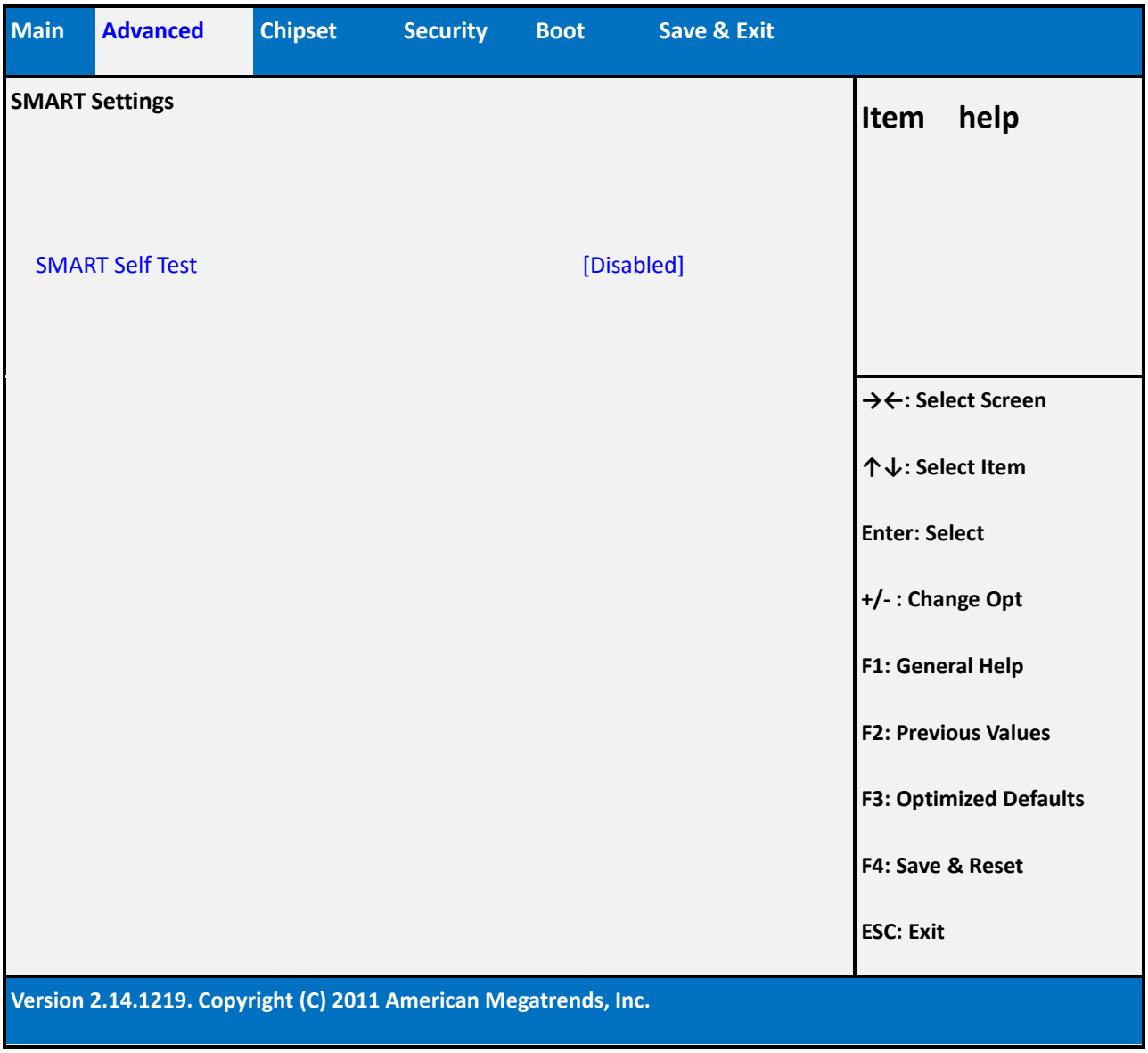


Field Name	**Security Device Support**
Default Value	Enabled

Possible Value	Disabled Enabled
Help	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

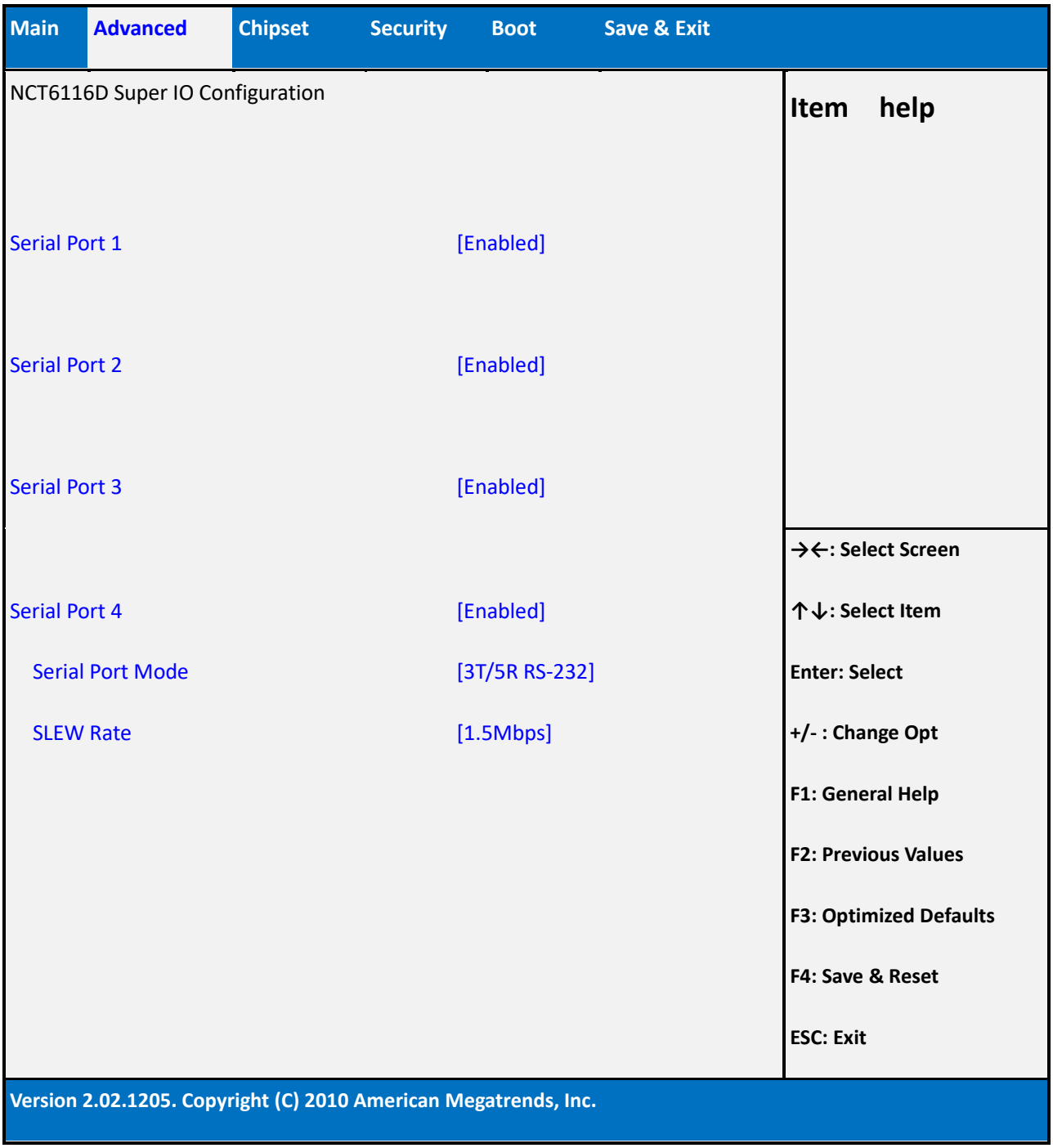
Field Name	**Pending operation**
Default Value	None
Possible Value	None TPM Clear
Help	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.

2.5 SMART SETTINGS



Field Name	SMART Self Test
Default Value	[Disabled]
Possible Value	Disabled Enabled
Help	Run SMART Self Test on all HDDs during POST.

2.6 NCT6116D SUPER IO CONFIGURATION



Field Name	Serial Port 1
Default Value	[Enabled]
Possible Value	Enabled Disabled
Help	Enable or Disable Serial Port (COM)

Field Name	Serial Port 2
Default Value	[Enabled]
Possible Value	Enabled Disabled
Help	Enable or Disable Serial Port (COM)

Field Name	Serial Port 3
Default Value	[Enabled]
Possible Value	Enabled Disabled
Help	Enable or Disable Serial Port (COM)

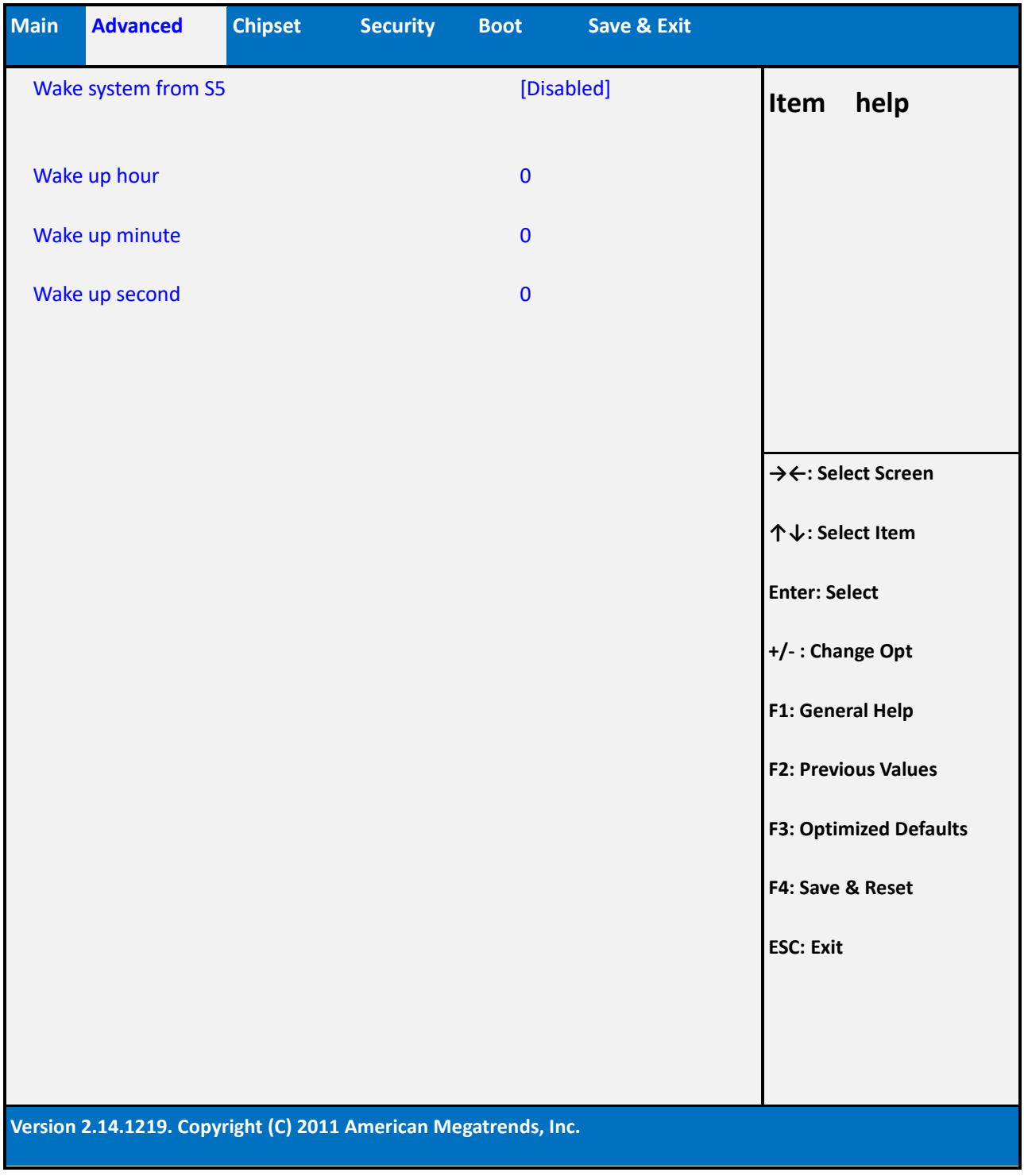
Field Name	Serial Port 4
Default Value	[Enabled]
Possible Value	Enabled Disabled
Help	Enable or Disable Serial Port (COM)

Field Name	Serial Port Mode
Default Value	[3T/5R RS-232]
Possible Value	1T/1R RS-422 3T/5R RS-232 1T/1R RS-485 TX ENABLE Low Active 1T/1R RS-485 with termination resistor TX ENABLE Low Active

	1T/1R RS-422 with termination resistor Disabled
Help	Enable or Disable Serial Port (COM)

Field Name	SLEW Rate
Default Value	[1.5Mbps]
Possible Value	256Kbps 1. 5Mbps
Help	Select SLEW rate to 1.5Mbps or 256Kbps

2.7 S5 RTC WAKE SETTINGS(NO FUNCTION WHEN DEEPSX POWER POLICIES ENABLED)



Field Name	Wake system from S5
Default Value	[Disabled]

Possible Value	Disabled Fixed Time Dynamic Time
Help	Enabler or disable System wake on alarm event, Select FixedTime, system will wake on the hr::min::sec specified. Select DynamicTime , system will wake on the current time + Increase minute (s)

Field Name	Wake up hour(Show when Wake system from S5 set to Fixed Time)
Default Value	0
Possible Value	0-23
Help	Select 0-23 For example enter 3 for 3am and 15 for 3pm

Field Name	Wake up minute(Show when Wake system from S5 set to Fixed Time)
Default Value	0
Possible Value	0-59
Help	0 - 59

Field Name	Wake up second(Show when Wake system from S5 set to Fixed Time)
Default Value	0
Possible Value	0 - 59
Help	0 - 59

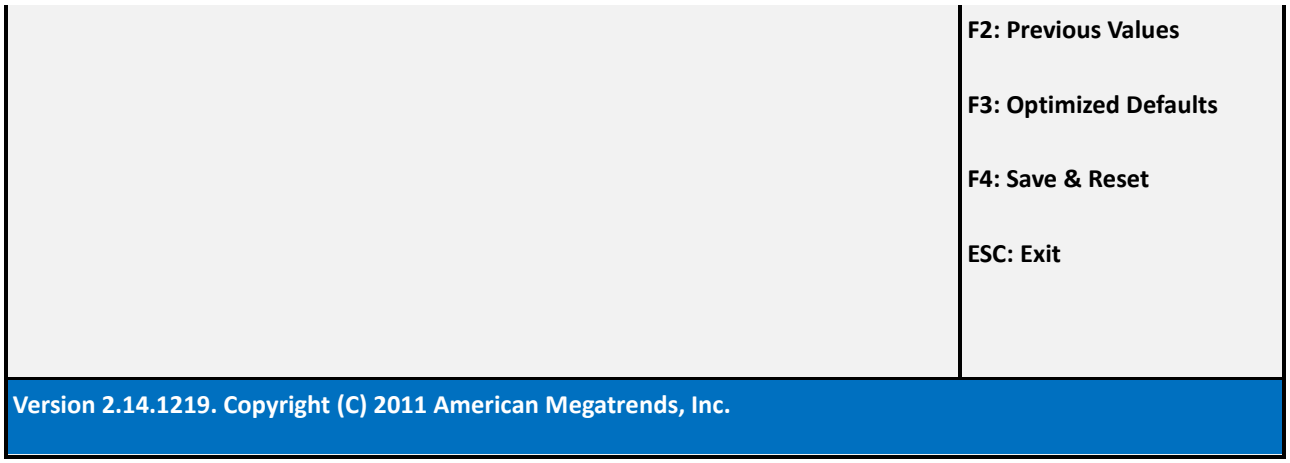
Field Name	Wake up minute increase(Show when Wake system from S5 set to Dynamic Time)
Default Value	1
Possible Value	1-5

Help	1 - 5

2.8 CPU CONFIGURATION

Main	Advanced	Chipset	Security	Boot	Save & Exit

CPU Configuration		Item help
Intel(R) Core(TM) CPU [CPU NAME] @ [CPU Freq.] GHz		
CPU Signature	406c3	
Microcode Patch	33c	
Max CPU Speed	1600 MHz	
Min CPU Speed	480 MHz	
Processor Cores	2	
Intel HT Technology	Not Supported	
Intel VT-x Technology	Supported	
L1 Data Cache	24 KB x 2	
L1 Code Cache	32 KB x 2	
L2 Cache	1024 KB x 1	
L3 Cache	Not Present	
64-bit	Supported	
Intel Virtualization Technology	[Enabled]	→←: Select Screen
EIST	[Enable]	↑↓: Select Item
Turbo mode	[Enable]	Enter: Select
		+/- : Change Opt
		F1: General Help



Field Name	CPU Configuration
Default Value	[Intel CPU Brand String]
Comment	This field is not selectable. There is no help text associated with it.

Field Name	CPU Signature
Default Value	Displays CPU Signature
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Microcode Patch
Default Value	CPU Microcode Patch Revision
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Max CPU Speed
Default Value	Displays the Max CPU Speed
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Min CPU Speed
Default Value	Displays the Min CPU Speed

Comment	This field is not selectable. There is no help text associated with it.

Field Name	CPU Speed
Default Value	Displays the CPU Speed
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Processor Cores
Default Value	Displays number of cores.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Intel HT Technology
Default Value	When Hyper-threading is enabled, 2 logical CPUS per core is present.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Intel VT-x Technology
Default Value	CPU VMX hardware support for virtual machines.
Comment	This field is not selectable. There is no help text associated with it.

Field Name	64-bit
Default Value	Displays if 64-bit supported
Comment	This field is not selectable. There is no help text associated with it.

Field Name	L1 Data Cache
Default Value	L1 Data Cache Size
Comment	This field is not selectable. There is no help text associated with it.

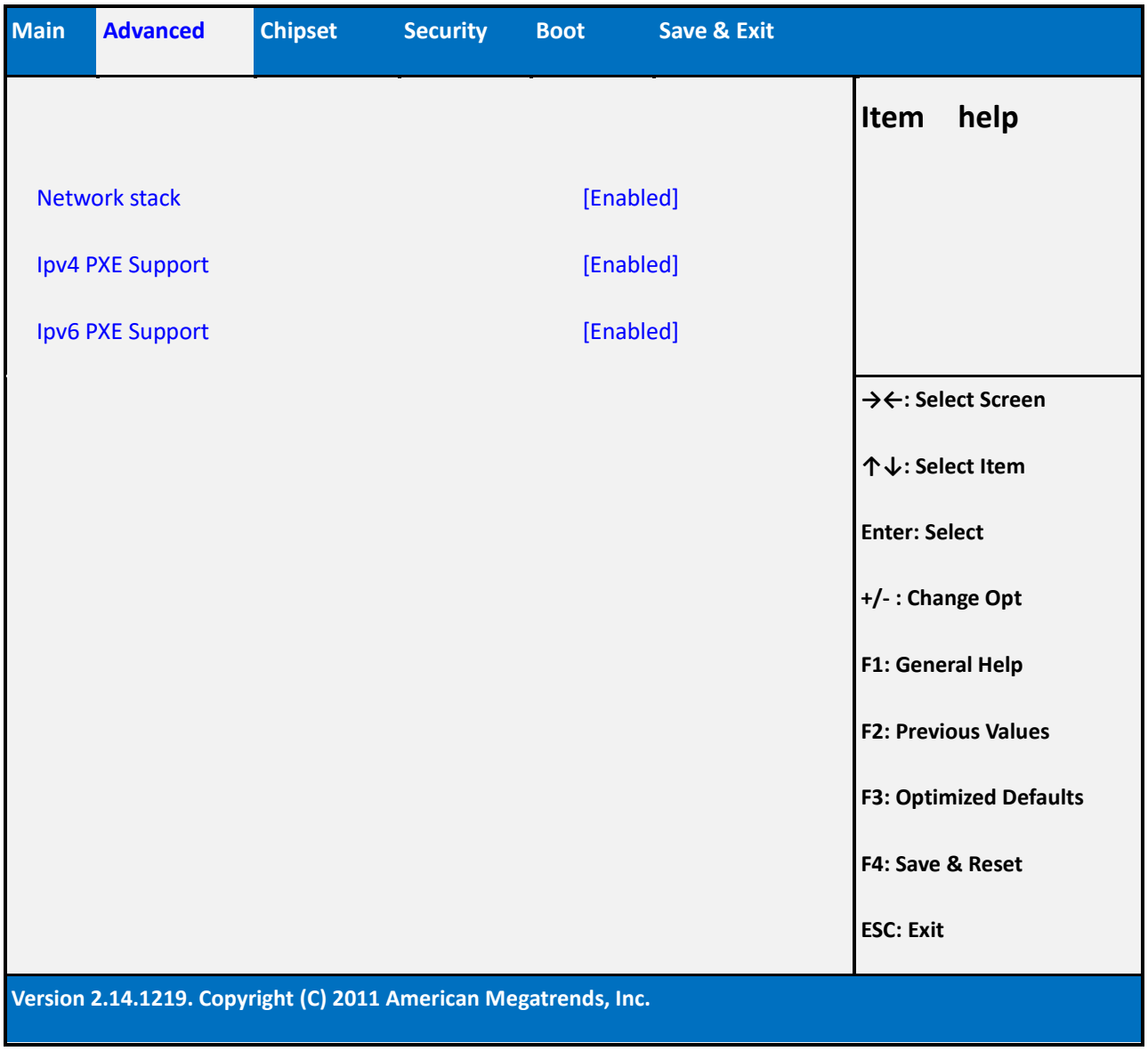
Field Name	L1 Code Cache
Default Value	L1 Code Cache Size
Comment	This field is not selectable. There is no help text associated with it.

Field Name	L2 Cache
Default Value	L2 Cache Size
Comment	This field is not selectable. There is no help text associated with it.

Field Name	L3 Cache
Default Value	L3 Cache Size
Comment	This field is not selectable. There is no help text associated with it.

Field Name	Intel Virtualization Technology
Default Value	[Disabled]
Possible Value	Enabled Disabled
Help	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

2.9 NETWORK STACK CONFIGURATION



Field Name	Network stack
Default Value	[Enabled]
Possible Value	Disabled Enabled
Help	Enable/Disable UEFI network stack.

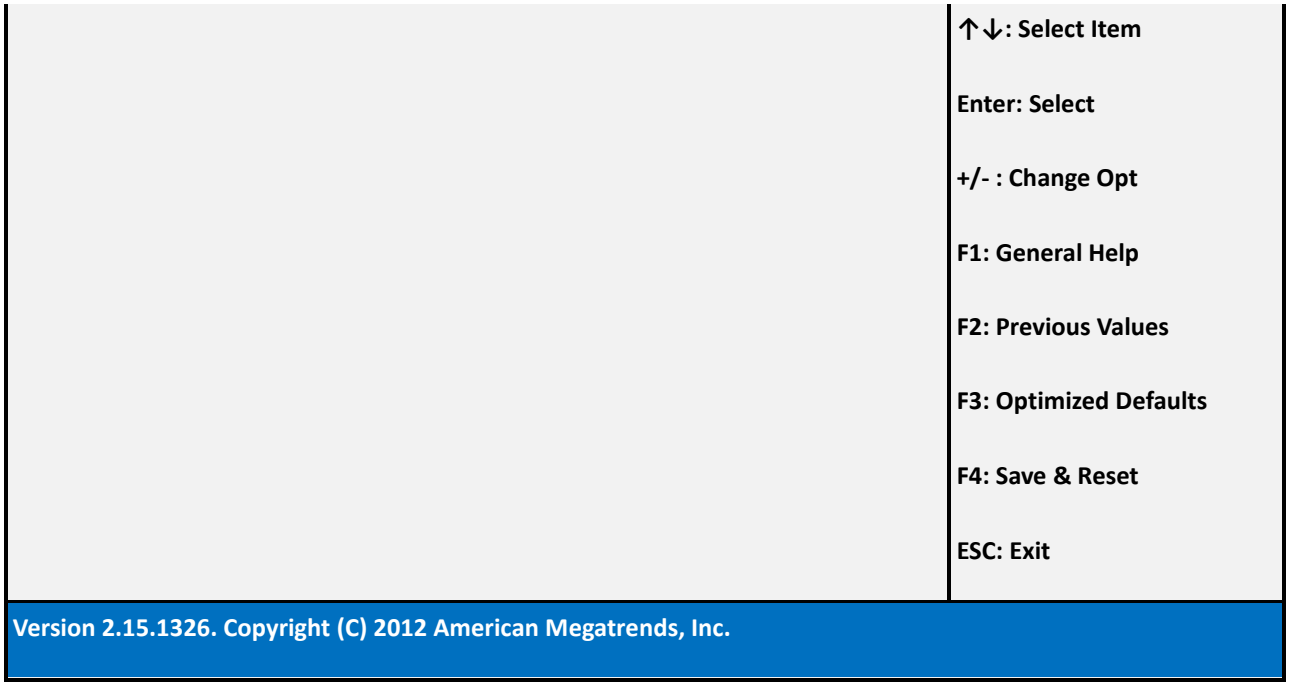
Field Name	Ipv4 PXE Support
Default Value	[Enabled]

Possible Value	Disabled Enabled
Help	Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.

Field Name	Ipv6 PXE Support
Default Value	[Enabled]
Possible Value	Disabled Enabled
Help	Enable Ipv6 PXE Boot Support. If disabled IPV6 PXE boot option will not be created.

2.10PLATFROM TRUST TECHNOLOGY

Main	Advanced	Device	Chipset	Security	Boot	Save & Exit	
TPM Configuration							**Item help**
fTPM				[Enabled]			
							→←: Select Screen



Field Name	Compatibility Support Module Configuration

Field Name	fTPM Support
Default Value	[Enabled]
Possible Value	Disabled/Enabled
Help	Enable/Disable fTPM

3. CHIPSET

Field Name	Restore AC Power State

Default Value	[Power Off]
Possible Value	Power off Power on Last State
Help	Select AC power state when power is re-applied after a power failure.

Field Name	DeepSx Power Policies
Default Value	Disabled
Possible Value	Disabled Enabled
Help	Configure the DeepSx Mode configuration.
Note	When enabled, “Wake On Lan” and “S5 RTC Wake Settings” are no function.

Field Name	Output Panel Type
Default Value	Disable
Possible Value	LVDS eDP Disabled
Help	Select Output Panel Type

Field Name	LVDS Interface Type
Default Value	8 bit-VESA Dual Channel
Possible Value	8 bit-VESA Single Channel 8 bit-VESA Dual Channel

	6 bit-VESA Single Channel 6 bit-VESA Dual Channel
Help	Sets LVDS connectivity.
Comment	This field only show when Output Panel Type set to LVDS

Field Name	LVDS Panel Type
Default Value	1920x1080
Possible Value	800x600 1024x768 1366x768 1280x800 1920x1080
Help	Select LVDS panel used by Internal Graphics Device by selecting the appropriate setup item.
Comment	This field only show when Output Panel Type set to LVDS

Field Name	DVMT Pre-Allocated
Default Value	[64M]
Possible Value	64M /96M /128M /160M /192M /224M /256M /288M /320M 352M /384M /416M /448M /480M /512M
Help	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

Field Name	DVMT Total Gfx Mem
Default Value	[256MB]

Possible Value	128MB /256MB /Max
Help	Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.

Field Name	Wake On Lan
Default Value	Enabled
Possible Value	Disabled Enabled
Help	Enable or Disable the Wake on Lan

Field Name	OS Selection
Default Value	Windows
Possible Value	Windows Intel Linux
Help	Select the target OS.

4. SECURITY

Main	Advanced	Chipset	Security	Boot	Save & Exit

Password Description

If Only the Administrator's password is set

then this only limits access to Setup and is

only asked for when entering Setup

If ONLY the User's password is set, then this

Is a power on password and must be entered to

boot or enter Setup. In Setup the User will.

have Administrator rights.

The password length must be

in the following range:

Minimum Length 3

Maximum Length 20

Setup Administrator Password

User Password

HDD Security Configuration

P0:Device Name

▶Secure Boot

Item help

→←: Select Screen

↑↓: Select Item

Enter: Select

+/- : Change Opt

F1: General Help

F2: Previous Values

F3: Optimized Defaults

F4: Save & Reset

ESC: Exit

Field Name	Setup Administrator Password
Help	Set Administrator Password
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	User Password
Help	Set User Password.
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	**P0: Device Name**
Help	HDD Security Configuration for selected drive
Comment	Press Enter when selected to go into the associated Sub-Menu.

Field Name	Secure Boot
Help	Customizable Secure Boot settings.
Comment	Press Enter when selected to go into the associated Sub-Menu.

2.11 HDD SECURITY CONFIGURATION

Main	Advanced	Chipset	Security	Boot	Save & Exit

HDD Password Description

Allow Access to Set, Modify and Clear
Hard Disk User and Master Password.
User Password need to be installed for
Enabling Security. Master Password can
Be Modified only when successfully unlocked
With Master Password in POST.
If the 'Set HDD Password' option is grayed out,
do power cycle to enable the option again.

HDD PASSWORD CONFIGURATION:

Security Supported	:	Yes
Security Enabled	:	No
Security Locked	:	No
Security Frozen	:	No
HDD User Pwd Status		NOT INSTALLED

Set User Password

Item help

→←: Select Screen
↑↓: Select Item
Enter: Select
+/- : Change Opt
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Reset
ESC: Exit

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Field Name	Set User Password
Help	Set HDD User Password
Comment	Press Enter when selected to go into the associated Sub-Menu.

2.12 SECURE BOOT MODE

Main	Advanced	Chipset	Security	Boot	Save & Exit	
						Item help
System Mode				Setup		
Vendor Keys				Not Modified		
Secure Boot Enable				[Enabled]		**→←: Select Screen**
						↑↓: Select Item
						Enter: Select
Secure Boot Mode				[Standard]		**+/- : Change Opt**
▶Key Management						**F1: General Help**
						F2: Previous Values
						F3: Optimized Defaults

	F4: Save & Reset **ESC: Exit**
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Field Name	Secure Boot Enable
Default Value	[Enabled]
Possible Value	Enabled / Disabled
Help	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM function is disabled

Field Name	Secure Boot Mode
Default Value	[Standard]
Possible Value	Standard / Custom
Help	Secure Boot Mode - Custom & Standard, Set UEFI Secure Boot Mode to STANDARD mode or CUSTOM mode, this change is effect after save. And after reset, the mode will return to STANDARD mode

Field Name	Key Management
Help	Enables experienced users to modify Secure Boot variables
Comment	Press Enter when selected to go into the associated Sub-Menu.

2.13KEY MANAGERMENT

Main	Advanced	Chipset	Security	Boot	Save & Exit

Provision Factory Default [Disabled]

Item help

▶Restorel Factory Keys

▶Enroll Efi Image

▶Export Secure Boot variables

Secure Boot variable	size	key#	key source
▶Platform Key(PK)	0	0	No Keys
▶Key Exchange Key	0	0	No Keys
▶Authorized Signatures	0	0	No Keys
▶Forbidden Signatures	0	0	No Keys
▶Authorized TimeStamps	0	0	No Keys
▶OsRecovery Signatures	0	0	No Keys

→←: Select Screen

↑↓: Select Item

Enter: Select

+/- : Change Opt

F1: General Help

F2: Previous Values

F3: Optimized Defaults

F4: Save & Reset

ESC: Exit

Field Name	Provision Factory Default
Default Value	[Disabled]
Possible Value	Enabled Disabled
Help	Provision factory default keys on next system re-boot while platform is in Setup Mode.

Field Name	Restore Factory Keys
Help	Reset the content of all UEFI Secure Boot key databases to their factory default values
Comment	

Field Name	Reset to Setup Mode
Help	Delete the content of all UEFI Secure Boot key databases. This puts the system in Setup Mode
Comment	

Field Name	Enroll Efi Image
Help	Allow the image to run in Secure Boot mode. Enroll SHA256 hash of an efi binary into Authorized Signature Database(db)
Comment	

Field Name	Export Secure Boot Variables
Help	Save NVRAM content of Secure Boot policy variables to the files

	(EFI_SIGNATURE_LIST data format) in root folder on a target file system device
Comment	

Field Name	Platform Key (PK) : 0 0 No Keys
Possible Value	Details Export Set New Delete
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,TestAMI

Field Name	Key Exchange Key : 0 0 No Keys
Possible Value	Details Export Set New Append Delete
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,TestAMI

Field Name	Authorized Signature : 0 0 No Keys
Possible Value	Details

	Export Set New Append Delete
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256)\nKey Source: Default,External,Mixed,TestAMI

Field Name	Forbidden Signature : 0 0 No Keys
Possible Value	Details Export Set New Append Delete
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,TestAMI

Field Name	Authorized TimeStamps : 0 0 No Keys
Possible Value	Set New Append
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256)\nKey Source: Default,External,Mixed,TestAMI

Field Name	OsRecovery Signatures: 0 0 No Keys
Possible Value	Set New Append
Help	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256)\nKey Source: Default,External,Mixed,TestAMI

5. BOOT

Boot mode select = UEFI

Main	Advanced	Chipset	Boot	Security	Save & Exit	
Boot Configuration						**Item help**
	Setup Prompt Timeout		3			
	Bootup NumLock State		[On]			
	Fast Boot		[Enable]			
FIXED BOOT ORDER Priorities						
	Boot Option #1		[Hard Disk]			
	Boot Option #2		[CD/DVD]			
	Boot Option #3		[USB Hard DIsk]			
	Boot Option #4		[USB CD/DVD]			
	Boot Option #5		[USB Key]			
	Boot Option #6		[USB Floppy]			
	Boot Option #7		[USB Lan]			
	Boot Option #8		[Network]			
						→←: Select Screen
						↑↓: Select Item
UEFI CD/DVD ROM Drive BBS Priorities						**Enter: Select**
UEFI Hard Disk Drive BBS Priorities						**+/- : Change Opt**
UEFI NETWORK Drive BBS Priorities						**F1: General Help**
UEFI USB CD/DVD ROM Drive BBS Priorities						**F2: Previous Values**
UEFI USB Hard Disk Drive BBS Priorities						**F3: Optimized Defaults**

UEFI USB KEY Drive BBS Priorities	**F4: Save & Reset** **ESC: Exit**
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Field Name	**Setup Prompt Timeout**
Default Value	3
Possible Value	1~65535
Help	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Field Name	**Boot NumLock State**
Default Value	[On]
Possible Value	On Off
Help	Select the keyboard NumLock state

Field Name	**Fast Boot**
Default Value	[Enabled]
Possible Value	Enabled Disabled
Help	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot mode select = UEFI

Field Name	**Boot Option #1**
Default Value	[Hard Disk]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #2**
Default Value	[CD/DVD]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #3**
Default Value	[USB Hard Disk]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #4**
Default Value	[USB CD/DVD]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #5**
Default Value	[USB Key]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #6**
Default Value	[USB Floppy]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #7**
Default Value	[USB Lan]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

Field Name	**Boot Option #8**
Default Value	[Network]
Possible Value	CD/DVD, Hard Disk, Network, USB CD/DVD, USB Hard Disk, USB KEY, USB Floppy, USB Lan
Help	Set the system boot order

6. SAVE & EXIT

Main	Advanced	Chipset	Security	Boot	Save & Exit

Save Options

Save Changes and Exit

Discard Changes and Exit

Save Changes and Reset

Discard Changes and Reset

Restore Defaults

Boot Override

Item help

→←: Select Screen

↑↓: Select Item

Enter: Select

+/- : Change Opt

F1: General Help

F2: Previous Values

F3: Optimized Defaults

F4: Save & Reset

ESC: Exit

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Field Name	Save Options

Field Name	Save Changes and Exit
Help	Exit system setup after saving the changes.
Comment	

Field Name	Discard Changes and Exit
Help	Exit system setup without saving the changes.
Comment	

Field Name	Save Changes and Reset
Help	Reset the system after saving the changes.
Comment	

Field Name	Discard Changes and Reset
Help	Reset system setup without saving any changes.
Comment	

Field Name	Restore Defaults
Help	Restore/Load Default values for all the setup options.
Comment	