IEI

IEI Integration Corp.

MODEL:

NANO-PV-D4252/N4552/D5252

EPIC Motherboard with Intel® Atom™ Processor D425/N455/D525, VGA, Dual LVDS, GbE LAN, Eight USB 2.0, Two SATA 3Gb/s, Four RS-232, RS-232/422/485, PCIe Mini, PCI-104, RoHS

User Manual

Rev. 1.13 – June 24, 2016

RoHS Lead Free

Revision

Date	Version	Changes
June 24, 2016	1.13	Added a note for using the LVDS2 and VGA connectors as dual display output (on pages 26 and 40)
November 13, 2015	1.12	Updated Section 1.3: Dimensions
September 21, 2015	1.11	Updated connector layout and Section 4.5.10
June 18, 2015	1.10	Updated for R11 version
March 2, 2015	1.06	Modified **Memory** spec on page 7 Updated Chapter 2
December 31, 2011	1.05	Added note to Section 3.1.3 and Section 4.8
August 24, 2011	1.04	Minor revision to pin definitions in the following sections: 4.5.9 LVDS1 Screen Resolution Selection 4.5.10 LVDS2 Screen Resolution Selection
June 17, 2011	1.03	Minor revision to pin definitions in section 3.2.16 Power Connector
April 18, 2011	1.02	Updated Table 4-7, 4-8, and 4-10 jumper settings. Updated KEY1 connector to LVDS2 Backlight Adjustment.
January 6, 2011	1.01	Revised Pins 11, 12, 23, 24 in Table 3-14 LVDS2 Connector Pinouts
November 24, 2010	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

HOT SURFACE

This symbol indicates a hot surface that should not be touched without taking care.

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Introduction

1.1 Introduction
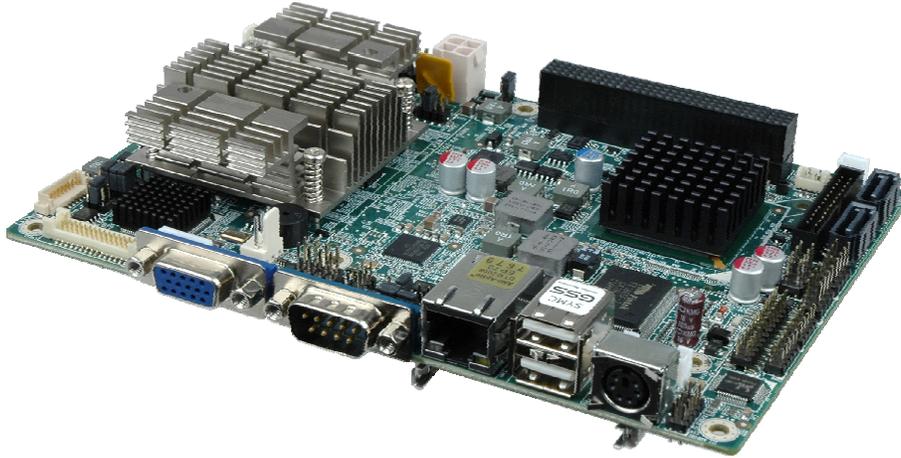
Figure 1-1: NANO-PV-D4252/N4552/D5252

The NANO-PV-D4252/N4552/D5252 EPIC motherboard is an Intel® Atom™ processor D525, D425 or N455 platform. Up to one 2.0 GB or 4.0 GB 800 MHz DDR3 SDRAM SO-DIMM is supported by the NANO-PV-D4252/N4552/D5252.

The integrated Intel® ICH8M chipset supports a GbE LAN port through the Realtek RTL8111E Ethernet controller (with ASF 2.0 support). The NANO-PV-D4252/N4552/D5252 also supports two SATA 3Gb/s drives and provides 5 V SATA power.

The NANO-PV-D4252/N4552/D5252 supports dual display via VGA and two internal LVDS LCD connectors. Eight USB 2.0 channels, one PCIe Mini socket, one PCI-104 slot and internal one parallel port connector provide flexible expansion options. High Definition Audio (HDA) support ensures HDA devices can be easily implemented on the NANO-PV-D4252/N4552/D5252. Serial device connectivity is provided by a RS-232 serial port, three internal RS-232 and one internal RS-232/422/485 connectors.

1.2 Connectors

The connectors on the NANO-PV-D4252/N4552/D5252 are shown in the figures below.
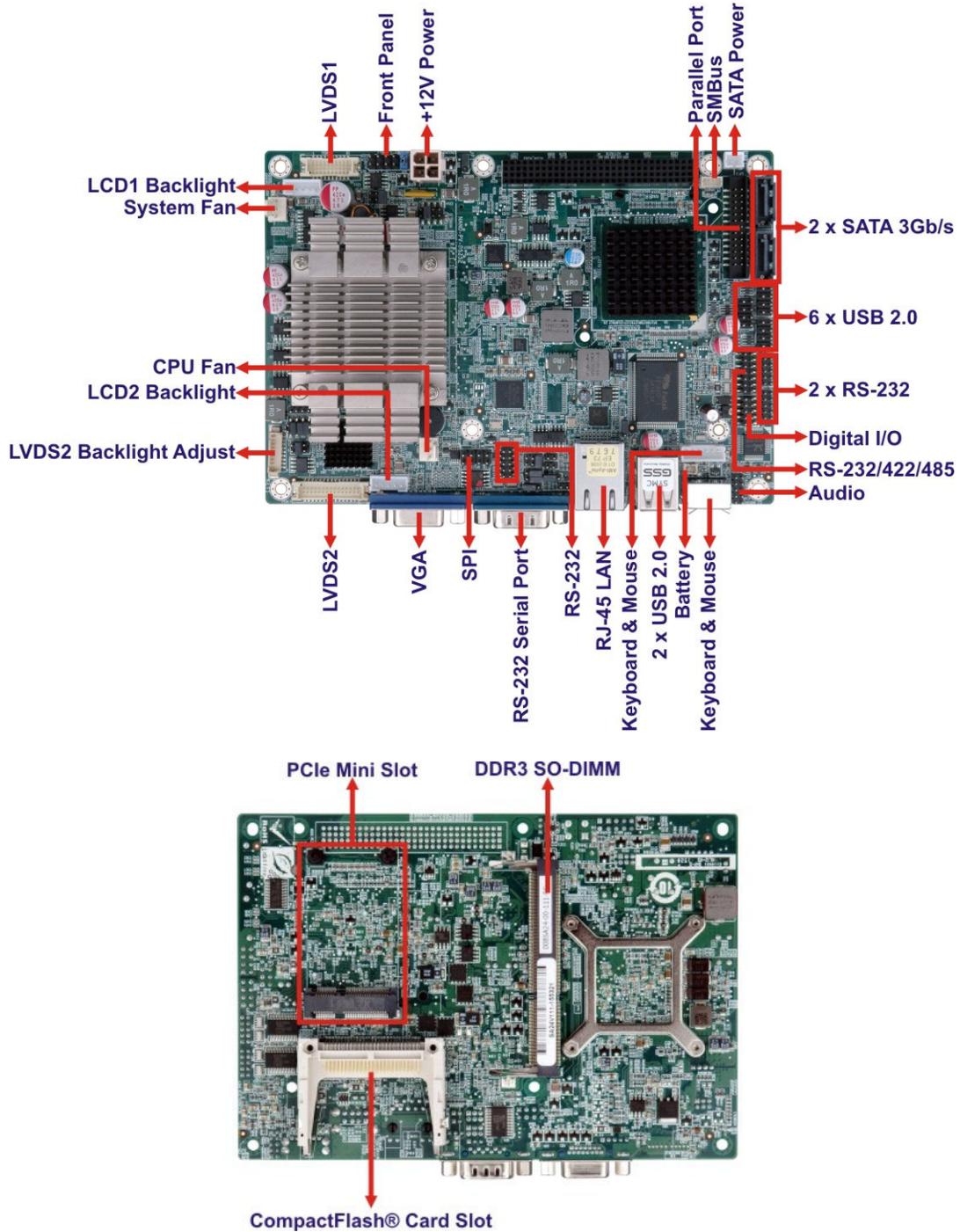
Figure 1-2: Connectors

1.3 Dimensions

The dimensions of the board are listed below:
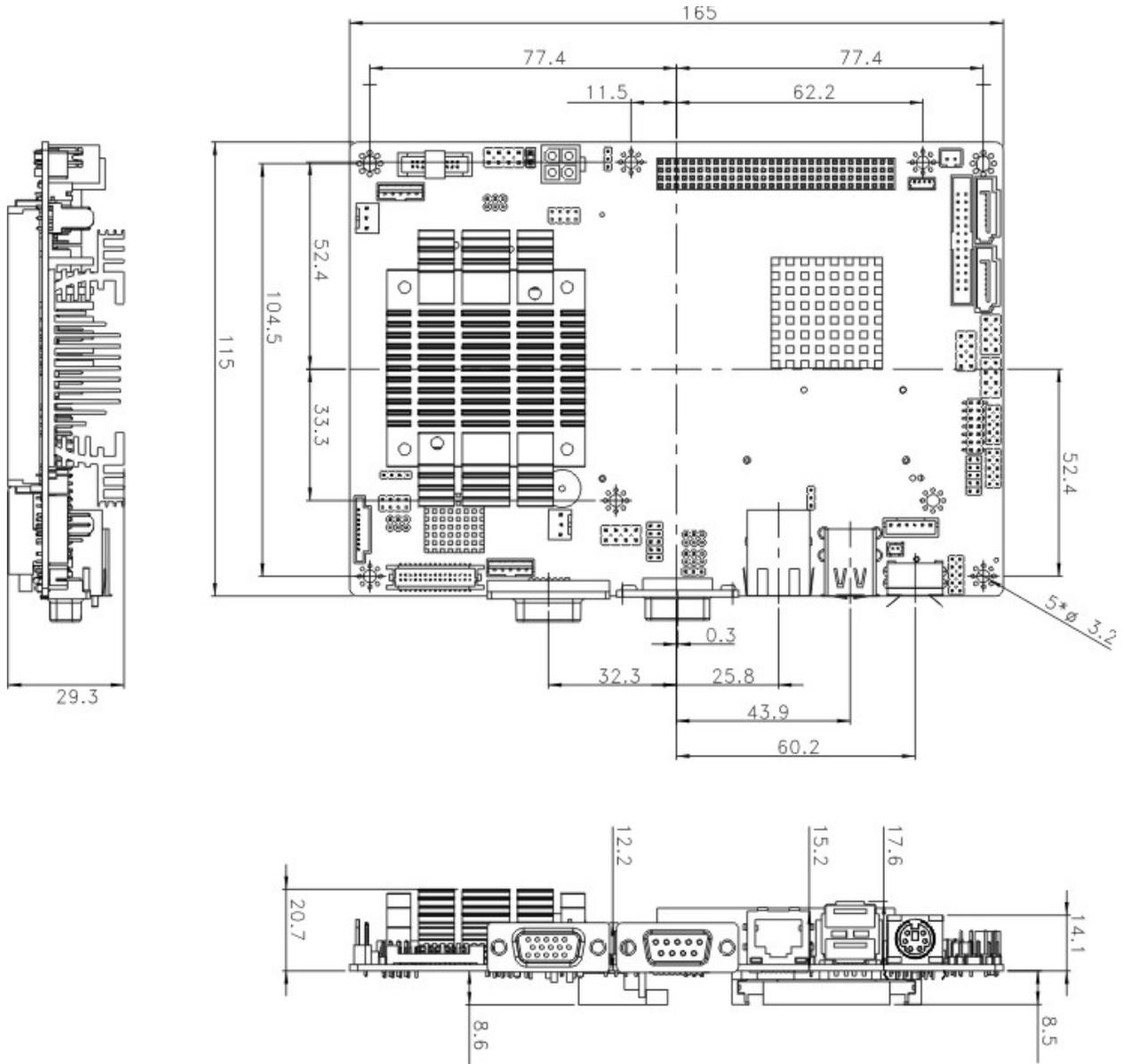
Figure 1-3: NANO-PV-D4252/N4552 Dimensions (mm)
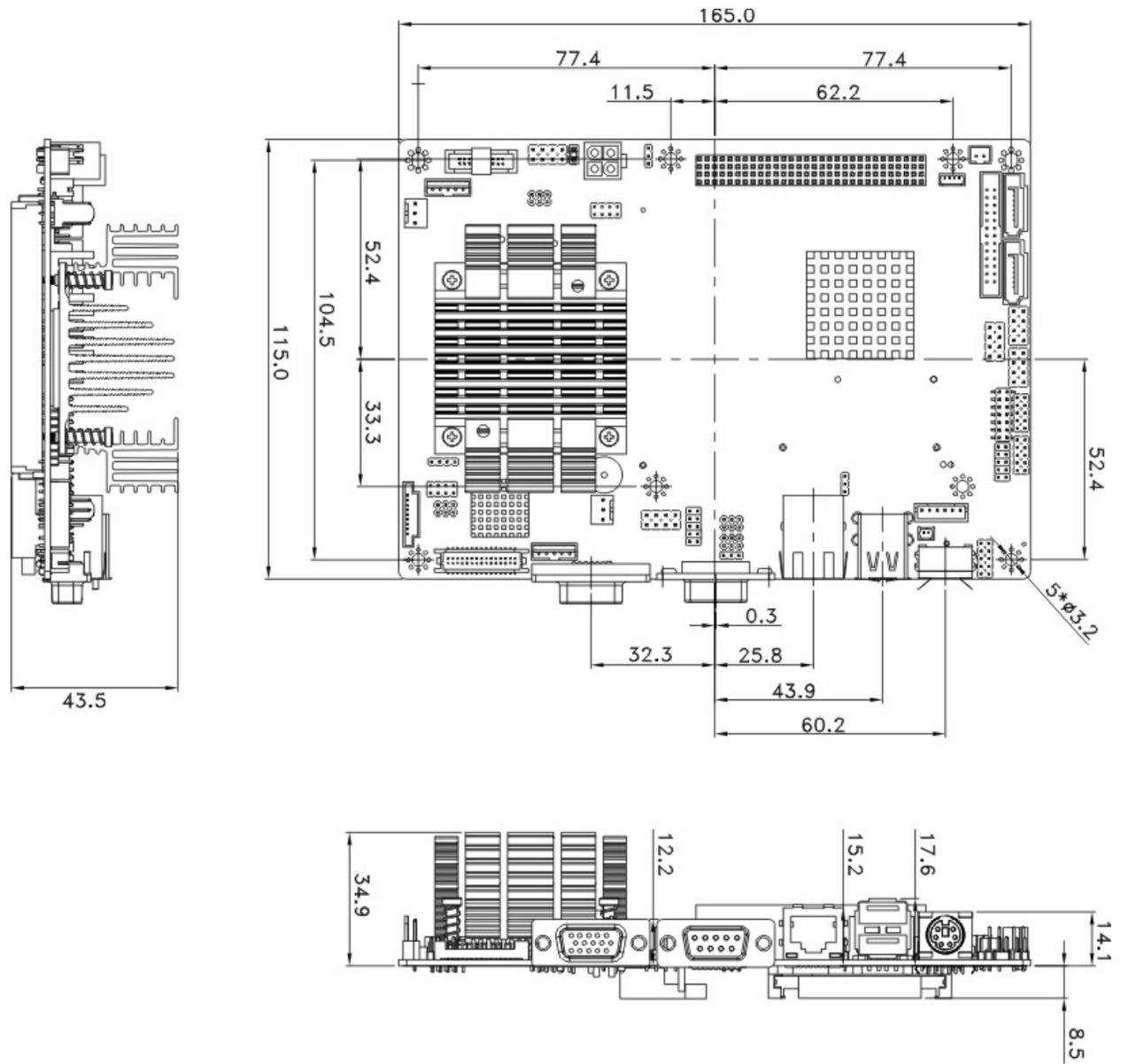
Figure 1-4: NANO-PV-D5252 Dimensions (mm)

1.4 Data Flow

Figure 1-5 shows the data flow between the two on-board chipsets and other components installed on the motherboard and described in the following sections of this chapter.
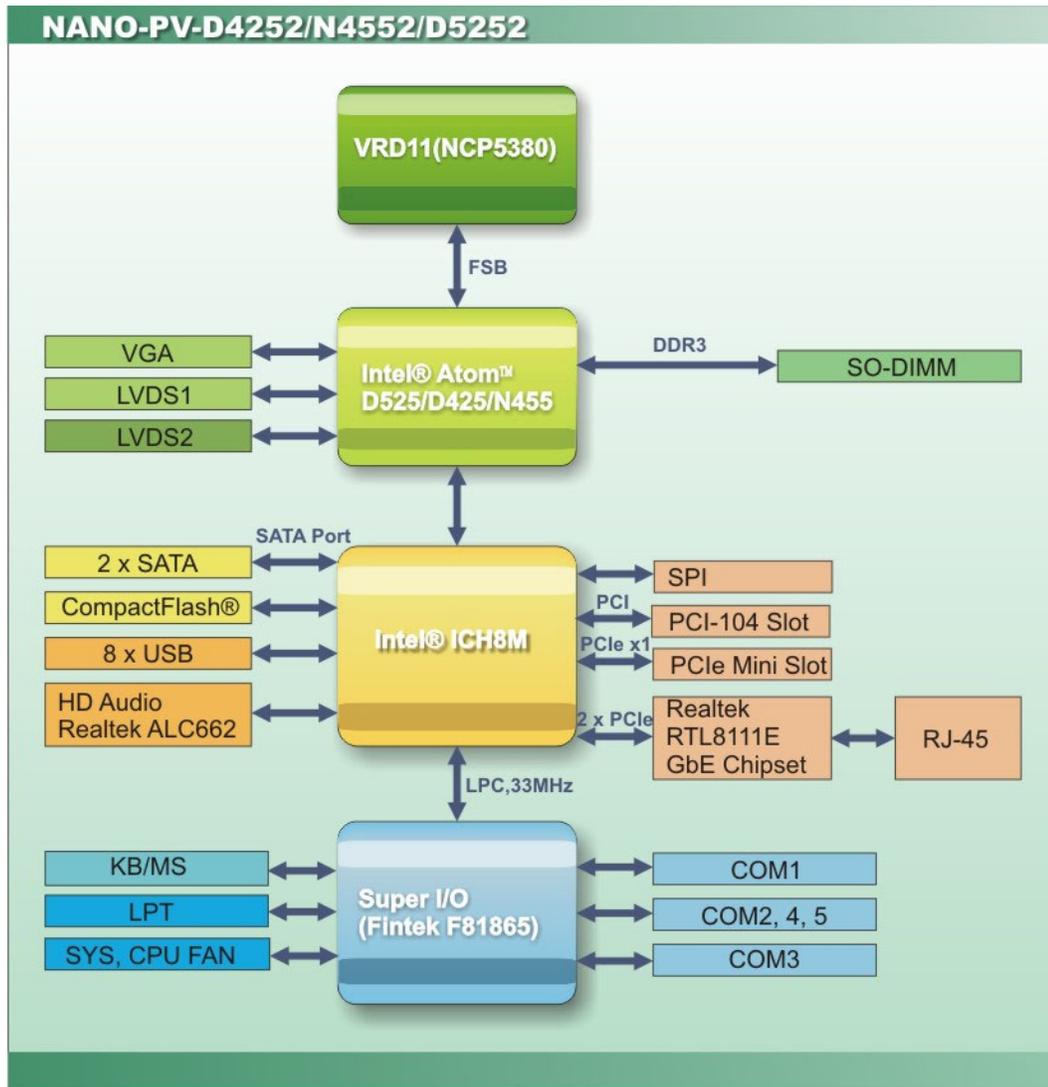
Figure 1-5: Data Flow Block Diagram

1.5 Technical Specifications

NANO-PV-D4252/N4552/D5252 technical specifications are listed in table below.

Specification	NANO-PV-D4252/N4552/D5252
Form Factor	EPIC
CPU options	Intel® Atom™ processor D525, 1.8 GHz/1 MB L2 cache Intel® Atom™ processor D425, 1.8 GHz/512 KB L2 cache Intel® Atom™ processor N455, 1.66 GHz/512 KB L2 cache
Express Chipset	Intel® ICH8M
Memory	One 204-pin 800 MHz DDR3 SDRAM SO-DIMM supported ▪ D525/D425: System max. 4.0 GB ▪ N455: System max. 2.0 GB
Audio	Realtek ALC662 HD audio codec
LAN	One Realtek RTL8111E PCIe GbE controller with ASF 2.0 support
Super I/O	Fintek F81865
Digital I/O	8-bit digital I/O
BIOS	AMI BIOS label
Watchdog Timer	Software programmable supports 1~255 sec. system reset
Expansion	
PCIe	One PCIe Mini slot
PCI	One PCI-104 slot
I/O Interface Connectors	
Audio Connector	One internal audio connector (10-pin header)
Display Ports	One VGA port (2048x1536) One internal 24-bit dual-channel LVDS connector by Novatek NT68660BUFG (up to 1920x1080) One internal 18-bit single-channel LVDS connector (up to 1024x768 or 1366x768)

Specification	NANO-PV-D4252/N4552/D5252
Ethernet	One RJ-45 GbE ports
Serial Ports	One RS-232 serial port Three RS-232 via four 10-pin headers One RS-232/422/485 via 14–pin header
USB 2.0/1.1 Ports	Two external USB ports Six internal USB ports via three 8-pin headers
Parallel Ports	One LPT connector via 26-pin header
Storage	
Serial ATA	Two SATA 3Gb/s connectors with RAID 0,1 support One 5 V SATA power connector
CompactFlash®	One CompactFlash® Type II socket
Environmental and Power Specifications	
Power Supply	12 V only ATX and AT power supported
Power Connector	One internal 4-pin Molex power connector for power supply
Power Consumption	12V@2.21A (Intel® Atom™ D525 with 1GB 667MHz DDR3)
Operating Temperature	-10ºC ~ 60ºC (requires cooler and silicone heat sink paste)
Storage Temperature	-20ºC ~ 70ºC
Humidity	5% ~ 95% (non-condensing)
Physical Specifications	
Dimensions	165 mm x 115 mm
Weight GW/NW	850 g / 350 g

Table 1-1: Technical Specifications

Chapter

2

Unpacking

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband**: Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding**: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad**: When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB**: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the NANO-PV-D4252/N4552/D5252 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the NANO-PV-D4252/N4552/D5252 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The NANO-PV-D4252/N4552/D5252 is shipped with the following components:

Quantity	Item and Part Number	Image
1	NANO-PV-D4252/N4552/D5252 SBC	
1	SATA and 5 V power cable (**P/N:** 32801-000201-100-RS)	
1	KB/MS PS/2 Y-cable (**P/N**: 32006-000300-100-RS)	
2	RS-232 serial port cable (**P/N**: 32200-000049-RS)	
1	AT 12 V Cable (**P/N**: 32100-087100-RS)	
1	Audio cable (**P/N:** 32000-072100-RS)	
1	Dual USB cable (wo bracket) (**P/N**: 32000-044300-RS)	

1	Mini jumper pack (2.0mm) (**P/N**: 33100-000033-RS)	
1	Utility CD	
1	One Key Recovery CD	
1	Quick installation guide	
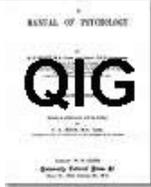
2.3.1 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
LPT cable (wo bracket) (**P/N**: 32200-015100-RS)	
RS-232/422/485 cable (**P/N**: 32200-026500-RS)	
CPU fan (**P/N**: 19FFD124010HB2A7-000001-RS)	
SATA cable (**P/N**: 32000-062800-RS)	

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 NANO-PV-D4252/N4552/D5252 Layout

The figures below show all the connectors and jumpers.
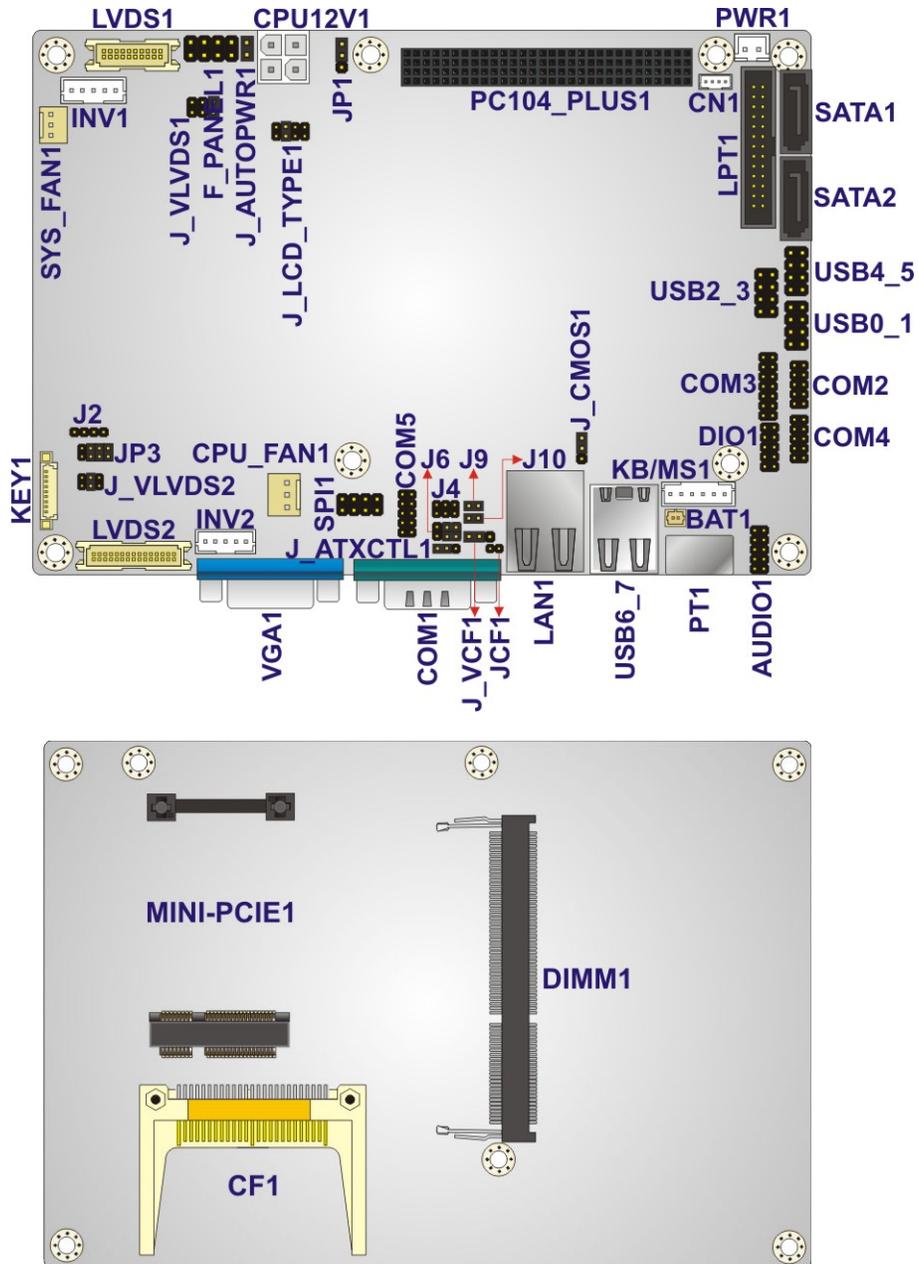
Figure 3-1: Connector and Jumper Locations

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
Audio connector	10-pin header	AUDIO1
Battery connector	2-pin wafer	BAT1
BIOS update connector	6-pin wafer	SPI1
CompactFlash® slot	50-pin header	CF1
DDR3 SO-DIMM socket	204-pin socket	DIMM1
Digital I/O connector	10-pin header	DIO1
Fan connector (CPU)	3-pin wafer	CPU_FAN1
Fan connector (system)	3-pin wafer	SYS_FAN1
Front panel connector	8-pin header	F_PANEL1
Keyboard and mouse connector	6-pin wafer	KB/MS1
LVDS1 backlight inverter connector	5-pin wafer	INV1
LVDS2 backlight inverter connector	5-pin wafer	INV2
LVDS2 backlight adjust connector	9-pin wafer	KEY1
LVDS1 LCD connector	30-pin crimp	LVDS1
LVDS2 LCD connector	20-pin crimp	LVDS2
Parallel port connector	26-pin header	LPT1
PCI-104 connector	PCI-104 connector	PC104_PLUS1
PCIe Mini card slot	PCIe Mini card slot	MINI_PCIE1
Power connector (+12V, power supply)	4-pin connector	CPU12V1
RS-232 serial port connector	10-pin header	COM2
RS-232 serial port connector	10-pin header	COM4
RS-232 serial port connector	10-pin header	COM5
RS-232/422/485 serial port connector	14-pin header	COM3

Serial ATA (SATA) drive connector	7-pin SATA	SATA1
Serial ATA (SATA) drive connector	7-pin SATA	SATA2
SATA power connector	2-pin wafer	PWR1
SMBus connector	4-pin wafer	CN1
USB connector	8-pin header	USB0_1
USB connector	8-pin header	USB2_3
USB connector	8-pin header	USB4_5

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

NOTE:

Due to limited space on the mainboard, the VGA and COM port on the I/O panel cannot be used simultaneously. To utilize both the VGA and COM port at the same time, please connect the RS-232 COM port cable to the mainboard pin-header. For convenience, the mainboard provides support for a maximum of four COM ports plus one VGA port or five COM ports without VGA setup.

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
Ethernet connector	RJ-45	LAN1
Keyboard/Mouse connector	PS/2	PT1
VGA port connector	15-pin Female	VGA1
Serial port (RS-232) connector	9-pin male	COM1
USB ports (dual)	USB port	USB6_7

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the NANO-PV-D4252/N4552/D5252.

3.2.1 Audio Connector

CN Label:	**AUDIO1**
CN Type:	10-pin header (2x5)
CN Location:	See **Figure 3-2**
CN Pinouts:	See **Table 3-3**

The audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.
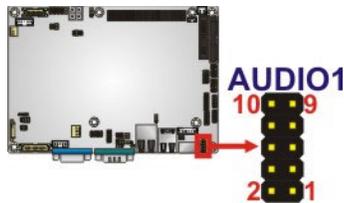
Figure 3-2: Audio Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LFRONT-R	2	LLINE-R
3	GND	4	GND
5	LFRONT-L	6	LLINE-L
7	GND	8	GND
9	LMIC1-CONN-R	10	LMIC1-CONN-L

Table 3-3: Audio Connector Pinouts

3.2.2 Battery Connector

⚠️ **CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

CN Label: **BAT1**

CN Type: 2-pin wafer (1x2)

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

This is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.
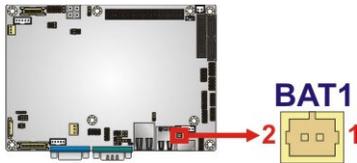
Figure 3-3: Battery Connector Location

Pin	Description
1	Battery+
2	Ground

Table 3-4: Battery Connector Pinouts

3.2.3 CompactFlash® Slot

CN Label: **CF1**

CN Type: CompactFlash® card slot

CN Location: See **Figure 3-4**

CN Pinouts: See **Table 3-5**

A CompactFlash® Type I/II card can be used in this slot.
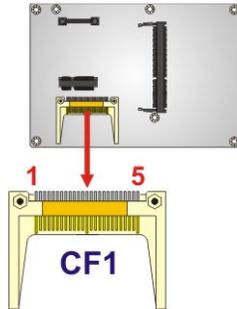
Figure 3-4: CompactFlash® Slot Location

Pin	Description	Pin	Description
1	GROUND	26	VCC-IN CHECK1
2	DATA 3	27	DATA 11
3	DATA 4	28	DATA 12
4	DATA 5	29	DATA 13
5	DATA 6	30	DATA 14
6	DATA 7	31	DATA 15
7	HDC_CS0#	32	HDC_CS1
8	GROUND	33	N/C
9	GROUND	34	IOR#
10	GROUND	35	IOW#
11	GROUND	36	VCC_CF
12	GROUND	37	IRQ14
13	VCC_CF	38	VCC_CF
14	GROUND	39	CSEL
15	GROUND	40	N/C
16	GROUND	41	HDD_RESET
17	GROUND	42	IORDY
18	SA2	43	SDREQ
19	SA1	44	SDACK#

Pin	Description	Pin	Description
20	SA0	45	HDD_ACTIVE#
21	DATA 0	46	66DET
22	DATA 1	47	DATA 8
23	DATA 2	48	DATA 9
24	N/C	49	DATA 10
25	VCC-IN CHECK2	50	GROUND

Table 3-5: CompactFlash® Slot Pinouts

3.2.4 Digital I/O Connector

CN Label: **DIO1**

CN Type: 10-pin header

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

The digital I/O connector provides programmable input and output for external devices. The digital I/O provides 4-bit output and 4-bit input.
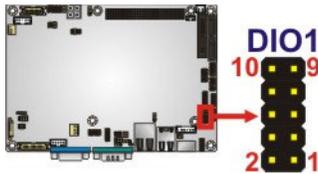
Figure 3-5: Digital I/O Connector Locations

Pin	Description	Pin	Description
1	GND	2	+5V
3	Output 3	4	Output 2
5	Output 1	6	Output 0
7	Input 3	8	Input 2
9	Input 1	10	Input 0

Table 3-6: Digital I/O Connector Pinouts

3.2.5 Fan Connector (CPU)

CN Label:	**CPU_FAN1**
CN Type:	3-pin wafer (1x3)
CN Location:	See **Figure 3-6**
CN Pinouts:	See **Table 3-7**

The fan connector attaches to a CPU cooling fan.
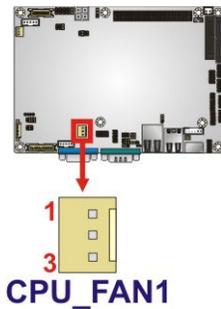
Figure 3-6: CPU Fan Connector Location

Pin	Description
1	FANIO1
2	POWER
3	GND

Table 3-7: CPU Fan Connector Pinouts

3.2.6 Fan Connector (System)

CN Label:	**SYS_FAN1**
CN Type:	3-pin wafer (1x3)
CN Location:	See **Figure 3-7**
CN Pinouts:	See **Table 3-8**

The cooling fan connector provides a 12V, 500mA current to the cooling fan. The connector has a "rotation" pin to get rotation signals from fans and notify the system so the system BIOS can recognize the fan speed. Please note that only specified fans can issue the rotation signals.
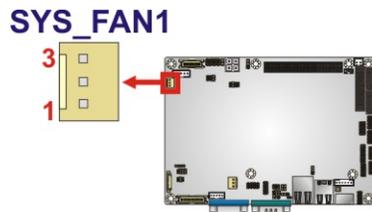
Figure 3-7: +12V Fan Connector Locations

PIN NO.	DESCRIPTION
1	FANIO2
2	+12V
3	GND

Table 3-8: +12V Fan Connector Pinouts

3.2.7 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 8-pin header (2x4)

CN Location: See **Figure 3-8**

CN Pinouts: See **Table 3-9**

The front panel connector connects to external switches and indicators to monitor and controls the motherboard. These indicators and switches include:

- Power button
- Reset
- Power LED
- HDD LED
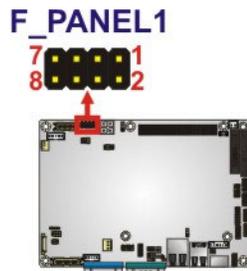
Figure 3-8: Front Panel Connector Location

FUNCTION	PIN	DESCRIPTION	FUNCTION	PIN	DESCRIPTION
Power Button	1	PWR_BTN+	Power LED	2	PWR LED
	3	GND		4	GND
SATA LED	5	SATA LED PWT	Reset	6	RESET
	7	SATA_LED#		8	GND

Table 3-9: Front Panel Connector Pinouts

3.2.8 Keyboard/Mouse Connector

CN Label: **KB/MS1**

CN Type: 6-pin wafer (1x6)

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-10**

The keyboard/mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.
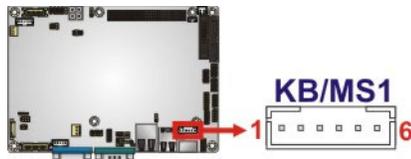
Figure 3-9: Keyboard/Mouse Connector Location

Pin	Description
1	+5 VCC
2	MS DATA
3	MS CLK
4	KB DATA
5	KB CLK
6	GROUND

Table 3-10: Keyboard/Mouse Connector Pinouts

3.2.9 Backlight Inverter Connector

CN Label: **INV1, INV2**

CN Type: 5-pin wafer (1x5)

CN Location: See **Figure 3-10**

CN Pinouts: See **Table 3-11**

The backlight inverter connector provides power to an LCD panel.
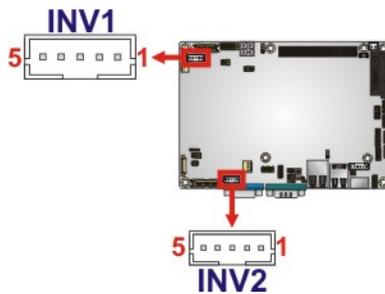
Figure 3-10: Backlight Inverter Connector Location

Pin	Description
1	BL_ADJ
2	GROUND
3	+12 V
4	GROUND
5	BACKLIGHT ENABLE

Table 3-11: Backlight Inverter Connector Pinouts

3.2.10 LVDS Backlight Adjustment (LVDS2)

CN Label: **KEY1**

CN Type: 9-pin header

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-12**

This connector allows adjustment of the LVDS2 backlight.
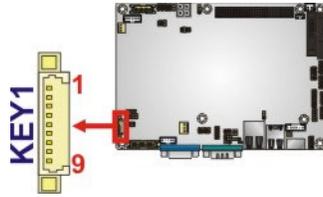
Figure 3-11: LVDS2 Backlight Adjustment Connector Location

Pin	Description	Pin	Description
1	LED-BL	2	N/A
3	LED-AM	4	menu/enter
5	DOWN	6	UP
7	auto/exit	8	POWER
9	GND		

Table 3-12: LVDS2 Backlight Adjustment Connector Pinouts

3.2.11 LVDS1 LCD Connector

CN Label: LVDS1

CN Type: 20-pin crimp (2x10)

CN Location: See **Figure 3-12**

CN Pinouts: See **Table 3-14**

The LVDS1 connector is for an LCD panel connected to the board.
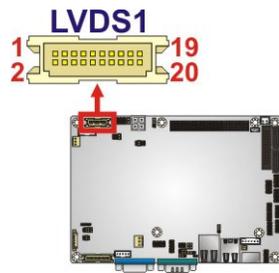
Figure 3-12: LVDS1 Connector Locations

Pin	Description	Pin	Description
1	GROUND	2	GROUND
3	LVDSA_DATA0+	4	LVDSA_DATA0-
5	LVDSA_DATA1+	6	LVDSA_DATA1-

Pin	Description	Pin	Description
7	LVDSA_DATA2+	8	LVDSA_DATA2-
9	LVDSA_CLK+	10	LVDSA_CLK-
11	N/C	12	N/C
13	GROUND	14	GROUND
15	LDDC_DATA	16	LDDC_CLK
17	VCC_LCD	18	VCC_LCD
19	VCC_LCD	20	VCC_LCD

Table 3-13: LVDS1 Connector Pinouts

3.2.12 LVDS2 LCD Connector

CN Label: **LVDS2**

CN Type: 30-pin crimp (2x15)

CN Location: See **Figure 3-13**

CN Pinouts: See **Table 3-13**

The LVDS2 connector is for an LCD panel connected to the board.

![NOTE icon] **NOTE:**

The extended mode is not supported when using LVDS2 and VGA connectors as dual display output. The user can only select the clone mode.
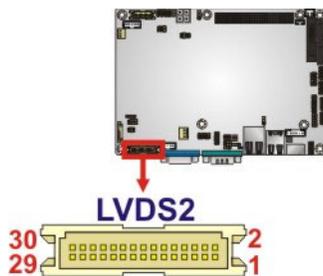
Figure 3-13: LVDS2 Connector Location

Pin	Description	Pin	Description
1	GROUND	2	GROUND
3	LVDSA_Y0+	4	LVDSA_Y0-
5	LVDSA_Y1+	6	LVDSA_Y1-
7	LVDSA_Y2+	8	LVDSA_Y2-
9	LVDSA_CLK+	10	LVDSA_CLK-
11	LVDSA_Y3+	12	LVDSA_Y3-
13	GROUND	14	GROUND
15	LVDSB_Y0+	16	LVDSB_Y0-
17	LVDSB_Y1+	18	LVDSB_Y1-
19	LVDSB_Y2+	20	LVDSB_Y2-
21	LVDSB_CLK+	22	LVDSB_CLK-
23	LVDSB_Y3+	24	LVDSB_Y3-
25	GROUND	26	GROUND
27	VCC_LVDS	28	VCC_LVDS
29	VCC_LVDS	30	VCC_LVDS

Table 3-14: LVDS2 Connector Pinouts

3.2.13 Parallel Port Connector

CN Label:	**LPT1**
CN Type:	26-pin box header
CN Location:	See **Figure 3-14**
CN Pinouts:	See **Table 3-15**

The parallel port connector connects to a parallel port connector interface or some other parallel port device such as a printer.
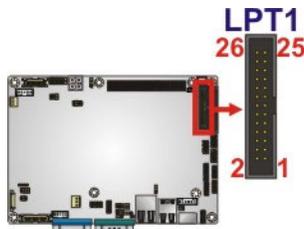
Figure 3-14: Parallel Port Connector Location

Pin	Description	Pin	Description
1	STROBE#	2	AFD
3	PTD0	4	ERROR#
5	PTD1	6	INITIALIZE
7	PTD 2	8	SLIN
9	PTD3	10	GROUND
11	PTD 4	12	GROUND
13	PTD 5	14	GROUND
15	PTD 6	16	GROUND
17	PTD7	18	GROUND
19	ACK	20	GROUND
21	BUSY	22	GROUND
23	PE	24	GROUND
25	SLCT	26	NC

Table 3-15: Parallel Port Connector Pinouts

3.2.14 PCI-104 Connector

CN Label: **PCI-104_PLUS1**

CN Type: PCI-104 connector

CN Location: See **Figure 3-15**

CN Pinouts: See **Table 3-16**

The PCI-104 connector is for installing a PCI-104 expansion card.
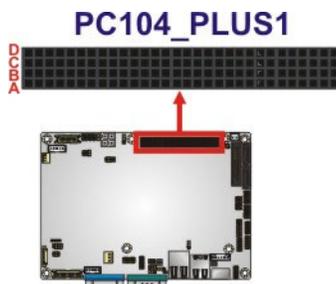
Figure 3-15: PCI-104 Connector Location

Pin	Row A	Row B	Row C	Row D
1	GND/5 V	TBD1	5 V	AD00
2	VI/O1	AD02	AD01	+5 V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O2	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3 V	C/BE1#	AD15	+3.3 V
9	SERR#	GND	SB0#	PAR
10	GND	PERR#	+3.3 V	SDONE
11	STOP#	+3.3 V	LOCK#	GND
12	+3.3 V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3 V
14	GND	AD16	+3.3 V	C/BE2#
15	AD18	+3.3 V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3 V	AD23	AD22	+3.3 V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O1	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 V	AD28	AD27
22	+5 V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O2
24	GND	REQ2#	+5 V	GNT0#
25	GNT1#	VI/O3	GNT2#	GND
26	+5 V	CLK0	GND	CLK1
27	CLK2	+5 V	CLK3	GND
28	GND	INTD#	+5 V	RST#
29	+12 V	INTA#	INTB#	INTC#
30	-12 V	TBD2	TBD	GND/3.3 V

Table 3-16: PCI-104 Connector Pinouts

3.2.15 PCIe Mini Card Slot

CN Label: **MINI-PCIE1**

CN Type: PCIe Mini card slot

CN Location: See **Figure 3-16**

CN Pinouts: See **Table 3-17**

The PCIe Mini card slot is for installing PCIe Mini expansion cards.
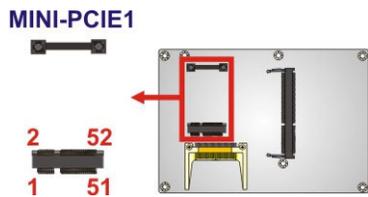
Figure 3-16: PCIe Mini Card Slot Location

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	VCC3
3	N/C	4	GND
5	N/C	6	1.5 V
7	CLKREQ#	8	LFRAME#
9	GND	10	LAD3
11	CLK-	12	LAD2
13	CLK+	14	LAD1
15	GND	16	LAD0
17	PCIRST#	18	GND
19	LPC	20	VCC3
21	GND	22	PCIRST#
23	PERN2	24	3VDual
25	PERP2	26	GND
27	GND	28	1.5 V
29	GND	30	SMBCLK
31	PETN2	32	SMBDATA
33	PETP2	34	GND
35	GND	36	USBD-

Pin	Description	Pin	Description
37	GND	38	USBD+
39	VCC3	40	GND
41	VCC3	42	N/C
43	GND	44	RF_LINK#
45	SATATXP1	46	BLUELED#
47	SATATXN1	48	1.5 V
49	SATARXN1	50	GND
51	SATARXP1	52	VCC3

Table 3-17: PCIe Mini Card Slot Pinouts

3.2.16 Power Connector (+12 V, power supply)

CN Label: **CPU12V1**

CN Type: 4-pin Molex power connector (1x4)

CN Location: See **Figure 3-17**

CN Pinouts: See **Table 3-18**

The connector supports the 12 V power supply.
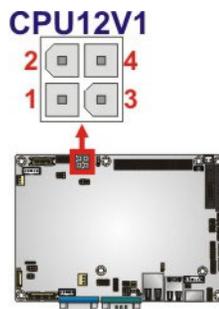
Figure 3-17: CPU 12V Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	+12V	4	+12V

Table 3-18: CPU 12V Power Connector Pinouts

3.2.17 SATA Drive Connectors

CN Label: **SATA1, SATA2**

CN Type: 7-pin SATA drive connectors

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-19**

The two SATA 3Gb/s drive connectors are each connected to a SATA 3Gb/s drive. The SATA 3Gb/s drives transfer data at speeds as high as 3.0 Gb/s.
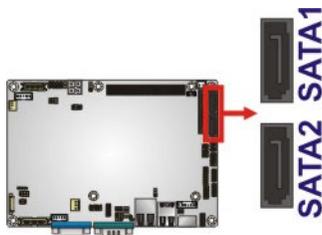
Figure 3-18: SATA Drive Connector Locations

PIN NO.	DESCRIPTION
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 3-19: SATA Drive Connector Pinouts

3.2.18 SATA Power Connector

CN Label: **PWR1**

CN Type: 2-pin wafer (1x2)

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-20**

The SATA Power Connector provides +5V power output to the SATA connectors.
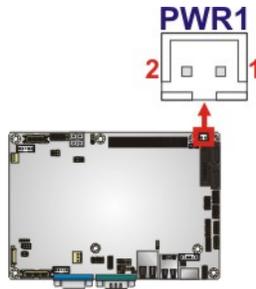
Figure 3-19: SATA Power Connector Locations

PIN NO.	DESCRIPTION
1	+5V
2	GND

Table 3-20: SATA Power Connector Pinouts

3.2.19 Serial Port Connectors (RS-232)

CN Label: **COM2, COM4, COM5**

CN Type: 10-pin header (2x5)

CN Location: See **Figure 3-20**

CN Pinouts: See **Table 3-21**

These connectors provide RS-232 communications.
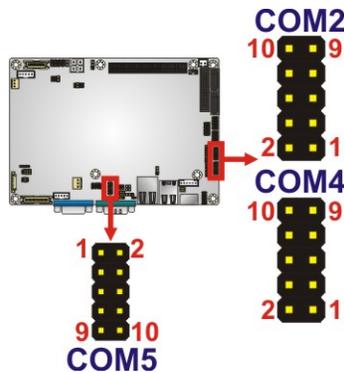
Figure 3-20: COM Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Data Carrier Direct (DCD)	2	Data Set Ready (DSR)
3	Receive Data (RXD)	4	Request To Send (RTS)

5	Transmit Data (TXD)	6	Clear To Send (CTS)
7	Data Terminal Ready (DTR)	8	Ring Indicator (RI)
9	Ground (GND)	10	GND

Table 3-21: COM Connector Pinouts

3.2.20 Serial Port Connector (RS-232/422/485)

CN Label: **COM3**

CN Type: 14-pin header (2x7)

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-22**

Used for RS-232/422/485 communications.
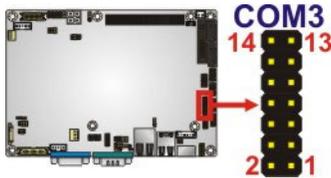
Figure 3-21: Serial Port Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR2
3	RXD	4	RTS2
5	TXD	6	CTS2
7	DTR	8	RI2
9	GND	10	N/A
11	RS422 TX2/485+	12	RS422 TX2/485-
13	RS422 RX2+	14	RS422 RX2-

Table 3-22: Serial Port Connector Pinouts

3.2.21 SMBus Connector

CN Label: **CN1**

CN Type: 4-pin wafer (1x4)

CN Location: See **Figure 3-19**

CN Pinouts: See **Table 3-20**

The SMBus Connector provides a connection to a SMBus (System Management Bus) device.

Figure 3-22: SMBus Connector Locations

PIN NO.	DESCRIPTION
1	GND
2	SMBDATA
3	SMBCLK
4	VCC5S

Table 3-23: SMBus Connector Pinouts

3.2.22 SPI Flash Connector

CN Label:	**SPI1**
CN Type:	8-pin header (2x4)
CN Location:	See **Figure 3-23**
CN Pinouts:	See **Table 3-24**

The 8-pin SPI Flash connector is used to flash the BIOS.
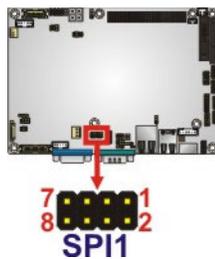
Figure 3-23: SPI Flash Connector

Pin	Description	Pin	Description
1	VCC	2	GND
3	CS#	4	CLOCK
5	SO	6	SI
7	NC	8	NC

Table 3-24: SPI Flash Connector Pinouts

3.2.23 USB Connectors

CN Label: **USB0_1, USB2_3, USB4_5**

CN Type: 8-pin header (2x4)

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-25**

The USB connectors connect to USB devices. Each pin header provides two USB ports.
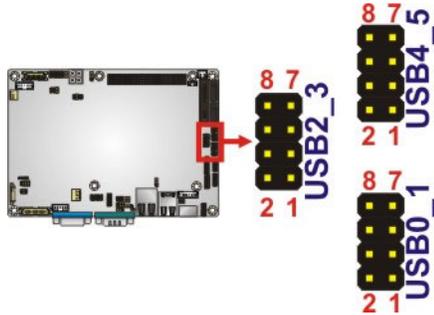
Figure 3-24: USB Connector Pinout Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	DATA-	4	DATA+
5	DATA+	6	DATA-
7	GND	8	VCC

Table 3-25: USB Port Connector Pinouts

3.3 External Peripheral Interface Connector Panel

Figure 3-25 shows the NANO-PV-D4252/N4552/D5252 external peripheral interface connector (EPIC) panel. The NANO-PV-D4252/N4552/D5252 EPIC panel consists of the following:

- 1 x Ethernet connector
- 1 x Keyboard/Mouse
- 1 x Serial port (RS-232)
- 2 x USB connectors
- 1 x VGA connector
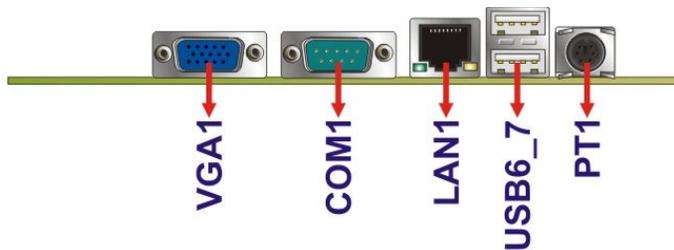
Figure 3-25: NANO-PV-D4252/N4552/D5252 External Peripheral Interface Connector

3.3.1 Ethernet Connector

CN Label: **LAN1**

CN Type: RJ-45

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-26**

The NANO-PV-D4252/N4552/D5252 is equipped with one built-in RJ-45 Ethernet controller. The controller can connect to the LAN through the RJ-45 LAN connector.

PIN	DESCRIPTION	PIN	DESCRIPTION
1	LAN1_MDI0P	2	LAN1_MDI0N
3	LAN1_MDI1P	4	LAN1_MDI1N
5	+VCT_LAN1	6	GND
7	LAN1_MDI2P	8	LAN1_MDI2N
9	LAN1_MDI3P	10	LAN1_MDI3N

Table 3-26: LAN Pinouts

The RJ-45 Ethernet connector has two status LEDs, one green and one yellow. The green LED indicates activity on the port and the yellow LED indicates the speed. See **Table 3-27**.

Speed LED		Activity/Link LED	
STATUS	**DESCRIPTION**	**STATUS**	**DESCRIPTION**
Off	10 Mbps connection	Off	No link
Green	100 Mbps connection	Yellow	Linked
Orange	Gbps connection	Blinking	TX/RX activity 1

Table 3-27: RJ-45 Ethernet Connector LEDs

Figure 3-26: RJ-45 Ethernet Connector

3.3.2 Keyboard/Mouse Connector

CN Label: **PT1**

CN Type: PS/2

CN Location: See **Figure 3-25**

CN Pinouts: See **Figure 3-27** and **Table 3-28**

The keyboard and mouse connector is a standard PS/2 connector.
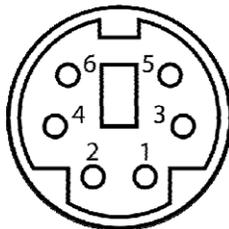
Figure 3-27: PS/2 Pinout and Configuration

Pin	Description
1	KB DATA
2	MS DATA
3	GND
4	VCC
5	KB CLOCK
6	MS CLOCK

Table 3-28: Keyboard Connector Pinouts

3.3.3 USB Connectors

CN Label: **USB6_7**

CN Type: USB port

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-29**

The NANO-PV-D4252/N4552/D5252 has four external USB 2.0 ports. The ports connect to both USB 2.0 and USB 1.1 devices.

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	5	VCC
2	DATA-	6	DATA-
3	DATA+	7	DATA+
4	GROUND	8	GROUND

Table 3-29: USB Port Connector Pinouts

3.3.4 VGA Connector

CN Label:	**VGA1**
CN Type:	15-pin Female
CN Location:	See **Figure 3-25**
CN Pinouts:	See **Figure 3-28** and **Table 3-30**

Connects to a monitor that accepts a standard VGA input.

NOTE:

The extended mode is not supported when using LVDS2 and VGA connectors for dual display output. The user can only select the clone mode.
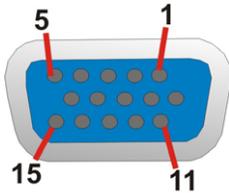
Figure 3-28: VGA Connector

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RED	2	GREEN
3	BLUE	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC / NC	10	GND
11	NC	12	DDC DAT
13	HSYNC	14	VSYNC
15	DDCCLK		

Table 3-30: VGA Connector Pinouts

Chapter

4

Installation

4.1 Anti-static Precautions

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the NANO-PV-D4252/N4552/D5252. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the NANO-PV-D4252/N4552/D5252 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband**: Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding**: Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad**: When configuring the NANO-PV-D4252/N4552/D5252, place it on an anti-static pad. This reduces the possibility of ESD damaging the NANO-PV-D4252/N4552/D5252.
- **Only handle the edges of the PCB**: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

![NOTE icon] **NOTE:**

The following installation notices and installation considerations should be read and understood before the NANO-PV-D4252/N4552/D5252 is installed. All installation notices pertaining to the installation of the NANO-PV-D4252/N4552/D5252 should be strictly adhered to. Failing to adhere to these precautions may lead to severe damage of the NANO-PV-D4252/N4552/D5252 and injury to the person installing the motherboard.

4.2.1 Installation Notices

![WARNING icon] **WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the NANO-PV-D4252/N4552/D5252, NANO-PV-D4252/N4552/D5252 components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  o The user manual provides a complete description of the NANO-PV-D4252/N4552/D5252 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  o Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the NANO-PV-D4252/N4552/D5252 on an anti-static pad:
  o When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.

- Turn all power to the NANO-PV-D4252/N4552/D5252 off:
  - o When working with the NANO-PV-D4252/N4552/D5252, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the NANO-PV-D4252/N4552/D5252 **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 Unpacking

When the NANO-PV-D4252/N4552/D5252 is unpacked, please check all the unpacking list items listed in Chapter 3 are indeed present. If any of the unpacking list items are not available please contact the NANO-PV-D4252/N4552/D5252 vendor reseller/vendor where the NANO-PV-D4252/N4552/D5252 was purchased or contact an IEI sales representative.

4.4 SO-DIMM Installation

SO-DIMM is a critical component of the NANO-PV-D4252/N4552/D5252. If it is not installed the NANO-PV-D4252/N4552/D5252 cannot run.

To install an SO-DIMM, please follow the steps below and refer to **Figure 4-1**.
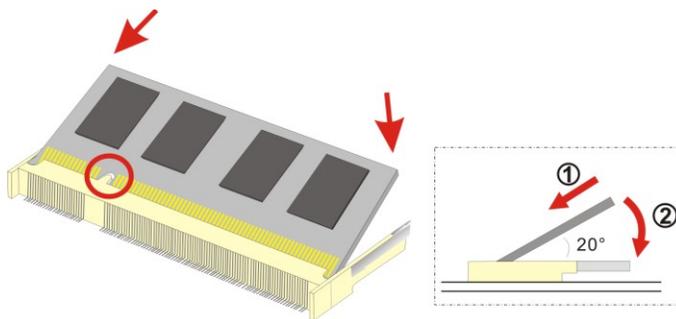
Figure 4-1: SO-DIMM Installation

Step 1: **Locate the SO-DIMM socket**. Place the board on an anti-static mat.

Step 2: **Align the SO-DIMM with the socket**. Align the notch on the memory with the notch on the memory socket.

Step 3: **Insert the SO-DIMM**. Push the memory in at a 20º angle. (See **Figure 4-1**)

Step 4: **Seat the SO-DIMM**. Gently push downwards and the arms clip into place. (See **Figure 4-1**)

4.5 Jumper Settings

NOTE:

A jumper is a metal bridge used to close an electrical circuit. It consists of two or three metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To CLOSE/SHORT a jumper means connecting the pins of the jumper with the plastic clip and to OPEN a jumper means removing the plastic clip from a jumper.
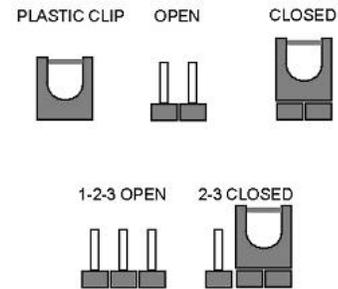
Before the NANO-PV-D4252/N4552/D5252 is installed in the system, the jumpers must be set in accordance with the desired configuration. The jumpers on the NANO-PV-D4252/N4552/D5252 are listed in **Table 4-1**.

Description	Type	Label
AT Auto Button	2-pin header	J_AUTOPWR1
Clear CMOS	3-pin header	J_CMOS1
CompactFlash® Master/Slave function setting	2-pin header	JCF1
CompactFlash® voltage select	3-pin header	J_VCF1
COM3 RS-232/422/485 select	6-pin header	J4
COM3 RS-422/485 select	6-pin header	J6

COM3 RS-422 Termination select	2-pin header	J10
COM3 RS-485 Termination select	2-pin header	J9
LVDS1 LCD Voltage select	6-pin header	J_VLVDS1
LVDS2 LCD Voltage select	6-pin header	J_VLVDS2
LVDS1 LCD panel type	8-pin header	J_LCD_TYPE1
LVDS2 LCD panel type	8-pin header	JP3

Table 4-1: Jumpers

4.5.1 AT Auto Button Power Select Jumper Settings

Jumper Label: J_AUTOPWR1

Jumper Type: 2-pin header

Jumper Settings: See **Table 4-2**

Jumper Location: See **Figure 4-2**

The AT Auto Button Power Select jumper specifies the systems auto button power mode as AT or ATX.

Setting	Description
Short	Use AT power
Open	Use ATX power

Table 4-2: AT Auto Button Power Select Jumper Settings
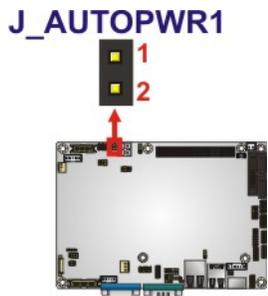
Figure 4-2: AT Auto Button Select Jumper Settings

4.5.2 AT/ATX Power Select Jumper Settings

Jumper Label: **J_ATXCTL1**

Jumper Type: 3-pin header (1x3)

Jumper Settings: See **Table 4-3**

Jumper Location: See **Figure 4-3**

The AT/ATX Power Select jumper specifies the systems power mode as AT or ATX. AT/ATX Power Select jumper settings are shown in **Table 4-3**.

AT Power Select	Description	
Short 1 - 2	Use ATX power	
Short 2 – 3	Use AT power	Default

Table 4-3: AT/ATX Power Select Jumper Settings

The location of the AT/ATX Power Select jumper is shown in **Figure 4-3** below.
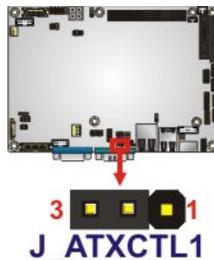
Figure 4-3: AT/ATX Power Select Jumper Location

4.5.3 Clear CMOS Jumper

Jumper Label: **J_CMOS1**

Jumper Type: 3-pin header (1x3)

Jumper Settings: See **Table 4-4**

Jumper Location: See **Figure 4-4**

If the NANO-PV-D4252/N4552/D5252 fails to boot due to improper BIOS settings, the clear CMOS jumper clears the CMOS data and resets the system BIOS information. To do

this, use the jumper cap to close pins 2 and 3 for a few seconds then reinstall the jumper clip back to pins 1 and 2.

If the "CMOS Settings Wrong" message is displayed during the boot up process, the fault may be corrected by pressing the F1 to enter the CMOS Setup menu.   Do one of the following:

- Enter the correct CMOS setting
- Load Optimal Defaults
- Load Failsafe Defaults.

After having done one of the above, save the changes and exit the CMOS Setup menu.

The clear CMOS jumper settings are shown in **Table 4-4**.

Clear CMOS	Description	
Short 1 - 2	Keep CMOS Setup	Default
Short 2 - 3	Clear CMOS Setup	

Table 4-4: Clear CMOS Jumper Settings

The location of the clear CMOS jumper is shown in **Figure 4-4** below.
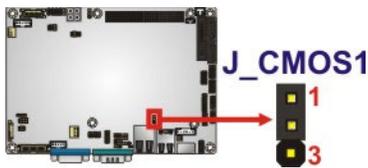
Figure 4-4: Clear CMOS Jumper

4.5.4 COM 3 Function Select Jumper

Jumper Label: J4

Jumper Type: 6-pin header

Jumper Settings: See Table 4-5

Jumper Location: See Figure 4-5

The COM 3 Function Select jumper sets the communication protocol used by the second serial communications port (COM 3) as RS-232, RS-422 or RS-485. The COM 3 Function Select settings are shown below.

Setting	Description
1-2	RS-232
3-4	RS-422
5-6	RS-485

Table 4-5: COM 3 Function Select Jumper Settings
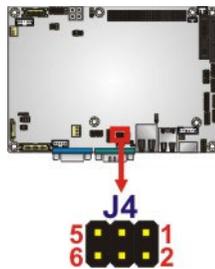
Figure 4-5: COM 3 Function Select Jumper Location

4.5.5 COM 3 RS-422/485 Function Select Jumper

Jumper Label: J6

Jumper Type: 6-pin header

Jumper Settings: See Table 4-5

Jumper Location: See Figure 4-5

The COM 3 Function Select jumper sets the communication protocol used by the second serial communications port (COM 3) as RS-422 or RS-485. The COM 3 Function Select settings are shown below.

Setting	Description
1-3, 2-4	RS-422
3-5, 4-6	RS-485

Table 4-6: COM 3 RS-422/485 Function Select Jumper Settings
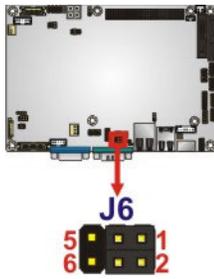
Figure 4-6: COM 3 RS-422/485 Function Select Jumper Location

4.5.6 COM 3 RS-422/485 Termination Select Jumpers

Jumper Label:	**J9 and J10**
Jumper Type:	2-pin header
Jumper Settings:	See **Table 4-5** and **Table 4-7**
Jumper Location:	See **Figure 4-7**

The COM 3 RS-422 and RS-485 Termination Select jumpers enable or disable the termination used by the serial COM 3 communications port as 120 ohm. The COM 3 RS-422 and RS-485 Termination Select settings are shown in **Table 4-5 and Table 4-7**.

RS-422 (J9) Setting	Description
Short	120 ohm termination Resistance
Open	NC (Default)

Table 4-7: COM 3 RS-422 Termination Select Jumper Settings

RS-485 (J10) Setting	Description
Short	120 ohm termination Resistance
Open	NC (Default)

Table 4-8: COM 3 RS-485 Termination Select Jumper Settings
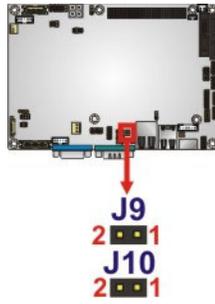
Figure 4-7: COM 3 RS-422 and RS-485 Termination Select Jumper Location

4.5.7 CompactFlash® Card Setup

Jumper Label: JCF1

Jumper Type: 2-pin header

Jumper Settings: See **Table 4-9**

Jumper Location: See **Figure 4-4**

The CompactFlash® slot is connected through an IDE connection. This jumper sets the CompactFlash® card as the master or slave IDE device.

Setting	Description
Open	Slave
Closed	Master

Table 4-9: CompactFlash® Setup Jumper Settings
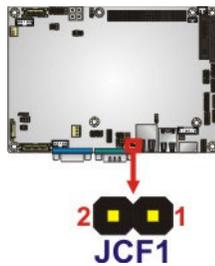
Figure 4-8: CompactFlash® Setup Jumper Location

4.5.8 CompactFlash® Voltage Selection

![Warning icon] **WARNING:**

Incorrect voltages can destroy the CF card. Make sure to select a voltage that matches the voltage required by the CF card.

Jumper Label: J_VCF1

Jumper Type: 3-pin header

Jumper Settings: See **Table 4-10**

Jumper Location: See **Figure 4-9**

The CompactFlash® voltage selection jumper sets the voltage of the power supplied to the CF card.

Setting	Description
Short 1-2	+5 V
Short 2-3	+3.3 V

Table 4-10: CompactFlash® Voltage Selection Jumper Settings
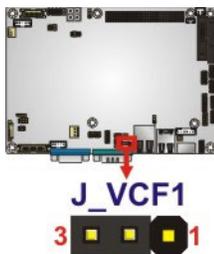
Figure 4-9: CompactFlash® Voltage Selection Jumper Location

4.5.9 LVDS1 Screen Resolution Selection

Jumper Label: J_LCD_TYPE1

Jumper Type: 8-pin header

Jumper Settings: See **Table 4-11**

Jumper Location: See **Figure 4-10**

The **LVDS1 Screen Resolution Selection** jumper allows the LVDS screen voltage to be set. The **LVDS1 Screen Resolution Selection** jumper settings are shown in Table 4-13.

Resolution	Pin 1-2	Pin 3-4	Pin 5-6	Pin 7-8
640 x 480 (18-bit)	Open	Open	Open	Open
800 x 480 (18-bit)	Short	Open	Open	Open
800 x 600 (18-bit)	Open	Short	Open	Open
1024 x 768 (18-bit)	Short	Short	Open	Open
1280 x 1024 (18-bit)	Open	Open	Short	Open
1366 x 768 (18-bit)	Short	Open	Short	Open
1280 x 800 (18-bit)	Open	Short	Short	Open
1280 x 600 (18-bit)	Short	Short	Short	Open

Table 4-11: LVDS1 Screen Resolution Jumper Settings
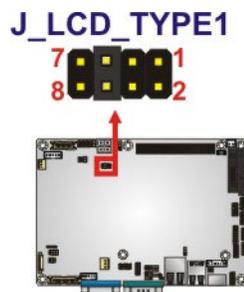
Figure 4-10: LVDS1 Screen Resolution Jumper Location

4.5.10 LVDS2 Screen Resolution Selection

Jumper Label: JP3

Jumper Type: 8-pin header

Jumper Settings: See **Table 4-13**

Jumper Location: See **Figure 4-12**

The **LVDS2 Screen Resolution Selection** jumper allows the LVDS2 screen voltage to be set. The **LVDS2 Screen Resolution Selection** jumper settings are shown in Table 4-13.

Resolution	Pin 1-2	Pin 3-4	Pin 5-6	Pin 7-8
800 x 600 (18-bit)	Short	Open	Open	Open
1024 x 768 (18-bit)	Open	Short	Open	Open

Resolution	Pin 1-2	Pin 3-4	Pin 5-6	Pin 7-8
1280 x 1024 (24-bit)	Short	Short	Open	Open
1366 x 768 (24-bit)	Open	Open	Short	Open
1920 x 1080 (24-bit)	Short	Open	Short	Open

Table 4-12: LVDS2 Screen Resolution Jumper Settings
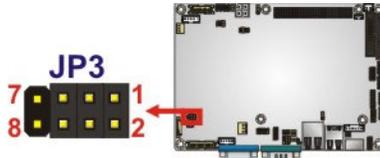
Figure 4-11: LVDS2 Screen Resolution Jumper Location

4.5.11 LVDS Voltage Selection

WARNING:

Incorrect voltages can destroy the LCD panel. Make sure to select a voltage that matches the voltage required by the LCD panel.

Jumper Label: J_VLVDS1, J_VLVDS2

Jumper Type: 6-pin header

Jumper Settings: See **Table 4-13**

Jumper Location: See **Figure 4-12**

The LCD voltage selection jumper sets the voltage of the power supplied to the LCD panel.

Setting	Description
1-2	+3.3 V (Default)
3-4	+5.0 V
5-6	+12 V

Table 4-13: LVDS Voltage Selection Jumper Settings
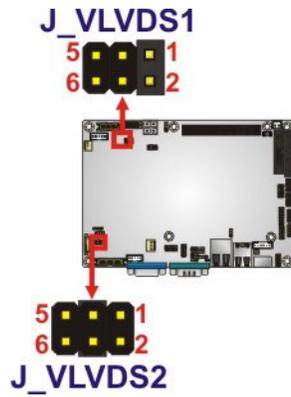
Figure 4-12: LVDS Voltage Selection Jumper Locations

4.5.12 PCI-104 Voltage Setup

Jumper Label:	**JP1**
Jumper Type:	3-pin header
Jumper Settings:	See **Table 4-14**
Jumper Location:	See **Figure 4-13**

This jumper selects the voltage supplied to the PCI-104 expansion module.

Setting	Description
1-2	+5.0 V
2-3	+3.3 V

Table 4-14: PCI-104 Voltage Jumper Settings
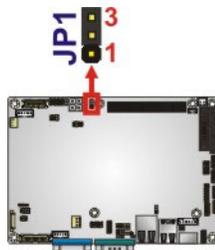
Figure 4-13: PCI-104 Voltage Jumper Location

4.6 Chassis Installation

4.6.1 Airflow

WARNING:

Airflow is critical to the cooling of the CPU and other onboard components. The chassis in which the NANO-PV-D4252/N4552/D5252 must have air vents to allow cool air to move into the system and hot air to move out.

The NANO-PV-D4252/N4552/D5252 must be installed in a chassis with ventilation holes on the sides allowing airflow to travel through the heat sink surface. In a system with an individual power supply unit, the cooling fan of a power supply can also help generate airflow through the board surface.

4.6.2 Motherboard Installation

To install the NANO-PV-D4252/N4552/D5252 motherboard into the chassis please refer to the reference material that came with the chassis.

4.7 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors

4.7.1 AT/ATX Power Connection

Follow the instructions below to connect the NANO-PV-D4252/N4552/D5252 to an AT or ATX power supply.

![WARNING icon] **WARNING:**

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the NANO-PV-D4252/N4552/D5252.

Step 1: **Locate the power cable**. The power cable is shown in the packing list in **Chapter 3**.

Step 2: **Connect the Power Cable to the Motherboard**. Connect the 4-pin (2x2) Molex type power cable connector to the AT/ATX power connector on the motherboard. See Figure 4-14.
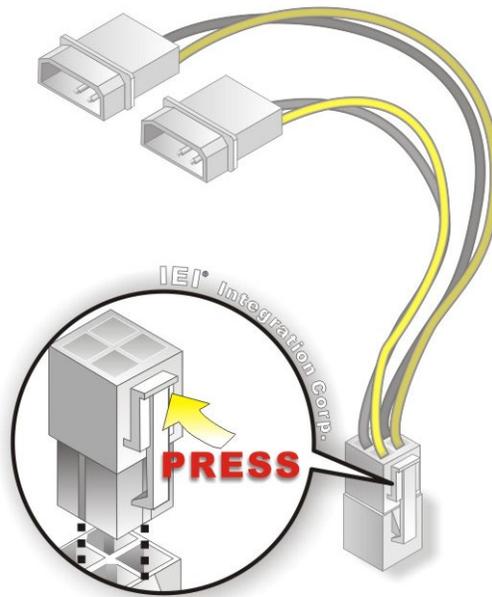
Figure 4-14: Power Cable to Motherboard Connection

Step 3: **Connect Power Cable to Power Supply**. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT/ATX power supply. See Figure 4-15.
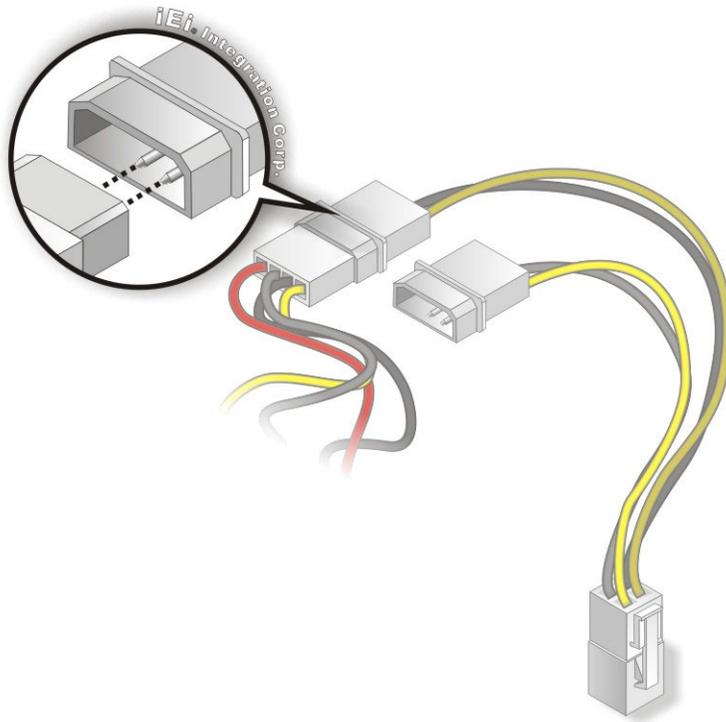
Figure 4-15: Connect Power Cable to Power Supply

4.7.2 Audio Kit Installation

The Audio Kit that came with the NANO-PV-D4252/N4552/D5252 connects to the audio connector on the NANO-PV-D4252/N4552/D5252. The audio kit consists of three audio jacks. Mic-in connects to a microphone. Line-in provides a stereo line-level input to connect to the output of an audio device. Line-out, a stereo line-level output, connects to two amplified speakers. To install the audio kit, please refer to the steps below:

Step 1: **Locate the audio connector**. The location of the 10-pin audio connector is

shown in **Chapter 3**.

Step 2: **Align pin 1**. Align pin 1 on the on-board connector with pin 1 on the audio kit

connector. Pin 1 on the audio kit connector is indicated with a white dot. See

Figure 4-16.
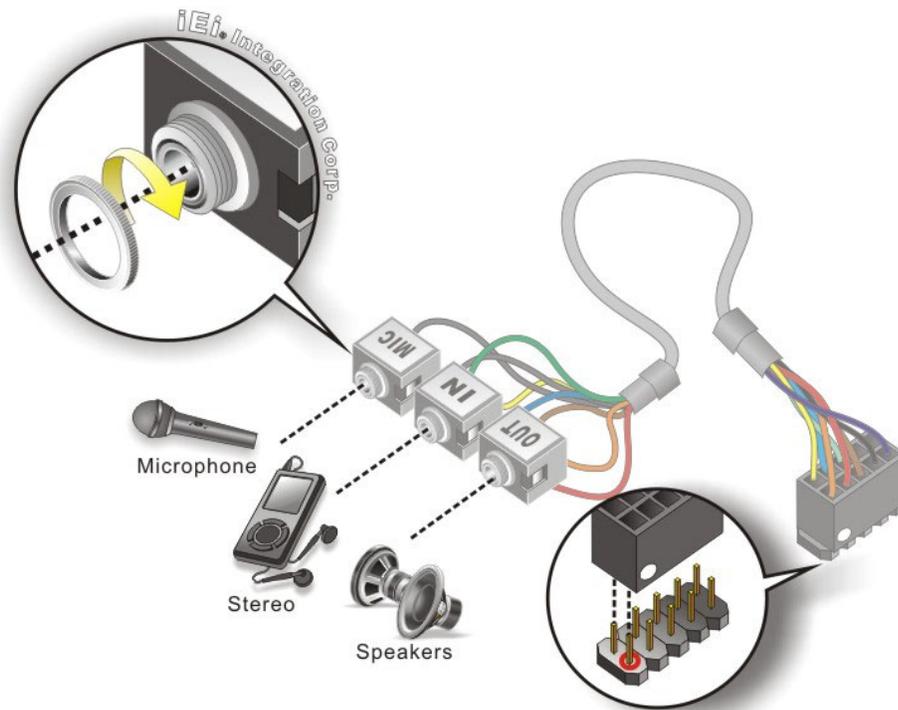
Figure 4-16: Audio Kit Cable Connection

Step 3: **Connect the audio devices**. Connect speakers to the line-out audio jack.

Connect the output of an audio device to the line-in audio jack. Connect a

microphone to the mic-in audio jack.

4.7.3 Single RS-232 Cable (w/o Bracket)

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

Step 1: **Locate the connector**. The location of the RS-232 connector is shown in

Chapter 3.

Step 2: **Insert the cable connector**. Insert the connector into the serial port box header.

See Figure 4-17. A key on the front of the cable connectors ensures the

connector can only be installed in one direction.
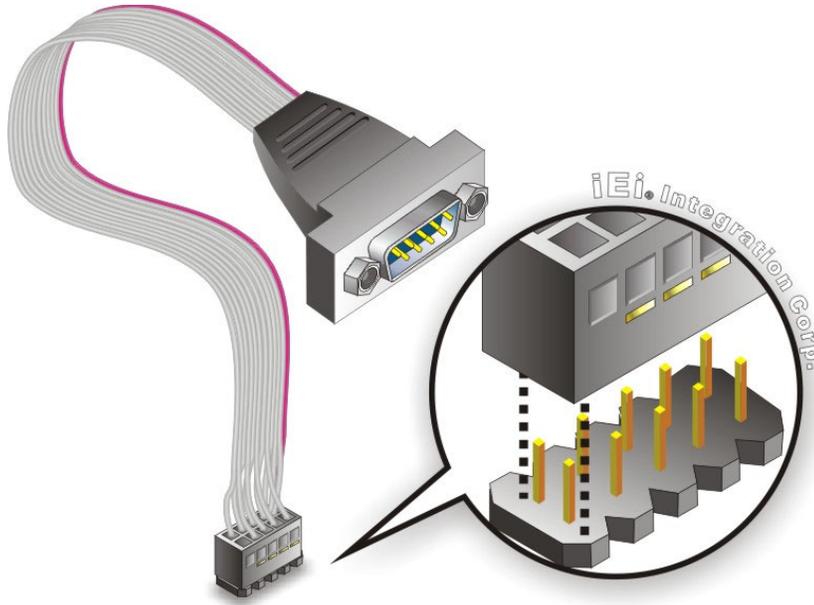
Figure 4-17: Single RS-232 Cable Installation

Step 3: **Secure the bracket**. The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.

Step 4: **Connect the serial device**. Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

4.8 Software Installation

All the drivers for the NANO-PV-D4252/N4552/D5252 are on the CD that came with the system. To install the drivers, please follow the steps below.

Step 1: Insert the CD into a CD drive connected to the system.

![NOTE icon] **NOTE:**

If the installation program doesn't start automatically:

Click "Start->My Computer->CD Drive->autorun.exe"

Step 2: The driver main menu appears (**Figure 4-18**).
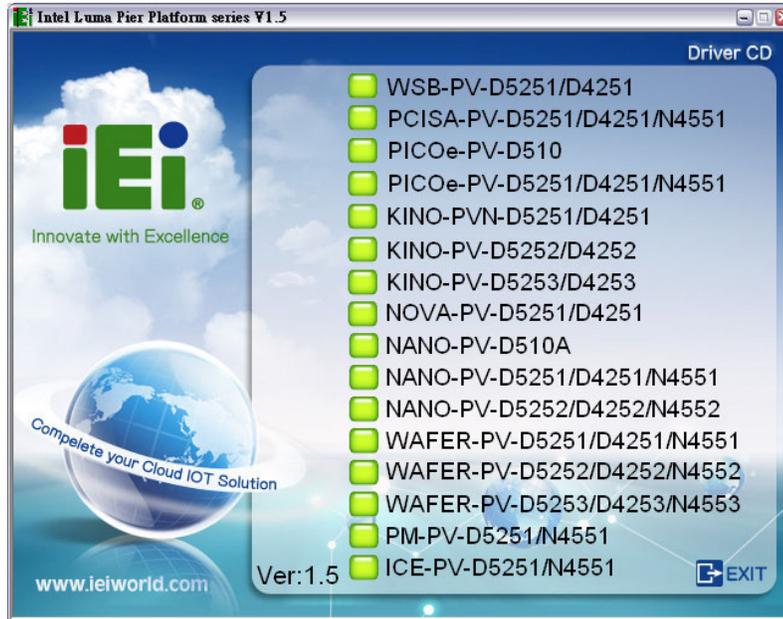
Figure 4-18: Introduction Screen

Step 3: Click **NANO-PV-D5252/D4252/N4552**.

Step 4: A new screen with a list of available drivers appears (**Figure 4-19**).

Figure 4-19: Available Drivers

Step 5: Install all of the necessary drivers in this menu.

Chapter

5

BIOS Screens

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The AMI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DEL** or **F2** key as soon as the system is turned on or
2. Press the **DEL** or **F2** key when the "**Press DEL or F2 to enter SETUP**" message appears on the screen.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press ENTER to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press ESC to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes

Key	Function
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu

Table 5-1: BIOS Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press **Esc**.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in Chapter **4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Boot – Changes the system boot configuration.
- Security – Sets User and Supervisor Passwords.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered. The **Main** menu gives an overview of the basic system information.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
   Main     Advanced   Chipset     Boot    Security  Save & Exit

BIOS Information                                            Set the Time. Use Tab to
BIOS Vendor                      American Megatrends        switch between Time
Core Version                     4.6.4.0 0.20               elements.
Compliency                       UEFI 2.0
Project Version                  SA24AR12.ROM
Build Date                       10/05/2010 20:29:21        ----------------------
                                                            →←: Select Screen
                                                            ↑ ↓: Select Item
System Date                      [Fri 12/10/2010]           Enter: Select
System Time                      [14:20:27]                 +/-:  Change Opt.
                                                            F1:  General Help
Access Level                     Administrator              F2:  Previous Values
                                                            F3:  Optimized Defaults
                                                            F4:  Save & Exit
                                                            ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 1: Main

➔ **BIOS Information**

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Project Version:** the board version
- **Build Date:** Date the current BIOS version was made

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:

⚠ **WARNING!**

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

```
        Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
   Main    Advanced   Chipset    Boot    Security  Save & Exit

 > ACPI Settings                                        System ACPI Parameters
 > Trusted Computing
 > CPU Configuration
 > IDE Configuration
 > USB Configuration                                    ----------------------
 > Super IO Configuration                               →←: Select Screen
 > H/W Monitor                                          ↑ ↓: Select Item
 > Serial Port Console Redirection                      Enter: Select
                                                        +/-:  Change Opt.
                                                        F1:   General Help
                                                        F2:   Previous Values
                                                        F3:   Optimized Defaults
                                                        F4:   Save & Exit
                                                        ESC: Exit

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 2: Advanced

5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.

```
      Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
          Advanced

ACPI Sleep State               [S1 (CPU Stop Clock)]   Select the highest ACPI
                                                       sleep state the system
                                                       will enter, when the
                                                       SUSPEND button is
                                                       pressed.

                                                       ----------------------
                                                       →←: Select Screen
                                                       ↑ ↓: Select Item
                                                       Enter: Select
                                                       +/-:  Change Opt.
                                                       F1:   General Help
                                                       F2:   Previous Values
                                                       F3:   Optimized Defaults
                                                       F4:   Save & Exit
                                                       ESC: Exit

      Version 2.01.1204. Copyright (C) 2010 American Megatrends, Inc.
```
   BIOS Menu 3: ACPI Settings

➔ **ACPI Sleep State [S1 (CPU Stop Clock)]**

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

➔ **Suspend Disabled**

➔ **S1 (CPU Stop Clock)** DEFAULT | The system enters S1 (POS) sleep state. The system appears off. The CPU is stopped; RAM is refreshed; the system is running in a low power mode.

➔ **S3 (Suspend to RAM)** | The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.2 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 4**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).

```
         Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
           Advanced

TPM Configuration                                      Enables or Disables TPM
  TPM SUPPORT                         [Disable]        support. O.S. will not
                                                       show TPM. Reset of
Current TPM Status Information                         platform is required.
  NO TPM Hardware

                                                       ----------------------
                                                       →←: Select Screen
                                                       ↑↓: Select Item
                                                       Enter: Select
                                                       +/-:  Change Opt.
                                                       F1:   General Help
                                                       F2:   Previous Values
                                                       F3:   Optimized Defaults
                                                       F4:   Save & Exit
                                                       ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 4: TPM Configuration

➔ **TPM Support [Disable]**

Use the **TPM Support** option to configure support for the TPM.

➔ **Disable** DEFAULT TPM support is disabled.

➔ **Enable** TPM support is enabled.

5.3.3 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 5**) to view detailed CPU specifications and configure the CPU.

```
          Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
            Advanced

CPU Configuration

Processor Type                  Intel(R) Atom(TM) CPU
                                CPU N475    @ 1.83GHz    ---------------------
EMT64                           Supported                →←: Select Screen
Processor Speed                 1834 MHz                 ↑ ↓: Select Item
System Bus Speed                667 MHz                  Enter: Select
Ratio Status                    11                       +/-:  Change Opt.
Actual Ratio                    11                       F1:   General Help
Processor Stepping              106ca                    F2:   Previous Values
Microcode Revision              263                      F3:   Optimized Defaults
L1 Cache RAM                    56 k                      F4:   Save & Exit
L2 Cache RAM                    512 k                     ESC: Exit
Processor Core                  Single
Hyper-Threading                 Supported

          Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 5: CPU Configuration

The CPU Configuration menu (**BIOS Menu 5**) lists the following CPU details:

- Processor Type: Lists the brand name of the CPU being used
- EMT64: Indicates if the EM64T is supported by the CPU.
- Processor Speed: Lists the CPU processing speed
- System Bus: Lists the system bus
- Ratio Status: List the maximum FSB divisor
- Actual Ratio: Lists current FSB divisor
- Processor Stepping: Lists the CPU processing stepping
- Microcode Revision: Lists the microcode revision
- L1 Cache RAM: Lists the CPU L1 cache size
- L2 Cache RAM: Lists the CPU L2 cache size
- Processor Core: Lists the number of the processor core
- Hyper-Threading: Indicates if the Intel Hyper-Threading Technology is supported by the CPU.

5.3.4 IDE Configuration

Use the **IDE Configuration** menu (**BIOS Menu 6**) to change and/or set the configuration of the SATA devices installed in the system.

```
           Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
             Advanced

 PATA Master                      Not Present          Select ATA/IDE
 PATA Slave                       Not Present          Configuration.

 SATA Port0                       Not Present
 SATA Port1                       Not Present          --------------------
 SATA Port2                       Not Present          →←: Select Screen
 SATA Port3                       Not Present          ↑ ↓: Select Item
                                                       Enter: Select
 ATA/IDE Configuration            [Enhanced]           +/-:  Change Opt.
   Configure SATA as              [IDE]                F1:   General Help
                                                       F2:   Previous Values
                                                       F3:   Optimized Defaults
                                                       F4:   Save & Exit
                                                       ESC: Exit

           Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
BIOS Menu 6: IDE Configuration

➔ **ATA/IDE Configurations [Enhanced]**

Use the **ATA/IDE Configurations** option to configure the ATA/IDE controller.

➔ **Disabled**   Disables the on-board ATA/IDE controller.

➔ **Compatible**   Configures the on-board ATA/IDE controller to be in compatible mode. In this mode, a SATA channel will replace one of the IDE channels. This mode supports up to 4 storage devices.

➔ **Enhanced**   DEFAULT   Configures the on-board ATA/IDE controller to be in Enhanced mode. In this mode, IDE channels and SATA channels are separated. This mode supports up to 6 storage devices. Some legacy OS do not support this mode.

➔ **Configure SATA as [IDE]**

Use the **Configure SATA as** option to configure SATA devices as normal IDE devices.

➔ **IDE**   DEFAULT   Configures SATA devices as normal IDE device.

➔ **AHCI**   Configures SATA devices as AHCI device.

5.3.5 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 7**) to read USB configuration information and configure the USB settings.

```
        Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
         Advanced

USB Configuration                                    Enables Legacy USB
                                                     support. AUTO option
USB Devices:                                         disables legacy support
        1 Keyboard                                   if no USB devices are
                                                     connected. DISABLE
Legacy USB Support                [Enabled]          option will keep USB
                                                     devices available only
                                                     for EFI applications.

                                                     --------------------
                                                     →←: Select Screen
                                                     ↑↓: Select Item
                                                     Enter: Select
                                                     +/-:  Change Opt.
                                                     F1:  General Help
                                                     F2:  Previous Values
                                                     F3:  Optimized Defaults
                                                     F4:  Save & Exit
                                                     ESC: Exit

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
BIOS Menu 7: USB Configuration

➔ **USB Devices**

The **USB Devices Enabled** field lists the USB devices that are enabled on the system

➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

➔ **Enabled** DEFAULT Legacy USB support enabled

➔ **Disabled** Legacy USB support disabled

➔ **Auto** Legacy USB support disabled if no USB devices are connected

5.3.6 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 8**) to set or change the configurations for the FDD controllers, parallel ports and serial ports.

```
         Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
            Advanced

 Super IO Configuration                              Set Parameters of Serial
                                                     Port 1 (COMA)
 Super IO Chip                    Finteck F81865
 > Serial Port 1 Configuration
 > Serial Port 2 Configuration                       ---------------------
 > Serial Port 3 Configuration                       ➔←: Select Screen
 > Serial Port 4 Configuration                       ↑ ↓: Select Item
 > Serial Port 5 Configuration                       Enter: Select
 > Parallel Port Configuration                       +/-:  Change Opt.
                                                     F1:   General Help
                                                     F2:   Previous Values
                                                     F3:   Optimized Defaults
                                                     F4:   Save & Exit
                                                     ESC: Exit


         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 8: Super IO Configuration

5.3.6.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 9**) to configure the serial port n.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
           Advanced

Serial Port 0 Configuration                                Enable or Disable Serial
                                                           Port (COM)
Serial Port                         [Enabled]
Device Settings                     IO=3F8h; IRQ=4
                                                           --------------------
Change Settings                     [Auto]                 →←: Select Screen
                                                           ↑ ↓: Select Item
                                                           Enter: Select
                                                           +/-:  Change Opt.
                                                           F1:   General Help
                                                           F2:   Previous Values
                                                           F3:   Optimized Defaults
                                                           F4:   Save & Exit
                                                           ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
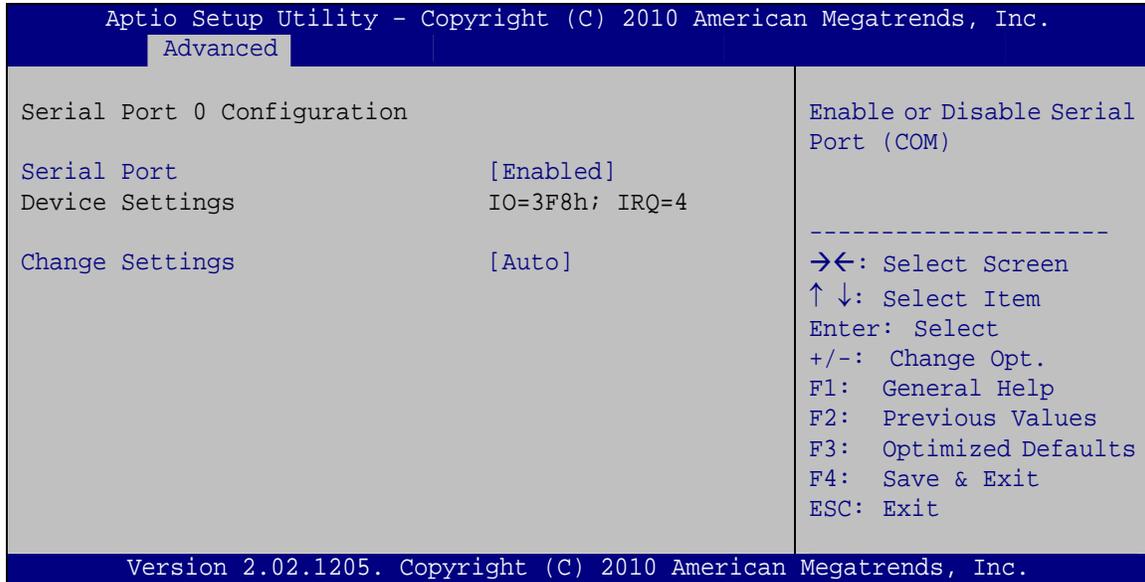
BIOS Menu 9: Serial Port n Configuration Menu

5.3.6.1.1 Serial Port 1 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**   Disable the serial port

➔ **Enabled** DEFAULT Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto** DEFAULT The serial port IO port address and interrupt address are automatically detected.

➔ **IO=3F8h;**
IRQ=4

Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

➔ **IO=3F8h;**
IRQ=3, 4

Serial Port I/O port address is 3F8h and the interrupt address is IRQ3 and IRQ4

➔ **IO=2F8h;**
IRQ=3, 4

Serial Port I/O port address is 2F8h and the interrupt address is IRQ3 and IRQ4

➔ **IO=2C0h;**
IRQ=3, 4

Serial Port I/O port address is 2C0h and the interrupt address is IRQ3 and IRQ4

➔ **IO=2C8h;**
IRQ=3, 4

Serial Port I/O port address is 2C8h and the interrupt address is IRQ3 and IRQ4

5.3.6.1.2 Serial Port 2 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**   Disable the serial port

➔ **Enabled** DEFAULT Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto** DEFAULT The serial port IO port address and interrupt address are automatically detected.

➔ **IO=2F8h;**
IRQ=3

Serial Port I/O port address is 2F8h and the interrupt address is IRQ3

➔ **IO=3F8h;**
IRQ=3, 4

Serial Port I/O port address is 3F8h and the interrupt address is IRQ3 and IRQ4

➔ **IO=2F8h;**
IRQ=3, 4

Serial Port I/O port address is 2F8h and the interrupt address is IRQ3 and IRQ4

➔ **IO=2C0h;**   Serial Port I/O port address is 2C0h and the interrupt

IRQ=3, 4   address is IRQ3 and IRQ4

➔ **IO=2C8h;**   Serial Port I/O port address is 2C8h and the interrupt

IRQ=3, 4   address is IRQ3 and IRQ4

5.3.6.1.3 Serial Port 3 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**   Disable the serial port

➔ **Enabled**   DEFAULT   Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt
address.

➔ **Auto**   DEFAULT   The serial port IO port address and interrupt address

are automatically detected.

➔ **IO=3E8h;**   Serial Port I/O port address is 3E8h and the interrupt

IRQ=10   address is IRQ10

➔ **IO=3E8h;**   Serial Port I/O port address is 3E8h and the interrupt

IRQ=10, 11   address is IRQ10, 11

➔ **IO=2E8h;**   Serial Port I/O port address is 2E8h and the interrupt

IRQ=10, 11   address is IRQ10, 11

➔ **IO=2D0h;**   Serial Port I/O port address is 2D0h and the interrupt

IRQ=10, 11   address is IRQ10, 11

➔ **IO=2D8h;**   Serial Port I/O port address is 2D8h and the interrupt

IRQ=10, 11   address is IRQ10, 11

➔ **Serial Port 3 Mode [RS232]**

Use the **Serial Port 3 Mode** option to select the serial port mode.

➔ **RS232**   DEFAULT   Enables serial port RS-232 support.

➔ **RS422/RS485**   Enables serial port RS-422/485 support.

5.3.6.1.4 Serial Port 4 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**   Disable the serial port

➔ **Enabled**   DEFAULT   Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**   DEFAULT   The serial port IO port address and interrupt address are automatically detected.

➔ **IO=2E8h;**   Serial Port I/O port address is 2E8h and the interrupt
   IRQ=10   address is IRQ10

➔ **IO=3E8h;**   Serial Port I/O port address is 3E8h and the interrupt
   IRQ=10, 11   address is IRQ10, 11

➔ **IO=2E8h;**   Serial Port I/O port address is 2E8h and the interrupt
   IRQ=10, 11   address is IRQ10, 11

➔ **IO=2D0h;**   Serial Port I/O port address is 2D0h and the interrupt
   IRQ=10, 11   address is IRQ10, 11

➔ **IO=2D8h;**   Serial Port I/O port address is 2D8h and the interrupt
   IRQ=10, 11   address is IRQ10, 11

5.3.6.1.5 Serial Port 5 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**   Disable the serial port

➔ **Enabled**   DEFAULT   Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

➔ **Auto**   DEFAULT   The serial port IO port address and interrupt address are automatically detected.

➔ **IO=2C0h; IRQ=10**   Serial Port I/O port address is 2C0h and the interrupt address is IRQ10

➔ **IO=2C0h; IRQ=10, 11**   Serial Port I/O port address is 2C0h and the interrupt address is IRQ10, 11

➔ **IO=2C8h; IRQ=10, 11**   Serial Port I/O port address is 2C8h and the interrupt address is IRQ10, 11

➔ **IO=2D0h; IRQ=10, 11**   Serial Port I/O port address is 2D0h and the interrupt address is IRQ10, 11

➔ **IO=2D8h; IRQ=10, 11**   Serial Port I/O port address is 2D8h and the interrupt address is IRQ10, 11

➔ **IO=2E0h; IRQ=10, 11**   Serial Port I/O port address is 2E0h and the interrupt address is IRQ10, 11

5.3.6.2 Parallel Port Configuration

Use the **Parallel Port Configuration** menu (**BIOS Menu 9**) to configure the serial port n.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
           Advanced

Parallel Port Configuration                                Enable or Disable
                                                           Parallel Port (LPT/LPTE)
Parallel Port                 [Enabled]
Device Settings               IO=378h; IRQ=7
                                                           --------------------
Change Settings               [Auto]                       →←: Select Screen
Device Mode                   [Printer Mode]               ↑ ↓: Select Item
                                                           Enter: Select
                                                           +/-: Change Opt.
                                                           F1:  General Help
                                                           F2:  Previous Values
                                                           F3:  Optimized Defaults
                                                           F4:  Save & Exit
                                                           ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 10: Parallel Port Configuration Menu

➔ **Parallel Port [Enabled]**

Use the **Parallel Port** option to enable or disable the parallel port.

➔ **Disabled**　　　　　　　Disable the parallel port

➔ **Enabled**　**DEFAULT**　Enable the parallel port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the parallel port IO port address and interrupt address.

➔ **Auto**　**DEFAULT**　The parallel port IO port address and interrupt address are automatically detected.

➔ **IO=378h; IRQ=7**　Parallel Port I/O port address is 378h and the interrupt address is IRQ7

➔	**IO=278h;**	Parallel Port I/O port address is 278h and the
	IRQ=7	interrupt address is IRQ7
➔	**IO=3BCh;**	Parallel Port I/O port address is 3BCh and the
	IRQ=7	interrupt address is IRQ7

➔   **Device Mode [Printer Mode]**

Use the **Device Mode** option to select the mode the parallel port operates in. Configuration options are listed below.

- ▪ Printer Mode   **Default**
- ▪ SPP Mode
- ▪ EPP-1.9 and SPP Mode
- ▪ EPP-1.7 and SPP Mode
- ▪ ECP Mode
- ▪ ECP and EPP 1.9 Mode
- ▪ ECP and EPP 1.7 Mode

5.3.7 H/W Monitor

The H/W Monitor menu (**BIOS Menu 11**) shows the operating temperature, fan speeds and system voltages.

```
        Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
            Advanced

 PC Health Status

 CPU Temperature                     :+39 C
 SYS Temperature                     :+40 C
 CPU FAN Speed                       :N/A
 SYS FAN Speed                       :N/A
 VCC3V                               :+3.344 V
 V_core                              :+1.136 V        --------------------
 Vcc                                 :+5.087 V        →←: Select Screen
 Vcc12                               :+11.352 V       ↑↓: Select Item
 Vcc1_5VDDR                          :+1.504 V        Enter: Select
 VSB3V                               :+3.360 V        +/-:  Change Opt.
 VBAT                                :+3.316 V        F1:  General Help
 CPU Smart Fan control               [Auto Mode]      F2:  Previous Values
 Temperature Bound1                  60               F3:  Optimized Defaults
 Temperature Bound2                  50               F4:  Save & Exit
 Temperature Bound3                  40               ESC: Exit
 Temperature Bound4                  30

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 11: H/W Monitor Configuration

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

- System Temperatures:
  - ○ CPU Temperature
  - ○ System Temperature
- Fan Speeds:
  - ○ CPU Fan Speed
  - ○ System Fan Speed
- Voltages:
  - ○ V_core
  - ○ Vcc
  - ○ Vcc12
  - ○ Vcc1_5VDDR
  - ○ VSB3V
  - ○ VBAT

➔ **CPU Smart Fan control [Auto Mode]**

Use the **CPU Smart Fan control** option to configure the CPU fan.

➔ **Auto Mode**   The fan adjusts its speed using these settings:

   Temperature Bound 1

   Temperature Bound 2

   Temperature Bound 3

   Temperature Bound 4

➔ **Manual Mode**   The fan spins at the speed set in:

   Manual Duty Cycle Setting

5.3.8 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 12**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.

```
        Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
         Advanced

  COM1                                              Console Redirection
  Console Redirection          [Disabled]           Enable/Disable
> Console Redirection Settings

  COM2                                              --------------------
  Console Redirection          [Disabled]           →←: Select Screen
> Console Redirection Settings                      ↑↓: Select Item
                                                    Enter:  Select
  COM3                                              +/-:  Change Opt.
  Console Redirection          [Disabled]           F1:   General Help
> Console Redirection Settings                      F2:   Previous Values
                                                    F3:   Optimized Defaults
  COM4                                              F4:   Save & Exit
  Console Redirection          [Disabled]           ESC:  Exit
> Console Redirection Settings

  COM5
  Console Redirection          [Disabled]
> Console Redirection Settings

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 12: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

➔ **Disabled**   DEFAULT   Disabled the console redirection function

➔ **Enabled**   Enabled the console redirection function

![NOTE icon] **NOTE:**

The following items will be available to configure only when the **Console Redirection** item is set to **Enabled**.

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100**   The target terminal type is VT100

➔ **VT100+**   The target terminal type is VT100+

➔ **ANSI**   DEFAULT   The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

➔ **9600**   Sets the serial port transmission speed at 9600.

➔ **19200**   Sets the serial port transmission speed at 19200.

➔ **38400**   Sets the serial port transmission speed at 38400.

➔ **57600**   Sets the serial port transmission speed at 57600.

➔ **115200**   DEFAULT   Sets the serial port transmission speed at 115200.

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 13**) to access the Northbridge and Southbridge configuration menus

![WARNING icon] **WARNING!**

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

```
        Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
   Main    Advanced  Chipset    Boot    Security  Save & Exit

> Host Bridge                                    North Bridge Parameters
> South Bridge
> Intel IGD SWSCI OpRegion
                                                 --------------------
                                                 →←: Select Screen
                                                 ↑ ↓: Select Item
                                                 Enter: Select
                                                 +/-:  Change Opt.
                                                 F1:   General Help
                                                 F2:   Previous Values
                                                 F3:   Optimized Defaults
                                                 F4:   Save & Exit
                                                 ESC:  Exit

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 13: Chipset

5.4.1 Host Bridge Configuration

Use the **Host Bridge Configuration** menu (**BIOS Menu 14**) to configure the Northbridge chipset.

```
          Aptio Setup Utility - Copyright (C) 2010 American Megatrends, Inc.
                      Chipset

 > OnChip VGA Configuration                              Config On Chip VGA
   Initate  Graphic Adapter          [PCI/IGD]           Settings.

 ******* Memory Information *******
 Memory Frequency                  667 Mhz
                                                         --------------------
 Total Memory                      1024 MB               →←: Select Screen
                                                         ↑ ↓: Select Item
 DIMM#0                            1024 MB               Enter: Select
 DIMM#1                            Not Present           +/-:  Change Opt.
                                                         F1:   General Help
                                                         F2:   Previous Values
                                                         F3:   Optimized Defaults
                                                         F4:   Save & Exit
                                                         ESC: Exit

          Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 14: Host Bridge Chipset Configuration

➔   **Initate Graphic Adapter [PCI/IGD]**

Use the **Initate Graphic Adapter** option to select which graphics controller to be used as the primary boot device. Configuration options are listed below.

- IGD
- PCI/IGD   DEFAULT

5.4.1.1 OnChip VGA Configuration

Use the **OnChip VGA Configuration** menu (**BIOS Menu 14**) to configure the OnChip VGA.

```
          Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
                    Chipset

OnChip VGA Configuration                               Select Share Memory
                                                       Size.
Share Memory Size                 [8 MB]
                                                       --------------------
                                                       →←: Select Screen
                                                       ↑ ↓: Select Item
                                                       Enter: Select
                                                       +/-:  Change Opt.
                                                       F1:   General Help
                                                       F2:   Previous Values
                                                       F3:   Optimized Defaults
                                                       F4:   Save & Exit
                                                       ESC:  Exit

          Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
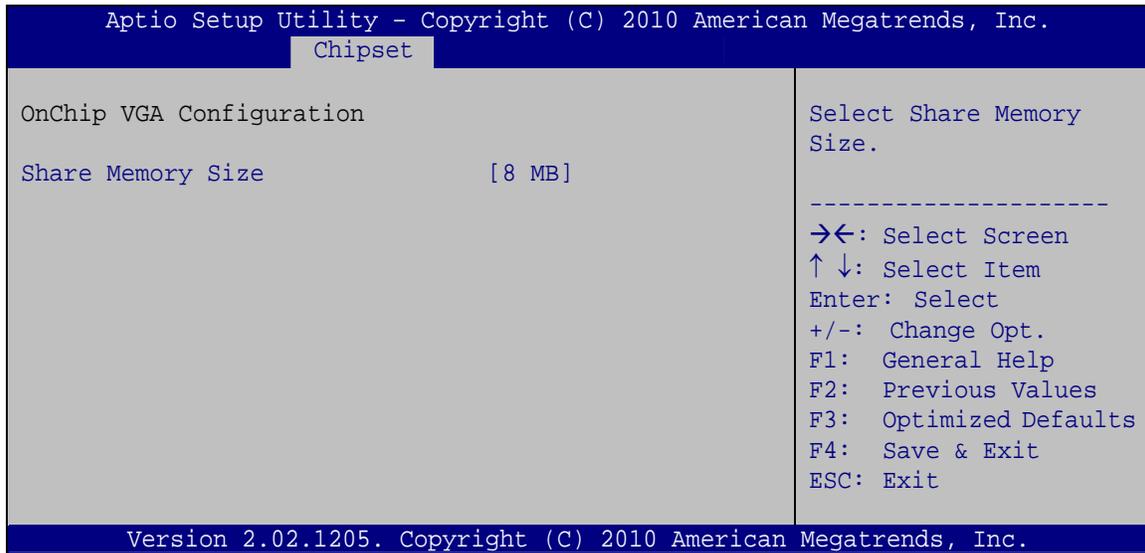
BIOS Menu 15: OnChip VGA Configuration

➔ **Share Memory Size [8 MB]**

Use the **Share Memory Size** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- Disabled
- 8 MB   **Default**

5.4.2 South Bridge Configuration

Use the **South Bridge Configuration** menu (**BIOS Menu 16**) to configure the Southbridge chipset.

```
Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
                        Chipset

Auto Power Button Function       [Enabled]            HD Audio Controller
HD Audio Controller              [Enabled]
USB Function                     [Enabled]
USB 2.0(EHCI) Support            [Enabled]             --------------------
Set Spread Spectrum function     [Disabled]
                                                       →←: Select Screen
                                                       ↑ ↓: Select Item
                                                       Enter: Select
                                                       +/-:  Change Opt.
                                                       F1:  General Help
                                                       F2:  Previous Values
                                                       F3:  Optimized Defaults
                                                       F4:  Save & Exit
                                                       ESC: Exit

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 16:South Bridge Chipset Configuration

➔ **HD Audio Controller [Enabled]**

Use the **HD Audio Controller** option to enable or disable the High Definition Audio controller.

➔ **Enabled**   DEFAULT   The onboard High Definition Audio controller automatically detected and enabled

➔ **Disabled**   The onboard High Definition Audio controller is disabled

➔ **USB Function [Enabled]**

Use the **USB Function** BIOS option to enable or disable USB function support.

➔ **Disabled**   USB function support disabled

➔ **Enabled**   DEFAULT   USB function support enabled

➔ **USB 2.0 (EHCI) Support [Enabled]**

Use the **USB 2.0 (EHCI) Support** BIOS option to enable or disable USB 2.0 support.

➔ **Enabled**   DEFAULT   USB 2.0 (EHCI) support enabled

➔ **Disabled**   USB 2.0 (EHCI) support disabled

➔ **Set Spread Spectrum Function [Disabled]**

The **Set Spread Spectrum Function** option can help to improve CPU EMI issues.

➔ **Disabled** DEFAULT The spread spectrum mode is disabled

➔ **Enabled** The spread spectrum mode is enabled

5.4.3 Intel IGD SWSCI OpRegion

Use the **Intel IGD SWSCI OpRegion** menu to configure the video device connected to the system.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
                        Chipset

Intel IGD SWSCI OpRegion Configuration                  Select DVMT Mode/Fixed
                                                        Mode
DVMT Mode Select                  [DVMT Mode]
DVMT/FIXED Memory                 [256 MB]              --------------------
IGD - Boot Type                   [VBIOS Default]       →←: Select Screen
LCD Panel Type                    [640x480 18bit]       ↑ ↓: Select Item
                                                        Enter: Select
                                                        +/-:  Change Opt.
                                                        F1:   General Help
                                                        F2:   Previous Values
                                                        F3:   Optimized Defaults
                                                        F4:   Save & Exit
                                                        ESC:  Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
**BIOS Menu 17:South Bridge Chipset Configuration**

➔ **DVMT Mode Select [DVMT Mode]**

Use the **DVMT Mode Select** option to select the Intel Dynamic Video Memory Technology (DVMT) operating mode.

➔ **Fixed Mode** A fixed portion of graphics memory is reserved as graphics memory.

➔ **DVMT Mode** DEFAULT Graphics memory is dynamically allocated according to the system and graphics needs.

➔ **DVMT/FIXED Memory [256 MB]**

Use the **DVMT/FIXED Memory** option to specify the maximum amount of memory that can be allocated as graphics memory. Configuration options are listed below.

- 128 MB
- 256 MB   **Default**
- Maximum

➔ **IGD - Boot Type [VBIOS Default]**

Use the **IGD - Boot Type** option to select the display device used by the system when it boots. Configuration options are listed below.

- VBIOS Default   **DEFAULT**
- CRT
- LFP
- CRT + LFP

➔ **LCD Panel Type [640x480 18bit]**

Use the **LCD Panel Type** option to select the type of flat panel connected to the system. Configuration options are listed below.

- 640x480 18bit   **DEFAULT**
- 800x480 18bit
- 800x600 18bit
- 1024x768 18bit
- 1280x1024 18bit
- 1366x768 18bit
- 1280x800 18bit
- 1280x600 18bit

5.5 Boot

Use the **Boot** menu (**BIOS Menu 18**) to configure system boot options.

```
        Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
   Main    Advanced   Chipset    Boot    Security  Save & Exit

 Boot Configuration                                  Select the keyboard
 Boot NumLock State              [On]                NumLock state

 Quiet Boot                      [Enabled]           --------------------
 Launch PXE OpROM                [Disabled]          →←: Select Screen
                                                     ↑ ↓: Select Item
 Boot Option Priorities                              Enter: Select
                                                     +/-:  Change Opt.
                                                     F1:  General Help
                                                     F2:  Previous Values
                                                     F3:  Optimized Defaults
                                                     F4:  Save & Exit
                                                     ESC: Exit

        Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 18: Boot

➔ **Bootup NumLock State [On]**

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

➔ **On**   DEFAULT   Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

➔ **Off**   Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔ **Disabled**　　　　　　　　Normal POST messages displayed

➔ **Enabled**　　DEFAULT　　OEM Logo displayed instead of POST messages

➔ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

➔ **Disabled**　　DEFAULT　　Ignore all PXE Option ROMs

➔ **Enabled**　　　　　　　　Load PXE Option ROMs.

5.6 Security

Use the **Security** menu (**BIOS Menu 19**) to set system and user passwords.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
   Main     Advanced   Chipset      Boot    Security  Save & Exit

 Password Description                                Set Setup Administrator
                                                     Password
 If ONLY the Administrator's password is set,
 then this only limits access to Setup and is
 only asked for when entering Setup.                 --------------------
 If ONLY the User's password is set, then this       ➔←: Select Screen
 is a power on password and must be entered to        ↑ ↓ : Select Item
 boot or enter Setup. In Setup the User will         Enter: Select
 have Administrator rights.                           +/-:  Change Opt.
 The password must be 3 to 20 characters long.       F1:  General Help
                                                     F2:  Previous Values
                                                     F3:  Optimized Defaults
 Administrator Password                              F4:  Save & Exit
 User Password                                       ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```

BIOS Menu 19: Security

➔ **Administrator Password**

Use the **Administrator Password** to set or change a administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.7 Save & Exit

Use the **Exit** menu (**BIOS Menu 20**) to load default BIOS values, optimal failsafe values and to save configuration changes.

```
         Aptio Setup Utility – Copyright (C) 2010 American Megatrends, Inc.
   Main    Advanced   Chipset     Boot    Security  Save & Exit

   Save Changes and Reset                            Reset the system after
   Discard Changes and Reset                         saving the changes.

   Restore Defaults
   Save as User Defaults                             --------------------
   Restore User Defaults                             →←: Select Screen
                                                     ↑ ↓: Select Item
                                                     Enter: Select
                                                     +/-:  Change Opt.
                                                     F1:   General Help
                                                     F2:   Previous Values
                                                     F3:   Optimized Defaults
                                                     F4:   Save & Exit
                                                     ESC: Exit

         Version 2.02.1205. Copyright (C) 2010 American Megatrends, Inc.
```
BIOS Menu 20: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

Product Disposal

⚠️ **CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union – If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union – The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.
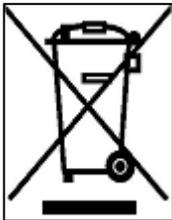
EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Menu Options

Appendix

D

Terminology

AC '97	Audio Codec 97 (AC'97) refers to a codec standard developed by Intel® in 1997.
ACPI	Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.
AHCI	Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.
ATA	The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.
APM	The Advanced Power Management (APM) application program interface (API) enables the inclusion of power management in the BIOS.
ARMD	An ATAPI Removable Media Device (ARMD) is any ATAPI device that supports removable media, besides CD and DVD drives.
ASKIR	Amplitude Shift Keyed Infrared (ASKIR) is a form of modulation that represents a digital signal by varying the amplitude ("volume") of the signal. A low amplitude signal represents a binary 0, while a high amplitude signal represents a binary 1.
BIOS	The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user
CODEC	The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.
CMOS	Complimentary metal-oxide-conductor is a type of integrated circuit used in chips like static RAM and microprocessors.
COM	COM is used to refer to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DE-9 connector.
DAC	The Digital-to-Analog Converter (DAC) converts digital signals to analog signals.
DDR	Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.
DMA	Direct Memory Access (DMA) enables some peripheral devices to bypass the system processor and communicate directly with the system

memory.

DIMM	Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.
EHCI	The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.
GbE	Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.
GPIO	General purpose input
IrDA	Infrared Data Association (IrDA) specify infrared data transmission protocols used to enable electronic devices to wirelessly communicate with each other.
L1 Cache	The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.
L2 Cache	The Level 2 Cache (L2 Cache) is an external processor memory cache.
LVDS	Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.
MAC	The Media Access Control (MAC) protocol enables several terminals or network nodes to communicate in a LAN, or other multipoint networks.
PCIe	PCI Express (PCIe) is a communications bus that uses dual data lines for full-duplex (two-way) serial (point-to-point) communications between the SBC components and/or expansion cards and the SBC chipsets. Each line has a 2.5 Gbps data transmission rate and a 250 MBps sustained data transfer rate.
POST	The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.
QVGA	Quarter Video Graphics Array (QVGA) refers to a display with a resolution of 320 x 240 pixels.
RAM	Random Access Memory (RAM) is a form of storage used in computer. RAM is volatile memory, so it loses its data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.

SATA   Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA 3Gb/s bus has data transfer speeds of up to 3.0 Gbps.

S.M.A.R.T   Self Monitoring Analysis and Reporting Technology (S.M.A.R.T) refers to automatic status checking technology implemented on hard disk drives.

UART   Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.

UHCI   The Universal Host Controller Interface (UHCI) specification is a register-level interface description for USB 1.1 Host Controllers.

USB   The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates, while USB 2.0 supports 480Mbps data transfer rates.

VGA   The Video Graphics Array (VGA) is a graphics display system developed by IBM.

Appendix

E

Digital I/O Interface

E.1 Introduction

The DIO connector on the NANO-PV-D4252/N4552/D5252 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 4-bit digital inputs and 4-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

NOTE:

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH
Sub-function:
AL – 8 :Set the digital port as INPUT
AL :Digital I/O input value

E.2 Assembly Language Sample 1

```
MOV        AX, 6F08H           ; setting the digital port as input
INT        15H                 ;
```

AL low byte = value

AH − 6FH
Sub-function:
AL − 9   : Set the digital port as OUTPUT
BL   : Digital I/O input value

E.3 Assembly Language Sample 2

```
MOV        AX, 6F09H           ; setting the digital port as output
MOV        BL, 09H             ; digital value is 09H
INT        15H                 ;
```

Digital Output is 1001b

Appendix

F

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. IEI support is contacted or the IEI website visited for specific drivers for more sophisticated operating systems, e.g., Windows and Linux.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMI or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer:

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table F-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. While the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the Watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

 NOTE:

> When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

Example program:

```
; INITIAL TIMER PERIOD COUNTER
;
W_LOOP:

        MOV     AX, 6F02H      ;setting the time-out value
        MOV     BL, 30H            ;time-out value is 48 seconds
        INT       15H
 ;
; ADD THE APPLICATION PROGRAM HERE
;
        CMP      EXIT_AP, 1         ;is the application over?
        JNE        W_LOOP       ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0               ;
        INT       15H
;
; EXIT ;
```

Appendix

G

Hazardous Materials Disclosure

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated "Environmentally Friendly Use Period" (EFUP). This is an estimate of the number of years that these substances would "not leak out or undergo abrupt change." This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

Please refer to the table on the next page.

Part Name	Toxic or Hazardous Substances and Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
Housing	O	O	O	O	O	O
Display	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O
Battery	O	O	O	O	O	O
O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011). X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).						

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
显示	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 (现由 GB/T 26572-2011 取代) 标准规定的限量要求。