

CIR-W4DUSY3208G

DDR4 WIDE TEMP. DIMM 3200MHz 8GB

Description

CIR-W4DUSY3208G is a CMOS Double Data Rate IV (DDR4) Synchronous DRAM module, in Fine Ball Grid Array (FBGA) packages on a 288pin glass-epoxy substrate.

DDR4 unbuffered UDIMM series offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Specifications

| | |
|------------------------|--------------------|
| Density | 8GB |
| Pin Count | 288pin |
| Type | Unbuffered |
| Dimensions | 133.35mm x 31.25mm |
| ECC | Non-ECC |
| Component Config | 1G x 8 bit |
| Data Rate | 3200 MHz |
| CAS Latency | 22 |
| Voltage | 1.2V |
| PCB Layers | 8 |
| Operating Temp.(TCASE) | -40°C~+85°C |
| Module Ranks | Single Rank |

Features

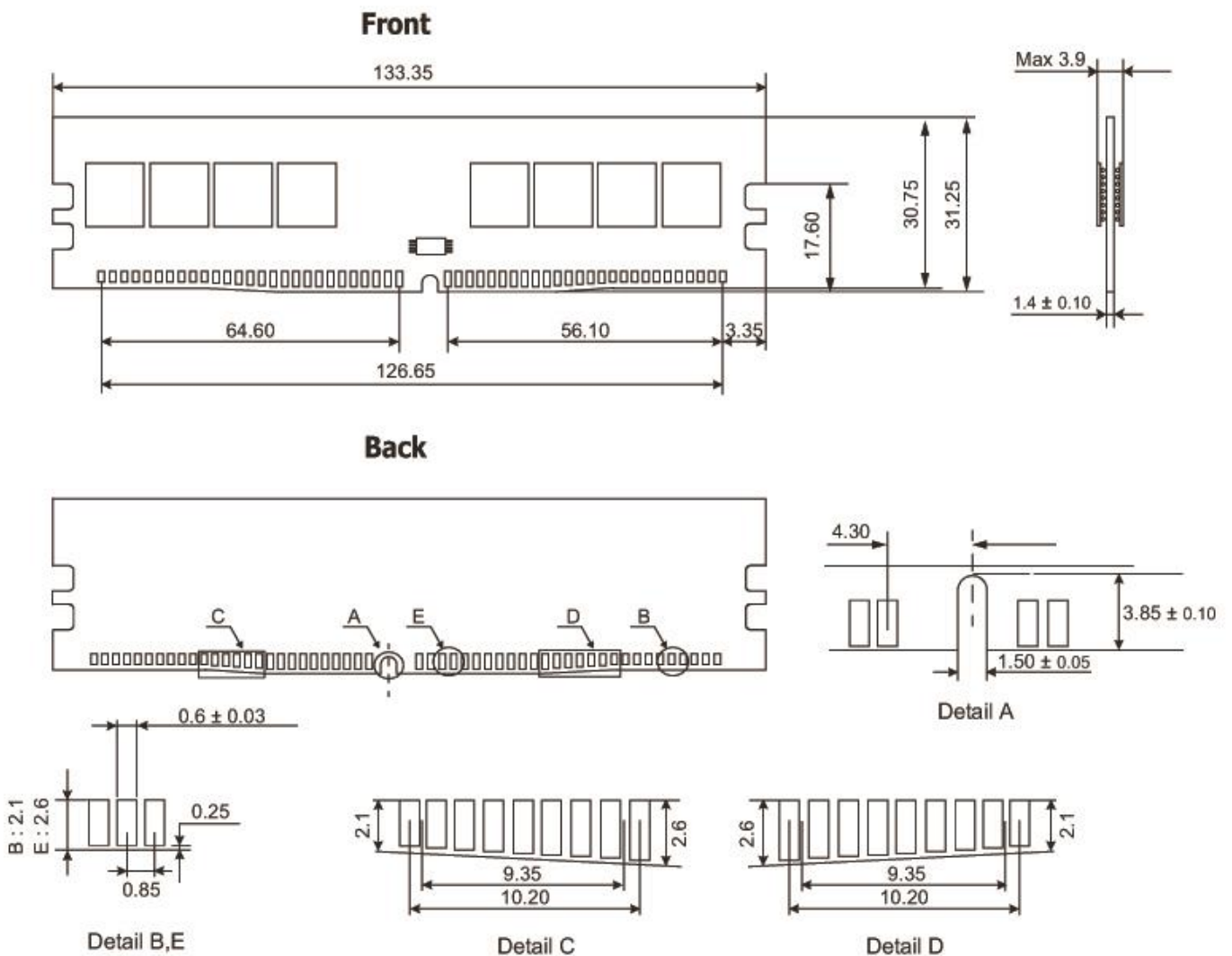
- JEDEC standard
- VDD=VDDQ = 1.2V±0.06V (1.14V~1.26V)
- Inputs and Outputs are SSTL-12 compatible
- Programmable CAS Latency(posted CAS): 11,12,13,14,15,16,17,18,19,20,21,22
- Low-Power auto self-refresh(LPASR)
- SDRAMs have 16 internal banks for concurrent operation(4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Fly-By topology
- Terminated control, command and address bus
- RoHS and Halogen free

Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | | | | | | | | | | CL-tRCD-tRP |
|-----------------|--------------------|---------------------|------|------|------|------|------|------|------|------|------|------|------|-------------|
| | | CL11 | CL12 | CL13 | CL14 | CL15 | CL16 | CL17 | CL18 | CL19 | CL20 | CL21 | CL22 | |
| DDR4-3200 | PC4-25600 | 1600 | 1600 | 1866 | 1866 | 2133 | 2133 | 2400 | 2400 | 2666 | 2666 | 2933 | 3200 | 22-22-22 |

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified