CIR-S3DUHK1304G

DDR3 DIMM 1333MHz 4GB

Description

The CIR-S3DUHK1304G is 512M words X 64 bits, 1 rank. Unbuffered dual in line memory module (DIMM). DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240pin glass-epoxy substrate. Provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

Density	4GB
Pin Count	240pin
Type	Unbuffered
Dimensions	133.35mm x 30.0mm
ECC	Non-ECC
Component Config	512M x 8 bit
Data Rate	1333 Mbps
CAS Latency	9
Voltage:	1.5V / 1.35V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Single Rank

Features

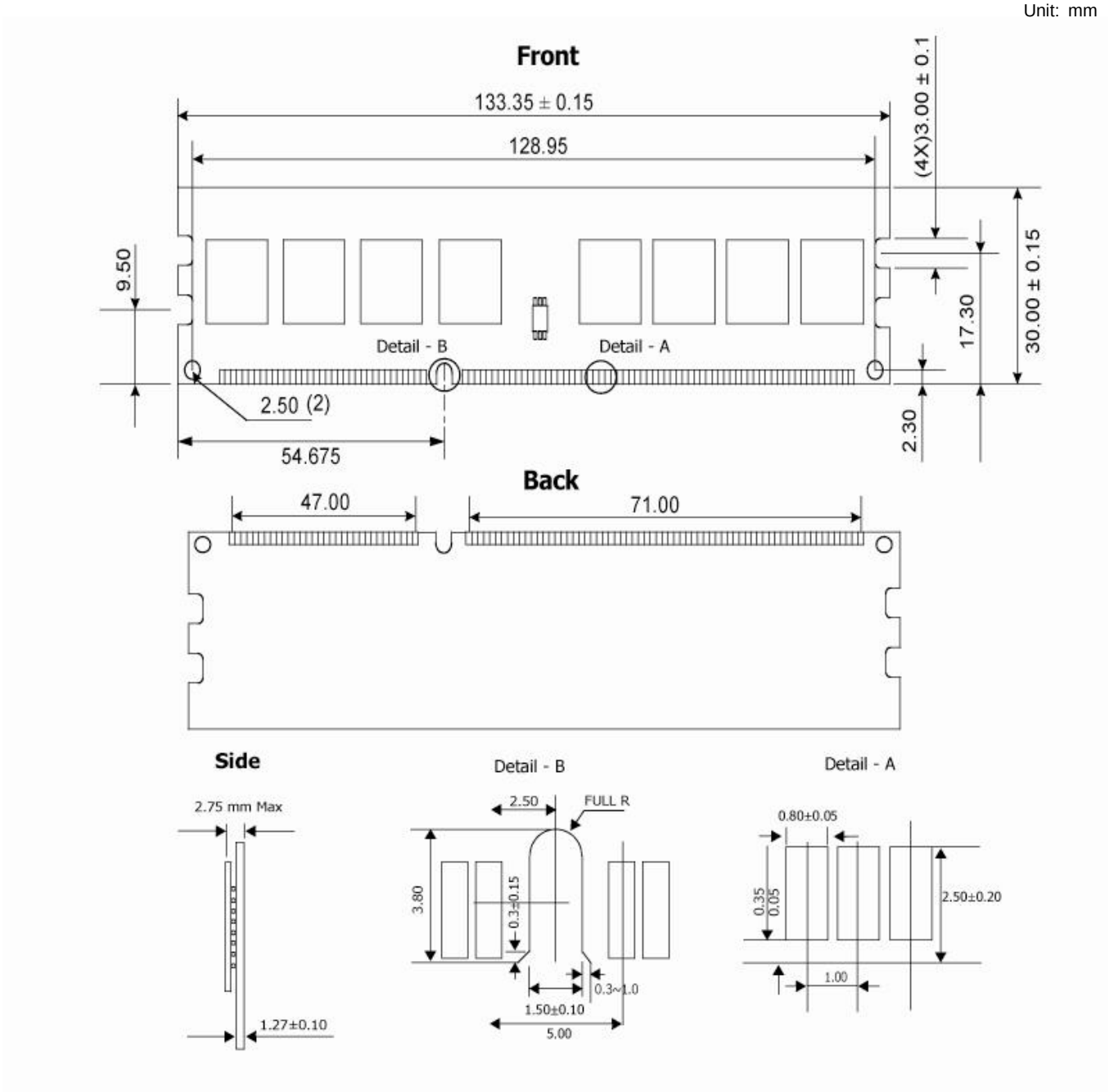
- Data rate: 1333Mbps
- 240-pin socket type Unbuffered dual in line memory module (DIMM)
- Power supply: VDD= 1.5V (1.425V to 1.575V) & VDD= 1.35V (1.283V to 1.45V)
- Interface: SSTL_15
- CAS (READ) latency (CL): 6, 7, 8, 9
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- DM masks write data-in at the both rising and falling edges of the data strobe
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Refresh: Auto-Refresh, Self-Refresh
- 8 bit pre-fetch
- Lead-Free Products are RoHS compliant
- TCASE of 0°C to 95°C (Components)
  —64ms, 8,192 cycle refresh at 0°C to 85°C
  —32ms at 85°C to 95°C

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support				CL-tRCD-tRP
		CL6	CL7	CL8	CL9	
DDR3-1333	PC3-10600	800	1066	1066	1333	9-9-9

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified