CIR-W3SULPK1304G

DDR3 WIDE TEMP. SO-DIMM LOW VOLTAGE 1333MHz 4GB

Description

The CIR-W3SULPK1304G is 512M words X 64 bits, 1 rank. Unbuffered Small Outline SingleIn-Line Memory Module (SO-DIMM) .DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

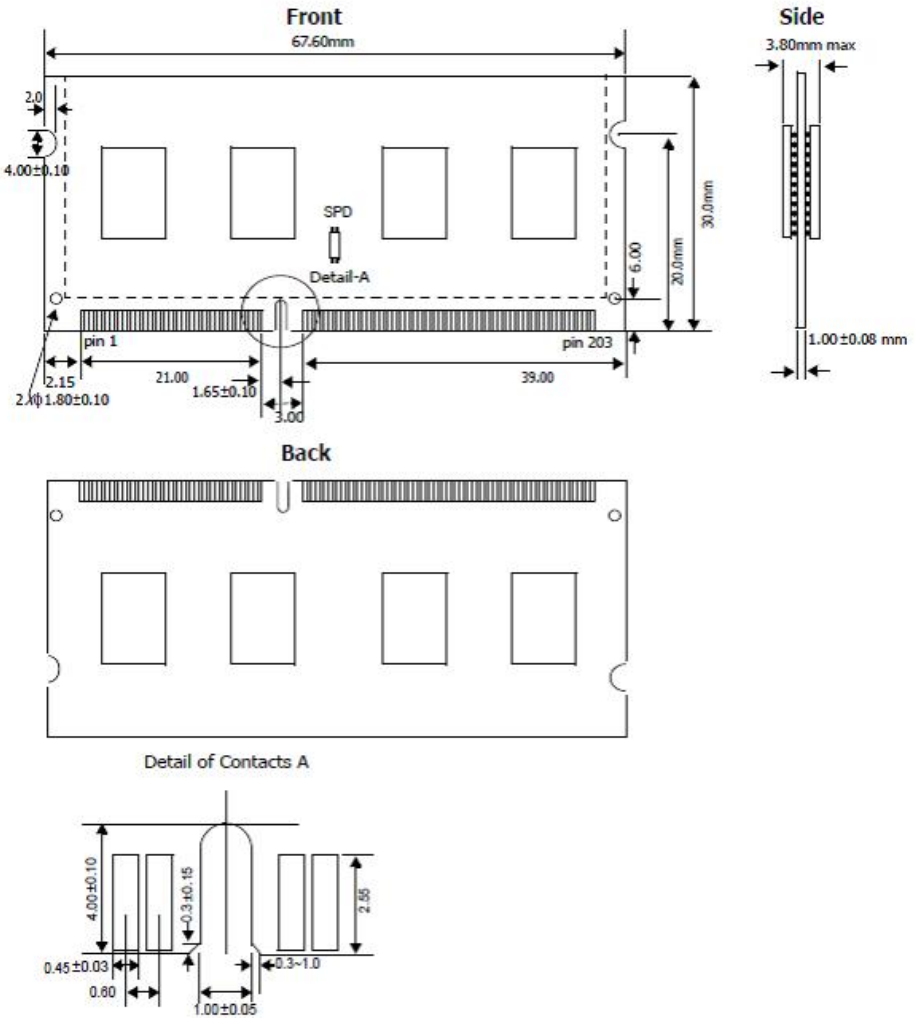
Density	4GB
Pin Count	204pin
Type	Unbuffered
Dimensions	67.6mm x 30.0mm
ECC	Non-ECC
Component Config	512M x 8 bit
Data Rate	1333 Mbps
CAS Latency	9
Voltage:	1.35V
PCB Layers	8
Operating Temp.	-40°C~+85°C
Module Ranks	Single Rank

Features

- Data rate:1333Mbps
- RoHS compliant products.
- 204pin,Small outline single in-line memory module(SO-DIMM)
- VDDQ= 1.35V (1.28V~1.45V) & VDDQ=1.5V(1.425V~1.575V)
- JEDEC standard 1.35V(1.28V~1.45V) & JEDEC standard 1.5V(1.425V~1.575V)
- Programmable CAS Latency(CL):6,7,8,9,10,11support
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- Serial presence detect with EEPROM
- 8 independent internal bank
- 8K refresh cycles /64ms
- On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Bi-directional Differential Data Strobe
- Burst Length: 4, 8
- 8 bit pre-fetch
- Average Refresh Period 7.8us at -40℃≦TC≦85℃
  3.9us at 85℃＜TC≦95℃

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified