CIR-W3SUII1302G

DDR3 WIDE TEMP. SO-DIMM 1333MHz 2GB

Description

The CIR-W3SUII1302G is 256M words X 64 bits, 1 rank. Unbuffered Small Outline dual In-Line Memory Module (SO-DIMM). DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

Density	2GB
Pin Count	204pin
Type	Unbuffered
Dimensions	67.6mm x 30.0mm
ECC	Non-ECC
Component Config	256M x 8 bit
Data Rate	1333 Mbps
CAS Latency	9
Voltage:	1.5V
PCB Layers	8
Operating Temp.(TCASE)	-40°C~+95°C
Module Ranks	Single Rank

Features

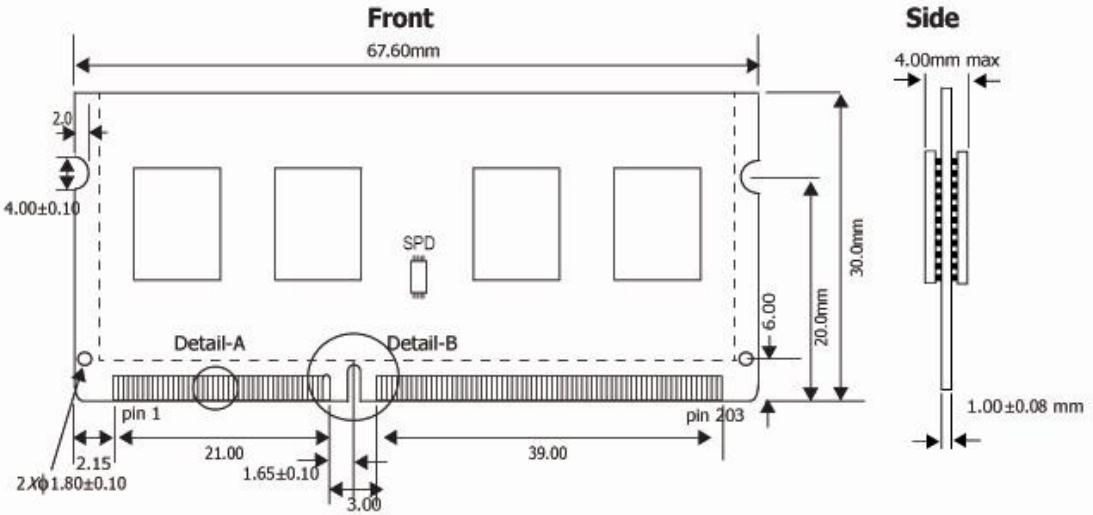
- Data rate: 1333Mbps
- RoHS compliant products.
- 204pin,Small outline dual in-line memory module(SO-DIMM)
- VDD = 1.5V (1.425V to 1.575V)
- Interface: SSTL_15
- Programmable CAS Latency(CL): 6,7,8,9 support
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- Serial presence detect with EEPROM
- 8 independent internal bank
- 8K refresh cycles /64ms
- On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- POSTED CAS additive latency (AL)
- Bi-directional Differential Data Strobe
- Burst Length: 4, 8
- 8 bit pre-fetch
- TCASE of 0°C to 95°C (Components)
  -- 64ms, 8,192 cycle refresh at 0°C to 85°C
  -- 32ms at 85°C to 95°C

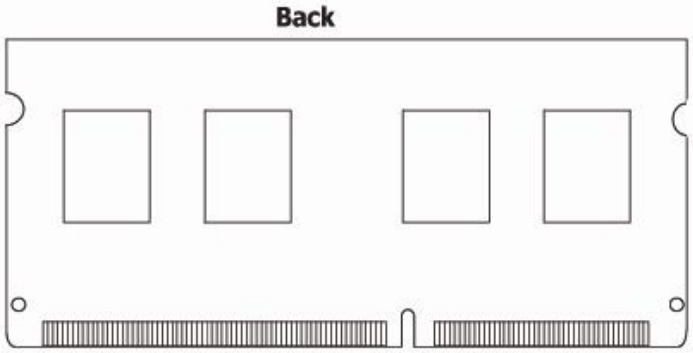
Speed Grade

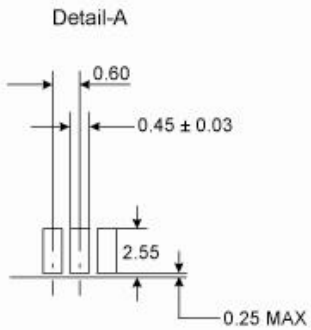
Frequency Grade	Data Transfer Rate	CAS Latency Support				CL-tRCD-tRP
		CL6	CL7	CL8	CL9	
DDR3-1333	PC3-10600	800	1066	1066	1333	9-9-9

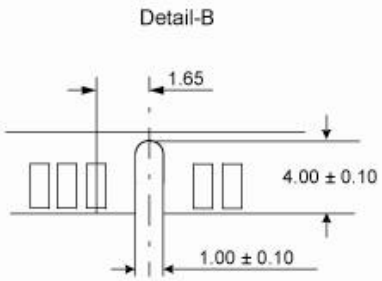
Package Dimensions

Unit: mm









Tolerances : ± 0.15mm unless otherwise specified