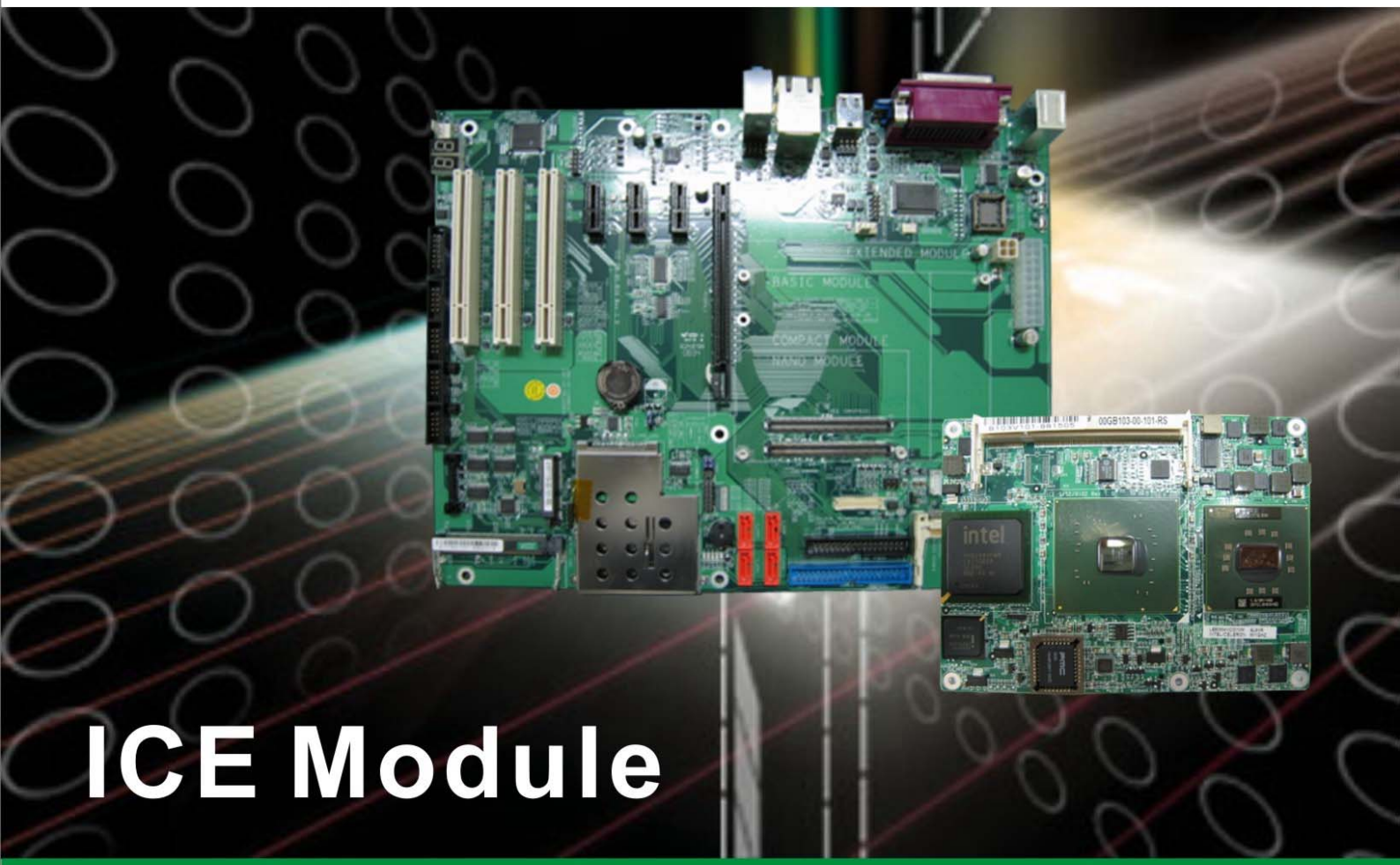
IEI Technology Corp.



ICE Module

Carrier Board Design Guide

Rev. 1.00 September 2008

RoHS Lead Free

Revision

Date	Version	Changes
2008-09	1.00	Initial release

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Chapter

1

Introduction

1.1 Introduction

This design guide describes the design concept of the IEI COM Express module and how to teach customers to develop their own COM Express baseboard. IEI COM Express module is compatible with all baseboards compliant with COM Express specification.

1.2 Acronyms and Abbreviations Definition

Table 1-1 defines the acronyms, conventions, and terminology that are used throughout the design guide.

Table 1-1: Conventions and Terminology

Terminology	Description
AC97	Audio Codec 97’
HDA	High Definition Audio
SATA	Serial AT Attachment: serial-interface standard for hard disks
IDE (ATA)	Integrated Drive Electronics (Advanced Technology Attachment)
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
PCIe x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x16 link.
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses
GBE	Gigabit Ethernet
CRT	Cathode Ray Tube
DDR	Double Data Rate SDRAM memory technology
DVI	Digital Visual Interface is the interface specified by the DDWG (Digital Display working Group) DVI Spec. Rev. 1.0
DDC	Display Data Channel is an I2C bus interface between a display and a graphics adapter.

I2C	Inter-IC (a two wire serial bus created by Philips)
LCD	Liquid Crystal Display
LFP	Local Flat Panel
LVDS	Low Voltage Differential Signaling: A high speed, low power data transmission standard used for display connections to LCD panels.
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
PCI	Peripheral Component Interface
RTC	Real Time Clock
SMBus	System Management Bus.
COM	Computer On Module
STD	Suspend To Disk
STR	Suspend To RAM
ULV	Ultra-Low Voltage
USB	Universal Serial Bus
PCI	
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

1.3 Reference Documents

Table 1-2 lists all the reference documents of this design guide.

Table 1-2: Reference Documents

Document	Location
PICMGR COM Express Module™ Base Specification	http://www.picmg.org/
I2C Bus Interface	http://www.semiconductors.philips.com/
PCI Local Bus Specification, Revision 2.3	http://www.pcisig.com/
Serial ATA Specification, Revision 1.0a	http://www.serialata.org/
PC104	http://www.pc104.org/technology/pc104_tech.html
SMBus	http://www.smbus.org/specs/
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org/home
IrDA	http://www.irda.org/
Ethernet(IEEE 802.3)	http://www.ieee.org/portal/site
RS-232	http://www.eia.org/
Advanced Configuration and Power Management (ACPI) Specification 1.0b & 2.0	http://www.teleport.com/~acpi/
Advanced Power Management (APM) Specification 1.2	http://www.microsoft.com/hwdev/busbios/amp_12.htm
PCI Express Base Specification, Revision 2.0	http://www.pcisig.com/specifications
ExpressCard Standard Release 1.0	http://www.expresscard.org/
High Definition Audio Specification, Rev. 1.0	http://www.intel.com/standards/hdaudio/
Extended Display Identification Data Standard Version 1.3 (EDID™)	http://www.vesa.org/
Enhanced Display Data Channel Specification Version 1.1 (DDC)	http://www.vesa.org/
Audio Codec '97 Component Specification, Version 2.3	http://www.intel.com/design/chipsets/audio/

Chapter

2

ICE Module Overview

2.1 Chapter Overview

ICE modules have various options for users to choose. IEI provides high-end, mid-range and low-end CPU modules. Using the ICE module can overcome the problems that may be caused by designing a compatible and stable module. IEI also provides the service of deigning COM Express baseboard.

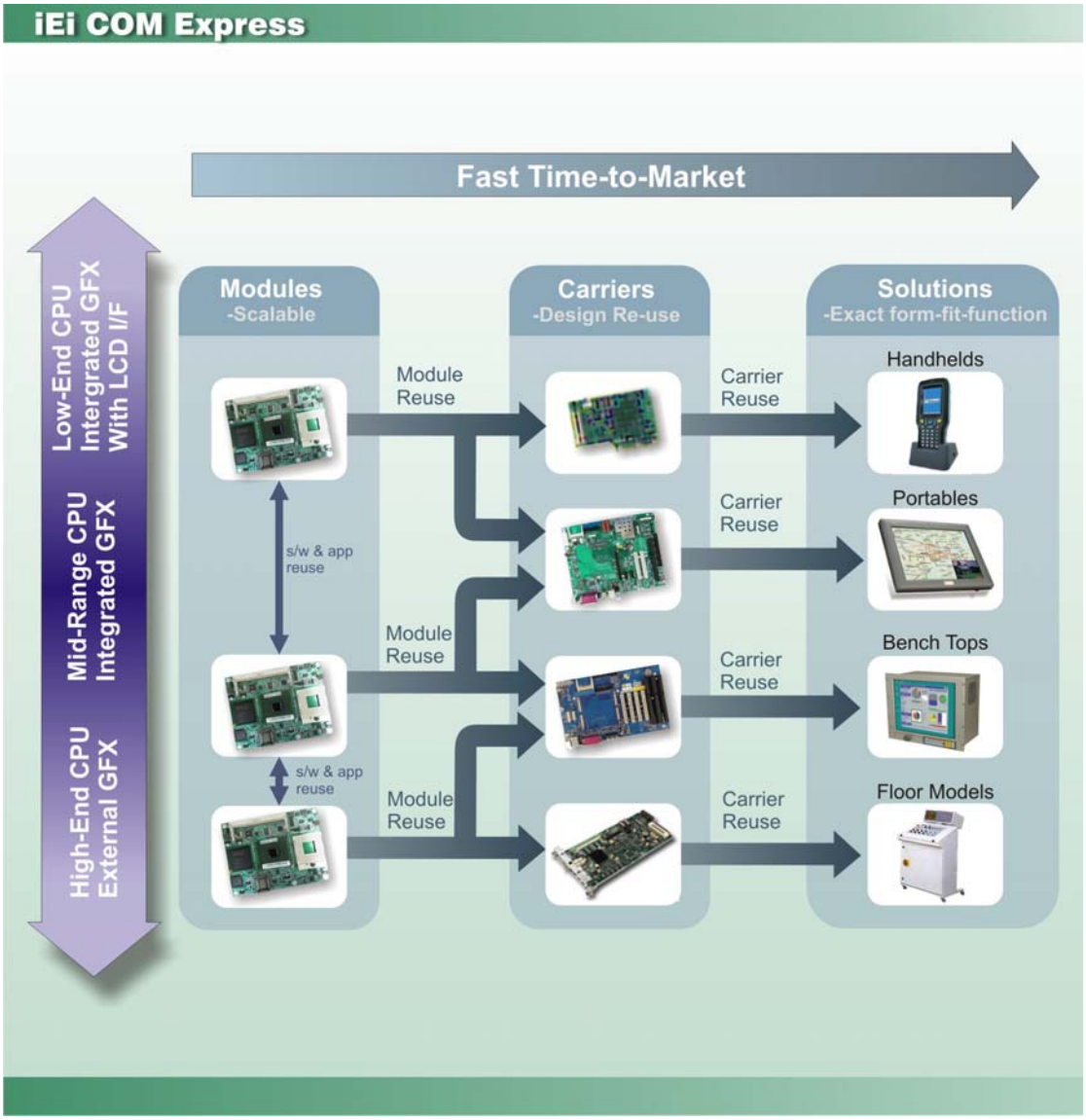


Figure 2-1: ICE Module Application

2.2 ICE Specifications

IEI provides many kinds of ICE modules for customers, including BGA type and socket type. Table 2-1 lists the IEI ICE modules and the specifications.

Table 2-1: IEI ICE Modules

ICE 910/915 Series	Description
ICE-9152-R10	COM Express Basic Type 2 Module, Socket 479 Intel® Pentium M CPU, VGA/LVDS, LAN, CF, SATA, USB 2.0 and Audio
ICE-9102-1GZ-R10	COM Express Basic Type 2 Module with Intel® Celeron® M 1G zero cache CPU, VGA/LVDS, LAN, CF, SATA, USB 2.0 and Audio
ICE-9102-1G512-R10	COM Express Basic Type 2 Module with Intel® Celeron® M 1G 512KB cache CPU, VGA/LVDS, LAN, CF, SATA, USB 2.0 and Audio
ICE Atom Series	**Description**
ICE-ATOM-R10	COM Express Basic Type 2 Module with Intel® Diamondville-SC Processor at FSB 533MHz, Intel® 945GSE/ICH7M Basic Mobile Platform supports
ICE GM45 Series	**Description**
ICE-GM45A-R10	COM Express Module with Intel® GM45/Penryn processor DDR2, GbE, LVDS/CRT/HDTV-out, SATAII, USB2.0
Carrier Board	**Description**
ICE-DB-9S-R10	Base Board for COM Express Type 2 modules
Others	**Description**

2.2.1 ICE-9152-R10

The ICE-9152 is shown in Figure 2-2 and the specifications are list in Table 2-2.

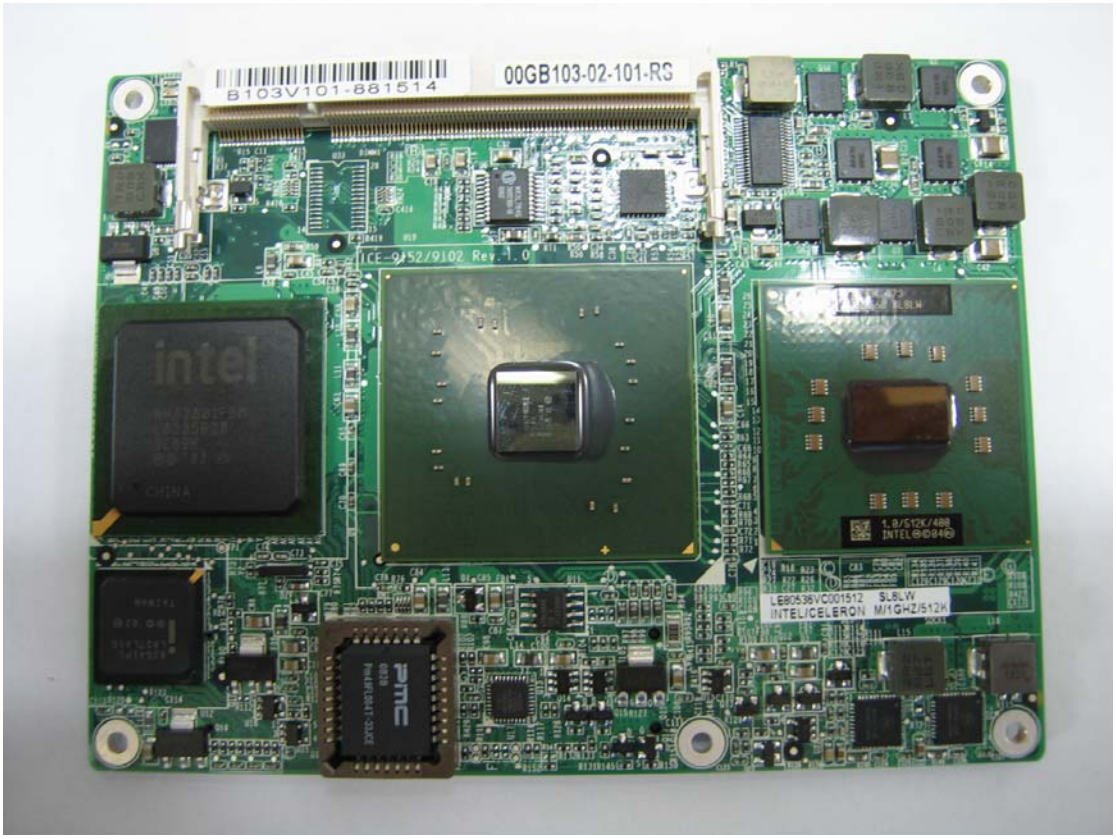


Figure 2-2: ICE-9152-R10

Table 2-2: ICE-9152-R10 Specification

Item	Description
CPU	Socket 479 Intel® Pentium® M, Celeron® M processor with a 533/400MHz FSB
System Memory	One 200-pin 533/400MHz DDR2 SDRAM SO-DIMM supported (system max. 2GB)
System Chipset	Intel® 915GME + ICH6M
BIOS	AMI Flash BIOS
WatchDog Timer	255 levels timer interval, from 1 to 255 sec or min setup by software, jumperless selection, generates system reset
Expansion Interface	1 x PCIe x16 signal to Base Board 4 x PCIe x1 signal to Base Board 4 x PCI , 32 bit / 33 MHz PCI bus Singal to Base Base Board
MIO	2 x SATA (Signal to Base Board) 1 x IDE channel (Signal to Base Board)
USB	8 x USB 2.0 (Signal to Base Board)

Audio	AC'97 Audio Signal to Base Board (Audio Codec on Base Board)
Ethernet	One Intel® 82541PI GbE Chipset (co-layout Intel® 82551ER 10/100Mbps Ethernet chipset) Signal to Base Board
CRT Display mode	VGA Integrated in Intel 915GME Signal (Signal to Base Board)
LCD Display mode	18/24-bit Dual channel LVDS Signal (to Base Board)
Dimensions (L x W)	125 mm x 95 mm
Power Supply Voltage	ATX / AT supported
Operating Temperature	0 ~ 60˚ C (32 ~ 140˚ F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing

2.2.2 ICE-9102-1GZ-R10

The ICE-9102-1GZ is shown in Figure 2-3 and the specifications are listed in Table 2-3.

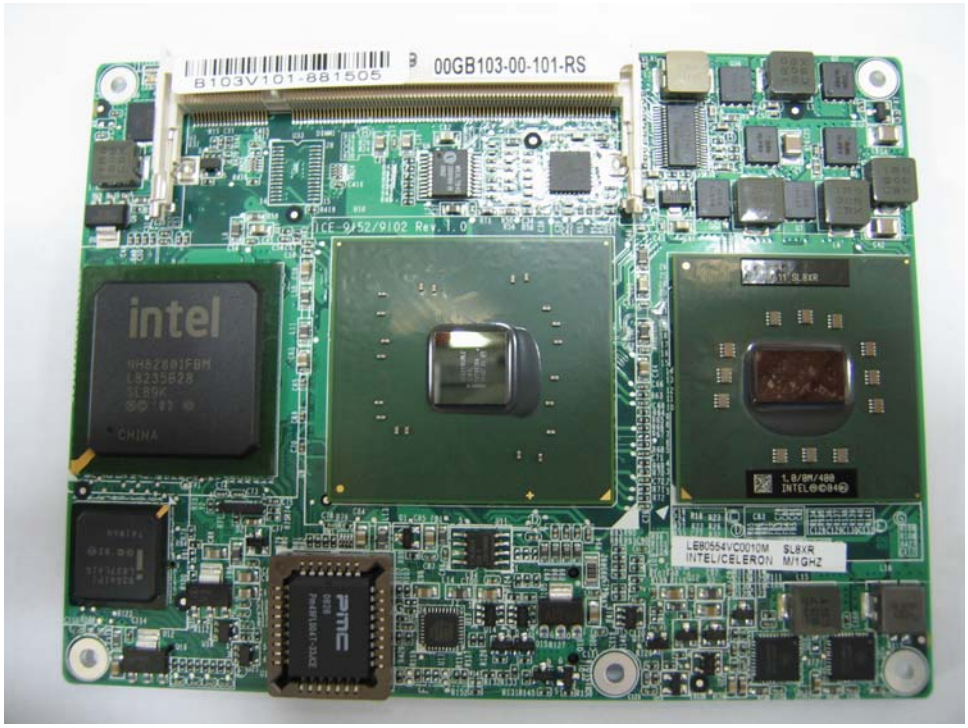


Figure 2-3: ICE-9102-1GZ-R10

Table 2-3: ICE-9102-1GZ-R10 Specification

Item	Description
CPU	On board Intel® Celeron® M 1GHz zero cache processor
System Memory	One 200-pin 400MHz DDR2 SDRAM SO-DIMM supported (system max. 2GB)
System Chipset	Intel® 910GMLE + ICH6-M
BIOS	AMI Flash BIOS
WatchDog Timer	Software programmable supports 1 ~255 sec. System reset
Expansion Interface	2 x SATA (Signal to Base Board) 1 x IDE channel (Signal to Base Board)
MIO	4 x PCIe x1 Signal to Base Board 4 x PCI , 32 bit / 33 MHz PCI bus Signal to Base Board
USB	8 x USB 2.0 (Signal to Base Board)
Audio	AC'97 Audio Signal to Base Board (Audio Codec on Base Board)
Ethernet	One Intel® 82541PI GbE Chipset (co-layout Intel® 82551ER 10/100Mbps Ethernet chipset)

	Singal to Base Board
CRT Display mode	VGA Integrated in Intel 910GMLE Signal (Signal to Base Board)
LCD Display mode	18/24-bit Dual channel LVDS Signal (Signal to Base Board)
Dimensions (L x W)	125 mm x 95 mm
Power Supply Voltage	ATX / AT supported
Operating Temperature	0 ~ 60˚ C (32 ~ 140˚ F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing

2.2.3 ICE-9102-1G512-R10

The ICE-9152-1G512 is shown in Figure 2-4 and the specifications are listed in Table 2-4.

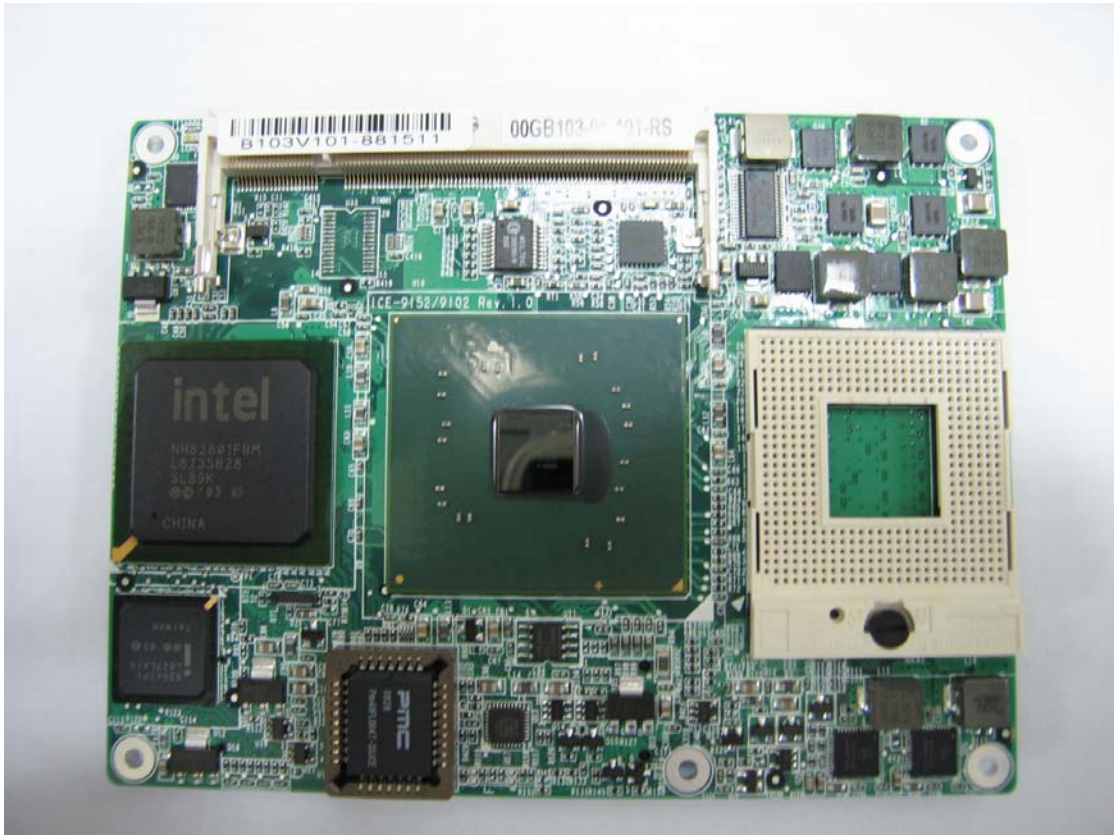


Figure 2-4: ICE-9102-1G512-R10

Table 2-4: ICE-9102-1G512-R10 Specification

Item	Description
CPU	On board Intel® Celeron® M 1GHz 512KB cache processor
System Memory	One 200-pin 400MHz DDR2 SDRAM SO-DIMM supported (system max. 2GB)
System Chipset	Intel® 910GMLE + ICH6-M
BIOS	AMI Flash BIOS
WatchDog Timer	Software programmable supports 1 ~255 sec. System reset
Expansion Interface	2 x SATA (Signal to Base Board) 1 x IDE channel (Signal to Base Board)
MIO	4 x PCIe x1 Signal to Base Board 4 x PCI , 32 bit / 33 MHz PCI bus Signal to Base Board
USB	8 x USB 2.0 (Signal to Base Board)
Audio	AC'97 Audio Signal to Base Board (Audio Codec on

	Base Board)
Ethernet	One Intel® 82541PI GbE Chipset (co-layout Intel® 82551ER 10/100Mbps Ethernet chipset) Signal to Base Board
CRT Display mode	VGA Integrated in Intel 910GMLE Signal (Signal to Base Board)
LCD Display mode	18/24-bit Dual channel LVDS Signal (Signal to Base Board)
Dimensions (L x W)	125 mm x 95 mm
Power Supply Voltage	ATX / AT supported
Operating Temperature	0 ~ 60˚ C (32 ~ 140˚ F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing

2.2.4 ICE-ATOM-R10

The ICE-ATOM is shown in Figure 2-5 and the specifications are listed in Table 2-5.

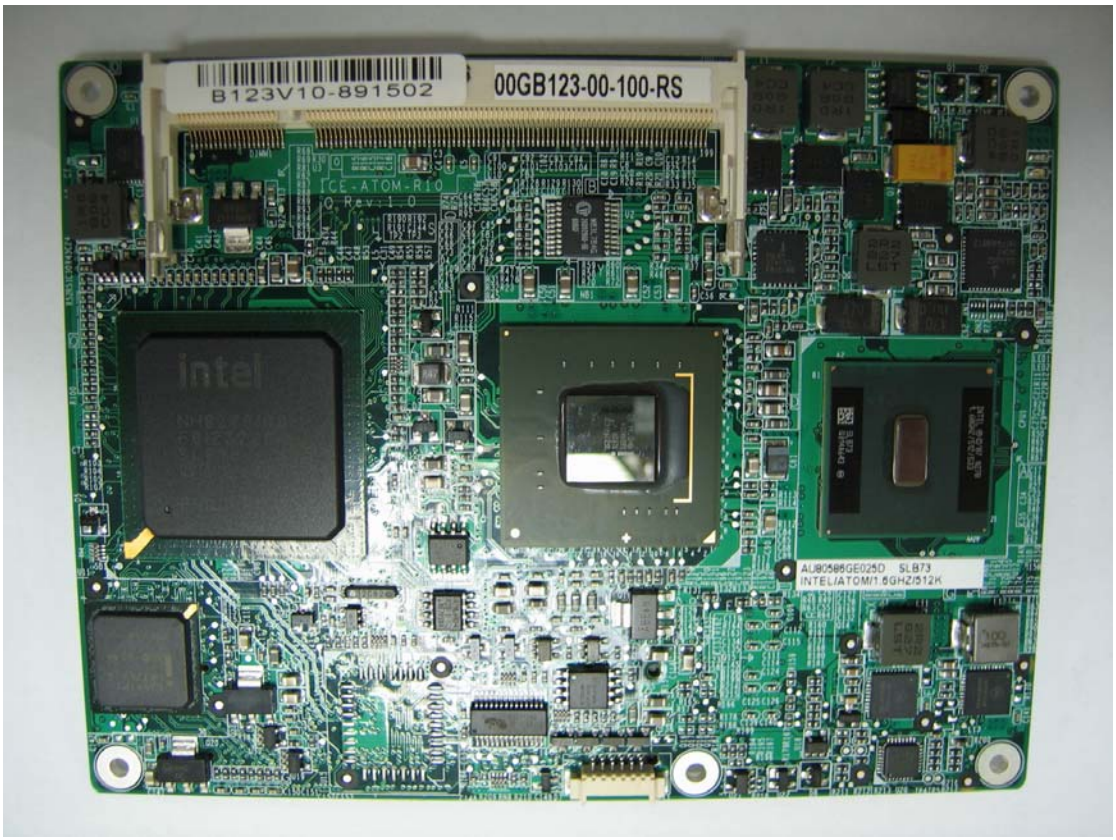


Figure 2-5: ICE-ATOM-R10

Table 2-5: ICE-ATOM-R10 Specification

Item	Description
CPU	Intel Diamondville-SC support at FSB 533Mhz
System Memory	1x DDR2 SO-DIMM 400/533MHz support up to 2GB
System Chipset	Intel 945GSE + ICH7M
BIOS	AMI BIOS
WatchDog Timer	Sofware Programmable support 1~255 sec. System reset
Audio	HD Audio Signal to Base Board (Audio Codec on Base Board)
MIO	2 x SATA II (Signal to Base Board) 1 x IDE channel (Signal to Base Board)
USB	8 USB ports, USB 2.0 (Signal to Base Board)
Ethernet	1 x Intel® 82541PI GbE Chipset (co-layout Intel® 82551ER 10/100Mbps Ethernet chipset) (Signal to Base Board)
Display	Analog CRT(VGA) Integrated in Intel® 945GSE (Signal

	to Base Board) 18-bits Dual Channel LVDS Signal (Signal to Base Board) HDTV-out (Signal to Base Board) 1 x SDVO Interface (Only SDVO Port_B)
Dimensions (L x W)	125 mm x 95 mm
Power Supply Voltage	AT/ATX support
Operating Temperature	0 ~ 60° C (32 ~ 140° F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing system

2.2.5 ICE-GM45A-R10

The ICE-GM45A is shown in Error! Reference source not found. and the specifications are listed in **Table 2-6**.

Table 2-6: ICE-GM45A-R10 Specification

Item	Description
CPU	Socket P Intel® mobile Core™ 2 Duo(Penryn), Intel® Celeron® M
System Memory	2 x 200-pins 1066/800MHz DDR2 SDRAM SO-DIMM Supported
System Chipset	Intel® GM45 + Intel® ICH9M
BIOS	AMI BIOS
WatchDog Timer	Software programmable supports 1 ~255 sec. System reset
Audio	HD Audio Signal to Base Board (Audio Codec on Base Board)
MIO	4 x SATA II (Signal to Base Board) 1 x IDE channel (Signal to Base Board)
Expansion	1 x PCIe x16 signal to Base Board 4 x PCIe x1 signal to Base Board 4 x PCI, 32 bit / 33 MHz PCI bus to Base Board
USB	8 x USB 2.0 (Signal to Base Board)
Ethernet	1 x Intel 82574L GbE chipset (Signal to Base Board)
Display	Analog CRT(VGA) Integrated in Intel® GM45 (Signal to Base Board) 18/24-bits Dual-Channel LVDS (Signal to Base Board) HDTV-out (Signal to Base Board)
Dimensions (L x W)	125 mm x 95 mm
Power Supply Voltage	ATX/AT supported
Operating Temperature	0 ~ 60° C (32 ~ 140° F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing system

2.2.6 ICE-DB-9S-R10

The ICE-DB-9S is a full function carrier board for customers to apply or test the COM Express module. The carrier board can be used for any combination, including software and hardware. Using the carrier board to develop and test the ICE module also can achieve a quicker time to market. The ICE-DB-9S is shown in Figure 2-6 and the specifications are listed in **Table 2-7**.

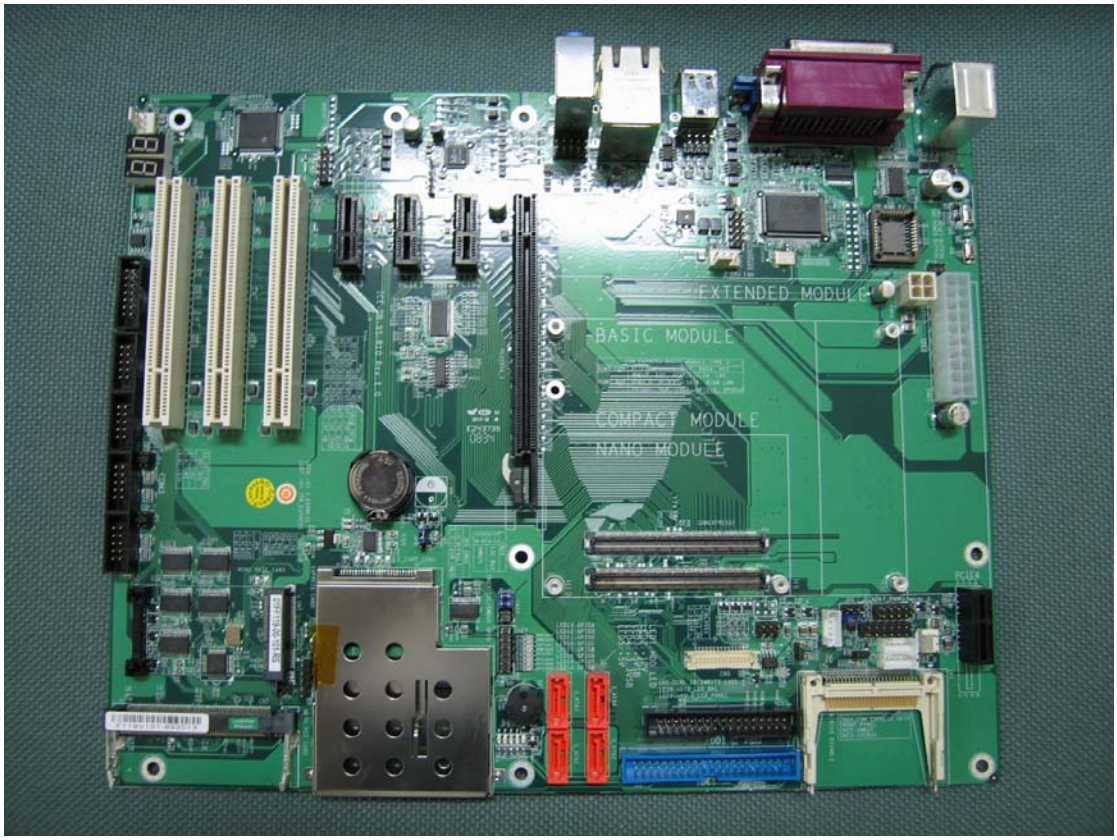


Figure 2-6: ICE-DB-9S-R10

Table 2-7: ICE-DB-9S-R10 Specification

Item	Description
CPU module interface	Supports COM Express Compact/Basic/Extended modules using connector pin out Type 2
Audio	Realtek ALC888 7.1 channels HD audio codec Front Audio by pin-header(Line in, Line out, Mic in) SPDIF by pin-header CD-IN by pin-header
MIO	1 x PCIe by 16 Slot 4 x PCIe by 1 Slot 3 x PCI Slot 1 x PCIe Mini card Slot 1 x Express Card Slot 1 x Mini PCI Card Slot

	1 x ISA 1 x IDE 2/4 x SATA/SATA II 1 x CF type II Slot 6 x USB 2.0 1 x LPT 1 x FDD 5 x RS-232 1 x RS-232/422/485 2 x USB 2.0 to PCIe Mini card Slot & Express Card Slot
Ethernet	1 x RJ-45 GbE connector
Display	VGA DB15 connector 1 x 18/24 bit dual channel LVDS Connector 1 x Inverter connector 1 x TV-out interface
Dimensions (L x W)	304.8 mm x 190.5 mm (12" x 7.5")
Power Supply Voltage	ATX / AT support
Operating Temperature	0 ~ 60° C (32 ~ 140° F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing system

2.3 Performance

Company	IEI	IEI	IEI	
Model Name	ICE-9102-1G512-R10	ICE-9102-1GZ-R10	ICE-9152-R10	
CPU	Celeron M 1GHz	Celeron M 1GHz	Pentium M 1.5G	
FSB	400MHz	400MHz	400MHz	
L2 Cache	512K	0	1GHz	
Chipset	910GMLE+ICH6M	910GMLE+ICH6M	915GME+ICH6M	
Memory	Kingston D2/1G/533	Kingston D2/1G/533	Kingston D2/1G/533	
HDD	WD WD800JD 80GB SATA	D WD800JD 80GB SA	WD WD800JD 80GB SATA	
Power Supply	Seventeam ST-300BKV 300W	Seventeam ST-300BKV 300W	Seventeam ST-300BKV 300W	
DVD ROM	TEAC DVD ROM	TEAC DVD ROM	TEAC DVD ROM	
BackPlane	ICE-DB-9S-R10	ICE-DB-9S-R10	ICE-DB-9S-R10	

3D Mark 2001				
Overall Score	2782	2139	3596	

	Sandra Perfessional 2003				
PU Benchm	Dhrystone ALU	3338	3326	5012	
	Whetstone FPU/SSE	1329/1979	1324/1972	2008/2967	
CPU Multi-	Integer iSSE	5692	5671	8537	
	Float iSSE	6581	6559	9903	
Memory B	RAM Bandwidth Int B	2027	1156	1982	
	RAM Bandwidth Floa	2031	1151	1979	

HCT 12.1				
12V	1.33	1.33	2.09	
5VSB	0	0	0	
BAT	0	0	0	
Watt	15.96	15.96	25.08	0

Idel				
12V	1.12	1.13	1.44	
5VSB	0	0	0	
BAT	0	0	0	
Watt	13.44	13.56	17.28	0

Chapter

3

Pin Assignments

3.1 Chapter Overview

This chapter describes pin assignments and I/O characteristics for COM Express modules. The carrier board uses two 220-pin 0.5 mm fine pitch board-to-board connectors. There are five different pin-out types currently defined by the COM Express Specification. The preferred choice of the embedded computer industry is the Type 2 pin-out and therefore the leading manufacturers have chosen to produce COM Express Type 2 modules. This pin-out offers the best balance between older technology such as PCI and Parallel ATA while providing the latest technologies including PCI Express, Serial ATA and PCI Express graphics.

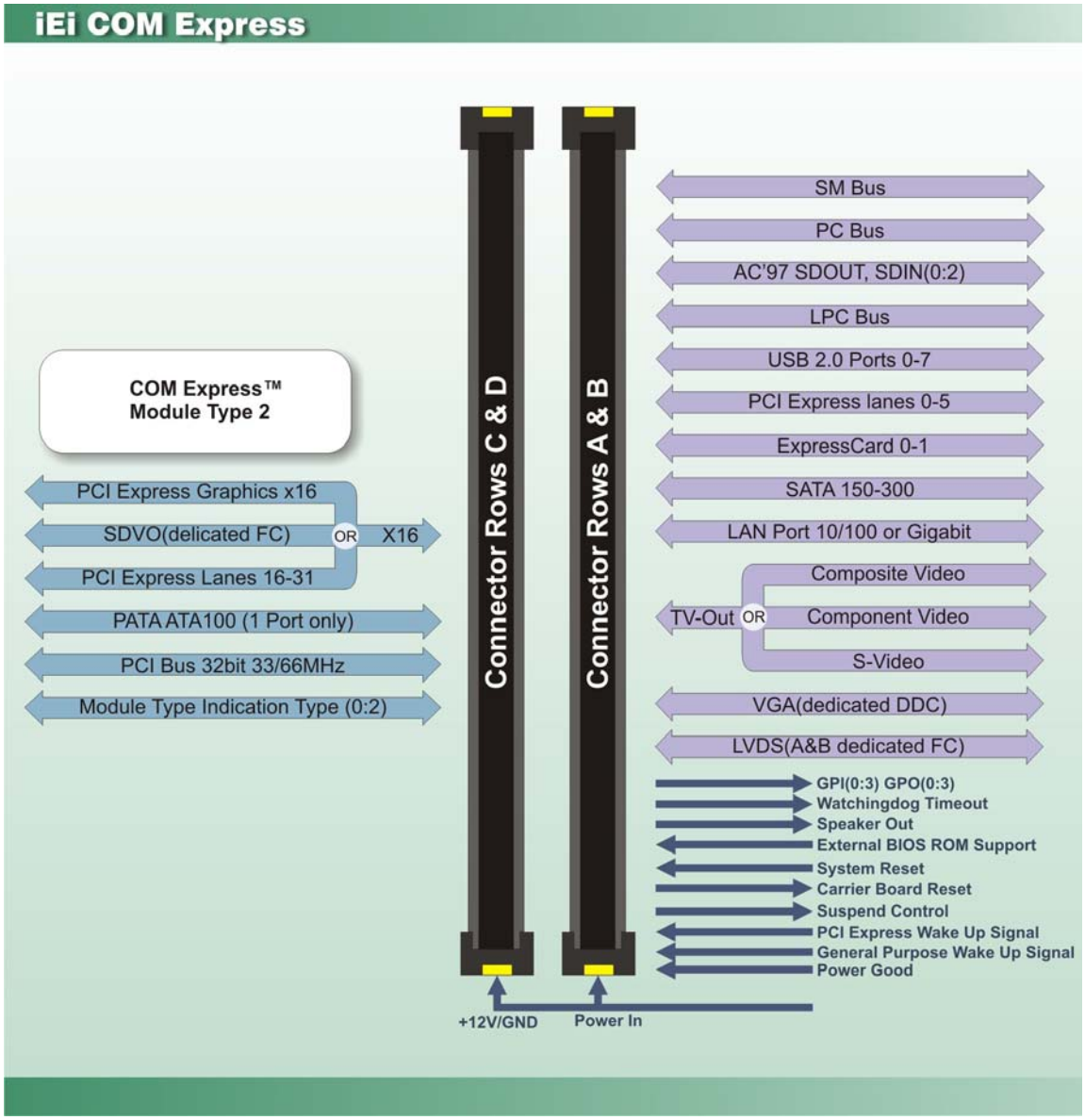


Figure 3-1: COM Express Type 2 Module Diagram

3.2 Type 1, Type 2, Type 3, Type 4 and Type 5

The differences among the Module Types are summarized in Table 3-1.

- Module Type 1 supports a single connector with two rows of pins (220 pins total).
- Module Types 2-5 support two connectors with four rows of pins (440 pins total).

Connector placement and most mounting holes have transparency between Form Factors.

Table 3-1

Module Type	Rows	PCIe Lanes (max)	PCI	IDE	LAN (Max)
1	AB	6	X	X	1
2 (Default)	AB, CD	22	V	V	1
3	AB, CD	22	X	V	3
4	AB, CD	32	V	X	1
5	AB, CD	32	X	X	3

3.3 Signal Table Terminology

The following section describes the signals found on COM Express Type 2 connectors. Most of the signals listed in the following sections also apply to other COM Express module types. The pinout for connector rows A and B remains the same regardless of the module type but the pinout for connector rows D and C are dependent on the module type. Refer to the COM Express specification for information about the different pin-outs of the module types other than Type 2.

Table 3-2 below describes the terminology used in this section for the Signal Description tables. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

Table 3-2: Conventions and Terminology

Term	Description
I/O	Bi-directional signal
I	Input signal
O	Output signal
I/F	Interface
GND	Ground
PWR	Power
OD	Open drain output
PD	Pull down
PU	Pull up
+V12	+12V ±5% Volts Normal Power
+V5SB	+5V ±5% Standby Power
+3.3VSB	+3.3V ±5% Standby Power
+V3.3	+3.3V ±5% Volts Normal Power
+V5	+5V ±5% Volts Normal Power
#	Active-Low Signals
'+' and '-'	Differential Pairs
PM	Power Management
GBE	Giga Bits Ethernet

3.4 Connector Pinout Row A and Row B

Table 3-3: Module Type 2 Connector Pinout Rows (A and B)

Pin	Signal	I/F	I/O	Pin	Signal	I/F	I/O
A1	GND	GND	-	**B1**	GND	GND	-
A2	GBE0_MDI3-	GBE	I/O	**B2**	GBE0_ACT#	GBE	O 3.3V
A3	GBE0_MDI3+	GBE	I/O	**B3**	LPC_FRAME#	LPC	O 3.3V
A4	GBE0_LINK100#	GBE	O 3.3V	**B4**	LPC_AD0	LPC	I/O 3.3V
A5	GBE0_LINK1000#	GBE	O 3.3V	**B5**	LPC_AD1	LPC	I/O 3.3V
A6	GBE0_MDI2-	GBE	I/O	**B6**	LPC_AD2	LPC	I/O 3.3V
A7	GBE0_MDI2+	GBE	I/O	**B7**	LPC_AD3	LPC	I/O 3.3V
A8	GBE0_LINK#	GBE	O 3.3V	**B8**	LPC_DRQ0#	LPC	I 3.3V
A9	GBE0_MDI1-	GBE	I/O	**B9**	LPC_DRQ1#	LPC	I 3.3V
A10	GBE0_MDI1+	GBE	I/O	**B10**	LPC_CLK	LPC	O 3.3V
A11	GND	GND	-	**B11**	GND	GND	-
A12	GBE0_MDI0-	GBE	I/O	**B12**	PWRBTN#	PM	I
A13	GBE0_MDI0+	GBE	I/O	**B13**	SMB_CK	SMB	-
A14	GBE0_CTREF	GBE		**B14**	SMB_DAT	SMB	-
A15	SUS_S3#	PM	O	**B15**	SMB_ALERT#	SMB	I
A16	SATA0_TX+	SATA	O	**B16**	SATA1_TX+	SATA	O
A17	SATA0_TX-	SATA	O	**B17**	SATA1_TX-	SATA	O
A18	SUS_S4#	PM	O	**B18**	SUS_STAT#	PM	O
A19	SATA0_RX+	SATA	I	**B19**	SATA1_RX+	SATA	I
A20	SATA0_RX-	SATA	I	**B20**	SATA1_RX-	SATA	I
A21	GND	GND	-	**B21**	GND	GND	-
A22	SATA2_TX+	SATA	O	**B22**	SATA3_TX+	SATA	O
A23	SATA2_TX-	SATA	O	**B23**	SATA3_TX-	SATA	O
A24	SUS_S5#	PM	O	**B24**	PWR_OK	PM	I
A25	SATA2_RX+	SATA	I	**B25**	SATA3_RX+	SATA	I
A26	SATA2_RX-	SATA	I	**B26**	SATA3_RX-	SATA	I
A27	BATLOW#	PM	I	**B27**	WDT	-	-
A28	ATA_ACT#	SATA	O 3.3V	**B28**	AC_SDIN2	HDA	I 3.3V
A29	AC_SYNC	HDA	O 3.3V	**B29**	AC_SDIN1	HDA	I 3.3V
A30	AC_RST#	HDA	O 3.3V	**B30**	AC_SDIN0	HDA	I 3.3V
A31	GND	GND	-	**B31**	GND	GND	-
A32	AC_BITCLK	HDA	O 3.3V	**B32**	SPKR	-	-
A33	AC_SDOUT	HAD	O 3.3V	**B33**	I2C_CK	I2C	-
A34	BIOS_DISABLE#	-	-	**B34**	I2C_DAT	I2C	-
A35	THRMTRIP#	PM	O	**B35**	THRM#	PM	I
A36	USB6-	USB	I/O	**B36**	USB7-	USB	I/O
A37	USB6+	USB	I/O	**B37**	USB7+	USB	I/O
A38	USB_6_7_OC#	USB	I 3.3V	**B38**	USB_4_5_OC#	USB	I 3.3V
A39	USB4-	USB	I/O	**B39**	USB5-	USB	I/O
A40	USB4+	USB	I/O	**B40**	USB5+	USB	I/O
A41	GND	GND	-	**B41**	GND	GND	-
A42	USB2-	USB	I/O	**B42**	USB3-	USB	I/O
A43	USB2+	USB	I/O	**B43**	USB3+	USB	I/O
A44	USB_2_3_OC#	USB	I 3.3V	**B44**	USB_0_1_OC#	USB	I 3.3V
A45	USB0-	USB	I/O	**B45**	USB1-	USB	I/O
A46	USB0+	USB	I/O	**B46**	USB1+	USB	I/O
A47	VCC_RTC	PWR	--	**B47**	EXCD1_PERST#	PCIE	-
A48	EXCD0_PERST#	PCIE	-	**B48**	EXCD1_CPPE#	PCIE	-
A49	EXCD0_CPPE#	PCIE	-	**B49**	SYS_RESET#	PM	I
A50	LPC_SERIRQ	LPC	I/O 3.3V	**B50**	CB_RESET#	PM	O

A51	GND	GND	-	**B51**	GND	GND	-
A52	PCIE_TX5+	PCIE	O	**B52**	PCIE_RX5+	PCIE	I
A53	PCIE_TX5-	PCIE	O	**B53**	PCIE_RX5-	PCIE	I
A54	GPI0	-	-	**B54**	GPO1	-	-
A55	PCIE_TX4+	PCIE	O	**B55**	PCIE_RX4+	PCIE	I
A56	PCIE_TX4-	PCIE	O	**B56**	PCIE_RX4-	PCIE	I
A57	GND	GND	-	**B57**	GPO2		--
A58	PCIE_TX3+	PCIE	O	**B58**	PCIE_RX3+	PCIE	I
A59	PCIE_TX3-	PCIE	O	**B59**	PCIE_RX3-	PCIE	I
A60	GND	GND	-	**B60**	GND	GND	-
A61	PCIE_TX2+	PCIE	O	**B61**	PCIE_RX2+	PCIE	I
A62	PCIE_TX2-	PCIE	O	**B62**	PCIE_RX2-	PCIE	I
A63	GPI1	-	-	**B63**	GPO3	-	-
A64	PCIE_TX1+	PCIE	O	**B64**	PCIE_RX1+	PCIE	I
A65	PCIE_TX1-	PCIE	O	**B65**	PCIE_RX1-	PCIE	I
A66	GND	GND	-	**B66**	WAKE0#	PCIE	I
A67	GPI2	-	-	**B67**	WAKE1#	PM	I
A68	PCIE_TX0+	PCIE	O	**B68**	PCIE_RX0+	PCIE	I
A69	PCIE_TX0-	PCIE	O	**B69**	PCIE_RX0-	PCIE	I
A70	GND	GND	-	**B70**	GND	GND	-
A71	LVDS_A0+	LVDS	O	**B71**	LVDS_B0+	LVDS	O
A72	LVDS_A0-	LVDS	O	**B72**	LVDS_B0-	LVDS	O
A73	LVDS_A1+	LVDS	O	**B73**	LVDS_B1+	LVDS	O
A74	LVDS_A1-	LVDS	O	**B74**	LVDS_B1-	LVDS	O
A75	LVDS_A2+	LVDS	O	**B75**	LVDS_B2+	LVDS	O
A76	LVDS_A2-	LVDS	O	**B76**	LVDS_B2-	LVDS	O
A77	LVDS_VDD_EN	LVDS	O 3.3V	**B77**	LVDS_B3+	LVDS	O
A78	LVDS_A3+	LVDS	O	**B78**	LVDS_B3-	LVDS	O
A79	LVDS_A3-	LVDS	O	**B79**	LVDS_BKLT_EN	LVDS	O 3.3V
A80	GND	GND	-	**B80**	GND	GND	-
A81	LVDS_A_CK+	LVDS	O	**B81**	LVDS_B_CK+	LVDS	O
A82	LVDS_A_CK-	LVDS	O	**B82**	LVDS_B_CK-	LVDS	O
A83	LVDS_I2C_CK	LVDS	O 3.3V	**B83**	LVDS_BKLT_CTRL	LVDS	O 3.3V
A84	LVDS_I2C_DAT	LVDS	IO 3.3V	**B84**	5VSB	PWR	-
A85	GPI3	-	-	**B85**	5VSB	PWR	-
A86	KBD_RST#	KB/MS		**B86**	5VSB	PWR	-
A87	KBD_A20GATE			**B87**	5VSB	PWR	-
A88	PCIE0_CK_REF+			**B88**	RSVD	-	-
A89	PCIE0_CK_REF-			**B89**	VGA_RED	VGA	
A90	GND			**B90**	GND	GND	-
A91	RSVD	-	-	**B91**	VGA_GRN	VGA	
A92	RSVD	-	-	**B92**	VGA_BLU	VGA	
A93	GPO0			**B93**	VGA_HSYNC	VGA	
A94	RSVD	-	-	**B94**	VGA_VSYNC	VGA	
A95	RSVD	-	-	**B95**	VGA_I2C_CK	VGA	
A96	GND	GND		**B96**	VGA_I2C_DAT	VGA	
A97	+V12	PWR	-	**B97**	TV_DAC_A	TV	
A98	+V12	PWR	-	**B98**	TV_DAC_B	TV	
A99	+V12	PWR	-	**B99**	TV_DAC_C	TV	
A100	GND	GND		**B100**	GND	GND	-
A101	+V12	PWR	-	**B101**	+V12	PWR	-
A102	+V12	PWR	-	**B102**	+V12	PWR	-
A103	+V12	PWR	-	**B103**	+V12	PWR	-
A104	+V12	PWR	-	**B104**	+V12	PWR	-
A105	+V12	PWR	-	**B105**	+V12	PWR	-
A106	+V12	PWR	-	**B106**	+V12	PWR	-

A107	+V12	PWR	-	**B107**	+V12	PWR	-
A108	+V12	PWR	-	**B108**	+V12	PWR	-
A109	+V12	PWR	-	**B109**	+V12	PWR	-
A110	GND	GND	-	**B110**	GND	GND	-

3.5 Connector Pinout Rows C and D

Table 3-4: Module Type 2 Connector Pinout Rows (C and D)

Pin	Signal	I/F	I/O	Pin	Signal	I/F	I/O
C1	GND	GND	-	**D1**	GND	GND	-
C2	IDE_D7	IDE	IO 3.3V	**D2**	IDE_D5	IDE	IO 3.3V
C3	IDE_D6	IDE	IO 3.3V	**D3**	IDE_D10	IDE	IO 3.3V
C4	IDE_D3	IDE	IO 3.3V	**D4**	IDE_D11	IDE	IO 3.3V
C5	IDE_D15	IDE	IO 3.3V	**D5**	IDE_D12	IDE	IO 3.3V
C6	IDE_D8	IDE	IO 3.3V	**D6**	IDE_D4	IDE	IO 3.3V
C7	IDE_D9	IDE	IO 3.3V	**D7**	IDE_D0	IDE	IO 3.3V
C8	IDE_D2	IDE	IO 3.3V	**D8**	IDE_REQ	IDE	I 3.3V
C9	IDE_D13	IDE	IO 3.3V	**D9**	IDE_IOW#	IDE	O 3.3V
C10	IDE_D1	IDE	IO 3.3V	**D10**	IDE_ACK#	IDE	O 3.3V
C11	GND	GND	-	**D11**	GND	GND	-
C12	IDE_D14	IDE	IO 3.3V	**D12**	IDE_IRQ	IDE	I 3.3V
C13	IDE_IORDY	IDE	I 3.3V	**D13**	IDE_A0	IDE	O 3.3V
C14	IDE_IOR#	IDE	O 3.3V	**D14**	IDE_A1	IDE	O 3.3V
C15	PCI_PME#	PCI	IO 3.3V	**D15**	IDE_A2	IDE	O 3.3V
C16	PCI_GNT2#	PCI	O 3.3V	**D16**	IDE_CS1#	IDE	O 3.3V
C17	PCI_REQ2#	PCI	I 3.3V	**D17**	IDE_CS3#	IDE	O 3.3V
C18	PCI_GNT1#	PCI	O 3.3V	**D18**	IDE_RESET#	IDE	IO 3.3V
C19	PCI_REQ1#	PCI	I 3.3V	**D19**	PCI_GNT3#	PCI	O 3.3V
C20	PCI_GNT0#	PCI	O 3.3V	**D20**	PCI_REQ3#	PCI	I 3.3V
C21	GND	GND	-	**D21**	GND	GND	-
C22	PCI_REQ0#	PCI	I 3.3V	**D22**	PCI_AD1	PCI	IO 3.3V
C23	PCI_RESET#	PCI	O 3.3V	**D23**	PCI_AD3	PCI	IO 3.3V
C24	PCI_AD0	PCI	IO 3.3V	**D24**	PCI_AD5	PCI	IO 3.3V
C25	PCI_AD2	PCI	IO 3.3V	**D25**	PCI_AD7	PCI	IO 3.3V
C26	PCI_AD4	PCI	IO 3.3V	**D26**	PCI_C/BE0#	PCI	IO 3.3V
C27	PCI_AD6	PCI	IO 3.3V	**D27**	PCI_AD9	PCI	IO 3.3V
C28	PCI_AD8	PCI	IO 3.3V	**D28**	PCI_AD11	PCI	IO 3.3V
C29	PCI_AD10	PCI	IO 3.3V	**D29**	PCI_AD13	PCI	IO 3.3V
C30	PCI_AD12	PCI	IO 3.3V	**D30**	PCI_AD15	PCI	IO 3.3V
C31	GND	GND	-	**D31**	GND	GND	-
C32	PCI_AD14	PCI	IO 3.3V	**D32**	PCI_PAR	PCI	IO 3.3V
C33	PCI_C/BE1#	PCI	IO 3.3V	**D33**	PCI_SERR#	PCI	IO 3.3V
C34	PCI_PERR#	PCI	IO 3.3V	**D34**	PCI_STOP#	PCI	IO 3.3V
C35	PCI_LOCK#	PCI	IO 3.3V	**D35**	PCI_TRDY#	PCI	IO 3.3V
C36	PCI_DEVSEL#	PCI	IO 3.3V	**D36**	PCI_FRAME#	PCI	IO 3.3V
C37	PCI_IRDY#	PCI	IO 3.3V	**D37**	PCI_AD16	PCI	IO 3.3V
C38	PCI_C/BE2#	PCI	IO 3.3V	**D38**	PCI_AD18	PCI	IO 3.3V
C39	PCI_AD17	PCI	IO 3.3V	**D39**	PCI_AD20	PCI	IO 3.3V
C40	PCI_AD19	PCI	IO 3.3V	**D40**	PCI_AD22	PCI	IO 3.3V
C41	GND	GND	-	**D41**	GND	GND	-
C42	PCI_AD21	PCI	IO 3.3V	**D42**	PCI_AD24	PCI	IO 3.3V
C43	PCI_AD23	PCI	IO 3.3V	**D43**	PCI_AD26	PCI	IO 3.3V
C44	PCI_C/BE3#	PCI	IO 3.3V	**D44**	PCI_AD28	PCI	IO 3.3V
C45	PCI_AD25	PCI	IO 3.3V	**D45**	PCI_AD30	PCI	IO 3.3V

C46	PCI_AD27	PCI	IO 3.3V	**D46**	PCI_IRQC#	PCI	I 3.3V
C47	PCI_AD29	PCI	IO 3.3V	**D47**	PCI_IRQD#	PCI	I 3.3V
C48	PCI_AD31	PCI	IO 3.3V	**D48**	PCI_CLKRUN#	PCI	I/O 3.3V
C49	PCI_IRQA#	PCI	I 3.3V	**D49**	PCI_M66EN	PCI	I 3.3V
C50	PCI_IRQB#	PCI	I 3.3V	**D50**	PCI_CLK	PCI	OI 3.3V
C51	GND	GND	-	**D51**	GND	GND	-
C52	PEG_RX0+	PEG	I	**D52**	PEG_TX0+	PEG	O
C53	PEG_RX0-	PEG	I	**D53**	PEG_TX0-	PEG	O
C54	TYPE0#			**D54**	PEG_LANE_RV#		
C55	PEG_RX1+	PEG	I	**D55**	PEG_TX1+	PEG	O
C56	PEG_RX1-	PEG	I	**D56**	PEG_TX1-	PEG	O
C57	TYPE1#			**D57**	TYPE2#		
C58	PEG_RX2+	PEG	I	**D58**	PEG_TX2+	PEG	O
C59	PEG_RX2-	PEG	I	**D59**	PEG_TX2-	PEG	O
C60	GND	GND	-	**D60**	GND	GND	-
C61	PEG_RX3+	PEG	I	**D61**	PEG_TX3+	PEG	O
C62	PEG_RX3-	PEG	I	**D62**	PEG_TX3-	PEG	O
C63	RSVD	-	-	**D63**	RSVD	-	-
C64	RSVD	-	-	**D64**	RSVD	-	-
C65	PEG_RX4+	PEG	I	**D65**	PEG_TX4+	PEG	O
C66	PEG_RX4-	PEG	I	**D66**	PEG_TX4-	PEG	O
C67	FAN_PWMOUT	-	O	**D67**	GND	GND	-
C68	PEG_RX5+	PEG	I	**D68**	PEG_TX5+	PEG	O
C69	PEG_RX5-	PEG	I	**D69**	PEG_TX5-	PEG	O
C70	GND	GND	-	**D70**	GND	GND	-
C71	PEG_RX6+	PEG	I	**D71**	PEG_TX6+	PEG	O
C72	PEG_RX6-	PEG	I	**D72**	PEG_TX6-	PEG	O
C73	SDVO_DATA			**D73**	SVDO_CLK		
C74	PEG_RX7+	PEG	I	**D74**	PEG_TX7+	PEG	O
C75	PEG_RX7-	PEG	I	**D75**	PEG_TX7-	PEG	O
C76	GND	GND	-	**D76**	GND	GND	-
C77	FAN_TACHOIN	-	I	**D77**	IDE_CBLID#	IDE	I 3.3V
C78	PEG_RX8+	PEG	I	**D78**	PEG_TX8+	PEG	O
C79	PEG_RX8-	PEG	I	**D79**	PEG_TX8-	PEG	O
C80	GND	GND	-	**D80**	GND	GND	-
C81	PEG_RX9+	PEG	I	**D81**	PEG_TX9+	PEG	O
C82	PEG_RX9-	PEG	I	**D82**	PEG_TX9-	PEG	O
C83	RSVD			**D83**	RSVD		
C84	GND	GND	-	**D84**	GND	GND	-
C85	PEG_RX10+	PEG	I	**D85**	PEG_TX10+	PEG	O
C86	PEG_RX10-	PEG	I	**D86**	PEG_TX10-	PEG	O
C87	GND	GND	-	**D87**	GND	GND	-
C88	PEG_RX11+	PEG	I	**D88**	PEG_TX11+	PEG	O
C89	PEG_RX11-	PEG	I	**D89**	PEG_TX11-	PEG	O
C90	GND	GND	-	**D90**	GND	GND	-
C91	PEG_RX12+	PEG	I	**D91**	PEG_TX12+	PEG	O
C92	PEG_RX12-	PEG	I	**D92**	PEG_TX12-	PEG	O
C93	GND	GND	-	**D93**	GND	GND	-
C94	PEG_RX13+	PEG	I	**D94**	PEG_TX13+	PEG	O
C95	PEG_RX13-	PEG	I	**D95**	PEG_TX13-	PEG	O
C96	GND	GND	-	**D96**	GND	GND	-
C97	RSVD	-	-	**D97**	PEG_ENABLE#		
C98	PEG_RX14+	PEG	I	**D98**	PEG_TX14+	PEG	O
C99	PEG_RX14-	PEG	I	**D99**	PEG_TX14-	PEG	O
C100	GND	GND	-	**D100**	GND	GND	-
C101	PEG_RX15+	PEG	I	**D101**	PEG_TX15+	PEG	O

C102	PEG_RX15-	PEG	I	**D102**	PEG_TX15-	PEG	O
C103	GND	GND	-	**D103**	GND	GND	-
C104	+V12	PWR	-	**D104**	+V12	PWR	-
C105	+V12	PWR	-	**D105**	+V12	PWR	-
C106	+V12	PWR	-	**D106**	+V12	PWR	-
C107	+V12	PWR	-	**D107**	+V12	PWR	-
C108	+V12	PWR	-	**D108**	+V12	PWR	-
C109	+V12	PWR	-	**D109**	+V12	PWR	-
C110	GND	GND	-	**D110**	GND	GND	-

Chapter

4

Signal Description and Routing Guideline

4.1 PEG (PCI Express Graphic)

The PEG Port can utilize COM Express PCIe lanes 16-32 and is suitable to drive a x16 link for an external high-performance PCI Express Graphics card, if implemented on the COM Express module. It supports a theoretical bandwidth of up to 4 GB/s – twice the peak bandwidth achievable with AGP 8x. Each lane of the PEG Port consists of a receiver and transmit differential signal pair designated 'PEG_RX0' (+ and -) to 'PEG_RX15' (+ and -) and correspondingly from 'PEG_TX0' (+ and -) to 'PEG_TX15' (+ and -). The corresponding signals can be found on the Module connector rows C and D. The pins of the PEG Port are shared with other functionality like SDVO or DVO depends of the used chipset. SDVO and PEG are defined on COM Express specification as “may be used”. Please be sure, your functionality will be supported by your module vendor.

4.1.1 Signal Description

Table 4-1: PCI Express Signal Descriptions

Pin	Signal	I/O	Description
C52	PEG_RX0+	I	PEG Port 0. Receive Input differential pair.
C53	PEG_RX0-		
D52	PEG_TX0+	O	PEG Port 0. Transmit Output differential pair.
D53	PEG_TX0-		
C55	PEG_RX1+	I	PEG Port 1. Receive Input differential pair.
C56	PEG_RX1-		
D55	PEG_TX1+	O	PEG Port 1. Transmit Output differential pair.
D56	PEG_TX1-		
C58	PEG_RX2+	I	PEG Port 2. Receive Input differential pair.
C59	PEG_RX2-		
D58	PEG_TX2+	O	PEG Port 2. Transmit Output differential pair.
D59	PEG_TX2-		
C61	PEG_RX3+	I	PEG Port 3. Receive Input differential pair.
C62	PEG_RX3-		
D61	PEG_TX3+	O	PEG Port 3. Transmit Output differential pair.
D62	PEG_TX3-		
C65	PEG_RX4+	I	PEG Port 4. Receive Input differential pair.
C66	PEG_RX4-		
D65	PEG_TX4+	O	PEG Port 4. Transmit Output differential pair.
D66	PEG_TX4-		
C68	PEG_RX5+	I	PEG Port 5. Receive Input differential pair.
C69	PEG_RX5-		
D68	PEG_TX5+	O	PEG Port 5. Transmit Output differential pair.
D69	PEG_TX5-		
C71	PEG_RX6+	I	PEG Port 6. Receive Input differential pair.
C72	PEG_RX6-		
D71	PEG_TX6+	O	PEG Port 6. Transmit Output differential pair.
D72	PEG_TX6-		
C74	PEG_RX7+	I	PEG Port 7. Receive Input differential pair.
C75	PEG_RX7-		
D74	PEG_TX7+	O	PEG Port 7. Transmit Output differential pair.

D75	PEG_TX7-		
C78	PEG_RX8+	I	PEG Port 8,. Receive Input differential pair.
C79	PEG_RX8-		
D78	PEG_TX8+	O	PEG Port 8. Transmit Output differential pair.
D79	PEG_TX8-		
C81	PEG_RX9+	I	PEG Port 9,. Receive Input differential pair.
C82	PEG_RX9-		
D81	PEG_TX9+	O	PEG Port 9. Transmit Output differential pair.
D82	PEG_TX9-		
C85	PEG_RX10+	I	PEG Port 10.. Receive Input differential pair.
C86	PEG_RX10-		
D85	PEG_TX10+	O	PEG Port 10.Transmit Output differential pair.
D86	PEG_TX10-		
C88	PEG_RX11+	I	PEG Port 11. Receive Input differential pair.
C89	PEG_RX11-		
D88	PEG_TX11+	O	PEG Port 11. Transmit Output differential pair.
D89	PEG_TX11-		
C91	PEG_RX12+	I	PEG Port 12. Receive Input differential pair.
C92	PEG_RX12-		
D91	PEG_TX12+	O	PEG Port 12. Transmit Output differential pair.
D92	PEG_TX12-		
C94	PEG_RX13+	I	PEG Port 13,. Receive Input differential pair.
C95	PEG_RX13-		
D94	PEG_TX13+	O	PEG Port 13. Transmit Output differential pair.
D95	PEG_TX13-		
C98	PEG_RX14+	I	PEG Port 14.. Receive Input differential pair.
C99	PEG_RX14-		
D98	PEG_TX14+	O	PEG Port 14. Transmit Output differential pair.
D99	PEG_TX14-		
C101	PEG_RX15+	I	PEG Port 15. Receive Input differential pair.
C102	PEG_RX15-		
D101	PEG_TX15+	O	PEG Port 15. Transmit Output differential pair.
D102	PEG_TX15-		
A88 A98	PCIE_CLK_REF + PCIE_CLK_REF-	O	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes
D73	SDVO_I2C_CLK	O 2.5V CMOS	I2C based control signal (clock) for SDVO device.
C73	SDVO_I2C_DATA	I/O 2.5V OD CMOS	I2C based control signal (data) for SDVO device
D54	PEG_LANE_RV#	I 3.3V CMOS	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.
D97	PEG_ENABLE#	I 3.3V CMOS	PEG enable function. Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface. ***PS: IEI Bios auto detect the SDVO or PCIEX16, please reserve for future use***

4.1.2 PEG Connector

Figure 4-1 illustrates the pinout definition for the standard PCI Express x16 connectors.

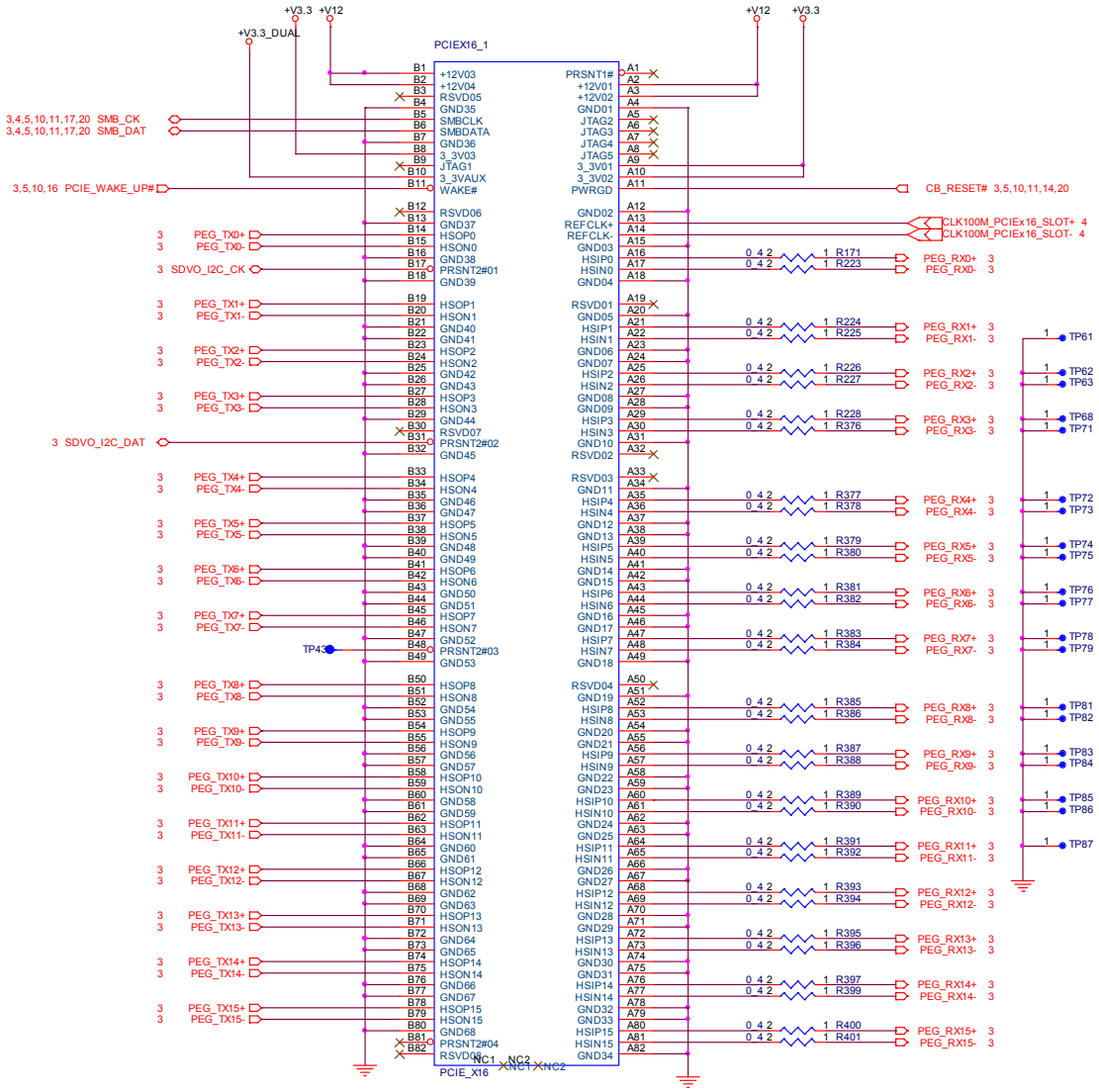


Figure 4-1: PCI Express x16 Slot Example

4.1.3 SDVO

The Serial Digital Video Out (SDVO) display ports are multiplexed over a subset of the External Graphics Interface using PCI Express. Users can choose a manufacturer approved by Intel® to convert the SDVO port to TV, LVDS, DVI or CRT connection. IEI also provides cables and SDVO card for customer to use. Due to the fact that SDVO is an Intel® defined interface, the number of supported SDVO devices is limited to devices that are supported by the Intel® Graphics Video BIOS and Graphics Driver software.

The COM Express Module graphics controller configures the PEG lines for SDVO operation if it detects that COM Express signals SDVO_I2C_CLK and SDVO_I2C_DATA are pulled high to 2.5V, and if the PEG_ENABLE# line is left floating. IEI BIOS auto detects the SDVO or PCIEX16, please reserve for future use.

Table 4-2: PEG & S DVO Pin Assignment

Pin	Signal	SDVO	Description
C52 C53	PEG_RX0+ PEG_RX0-	SDVO_TVCLKIN+ SDVO_TVCLKIN-	SDVO TVOUT Synchronization Clock differential pair.
C55 C56	PEG_RX1+ PEG_RX1-	SDVOB_INT+ SDVOB_INT-	SDVOB Input Interrupt differential pair.
C58 C59	PEG_RX2+ PEG_RX2-	SDVO_FLDSTALL+ SDVO_FLDSTALL-	SDVO Field Stall differential pair.
C68 C69	PEG_RX5+ PEG_RX5-	SDVOB_INT+ SDVOB_INT-	SDVOC Input Interrupt differential pair.
D52 D53	PEG_TX0+ PEG_TX0-	SDVOB_RED+ SDVOB_RED-	SDVO Channel B Red differential pair.
D55 D56	PEG_TX1+ PEG_TX1-	SDVOB_GREEN+ SDVOB_GREEN-	SDVO Channel B Green differential pair.
D58 D59	PEG_TX2+ PEG_TX2-	SDVOB_BLUE+ SDVOB_BLUE-	SDVO Channel B Blue differential pair.
D61 D62	PEG_TX3+ PEG_TX3-	SDVOB_CLK+ SDVOB_CLK-	SDVO Channel B Clock differential pair.
D65 D66	PEG_TX4+ PEG_TX4-	SDVOC_RED+ SDVOC_RED-	SDVO Channel C Red differential pair.
D68 D69	PEG_TX5+ PEG_TX5-	SDVOC_GREEN+ SDVOC_GREEN-	SDVO Channel C Green differential pair.
D71 D72	PEG_TX6+ PEG_TX6-	SDVOC_BLUE+ SDVOC_BLUE-	SDVO Channel C Blue differential pair.
D74 D75	PEG_TX7+ PEG_TX7-	SDVOC_CLK+ SDVOC_CLK-	SDVO Channel C Clock differential pair.

Table 4-3: Intel® SDVO Support Device List

Device	Vander	Application	Link

CH7021A	Chrontel	SDTV / HDTV Transmitter	http://www.chrontel.com
CH7308A	Chrontel	LVDS Transmitter	http://www.chrontel.com
CH7307C	Chrontel	DVI Transmitter	http://www.chrontel.com
CH7312	Chrontel	DVI Transmitter	http://www.chrontel.com
CX25905	Conexant	DVI-D / TV / CRT Transmitter	http://www.conexant.com
SiL1362/1364	Silicon Image	DVI Transmitter	http://www.siliconimage.com
SiL 1390	Silicon Image	HDMI Transmitter	http://www.siliconimage.com

4.1.4 PEG_ENABLE#

PEG_ENABLE# is defined on the COM Express connector as a method to configure the COM Express PCIe lanes 16 through 32 on the C-D connector as a PCI Express Graphics port, for use with an external graphics device. The usual effect of pulling PEG_ENABLE# low is to disable the on-Module graphics engine. For some Modules, it is possible to configure the Module such that the internal graphics engine remains active, even when the external PEG interface is being used for a Carrier Board graphics device. This is Module dependent. Check with your vendor. ICE Modules implement the auto-detect function. So, please reserve this pin for future use.

4.1.5 PCI Express Test Points and Probing

IEI follows the suggestion provided by Intel® to preserve 0-Ω on the baseboard. Additional test structures were not included in the simulation sweeps that this guideline is based on. The inclusion of test points and probing structures has the ability to impact the loss and jitter budgets of a PCI Express interconnect. This is not to say that they cannot be tolerated. In general, test points and probe structures should not introduce stubs on the differential pairs or cause significant deviation from the recommendations given throughout this chapter. Existing vias, pads or pins should be used wherever possible to accommodate such structures. Careful consideration must be taken whenever additional probing structures are used.

The PCI Express based specification requires the data eyes to be measured into a 50-Ω resistor terminated to ground. To facilitate the measurement, an additional test structure may be required on a test board. This test structure should not be included in a production board because it will affect the overall signal quality and resulting margins. The three-pad test structure consists of the footprints of two resistors, perpendicular to each other forming a “L” shape. The resistor package/footprint should

be as small as possible, preferably 0402. To enable the test mode, a 50 Ω ±1% resistor stuffing option is needed to break the path. This will force the transmitter port to enter the compliance mode and begin transmitting the compliance packet. Otherwise, use a 0-Ω resistor to continue the trace route to the Rx port. This will allow normal operation of the device.

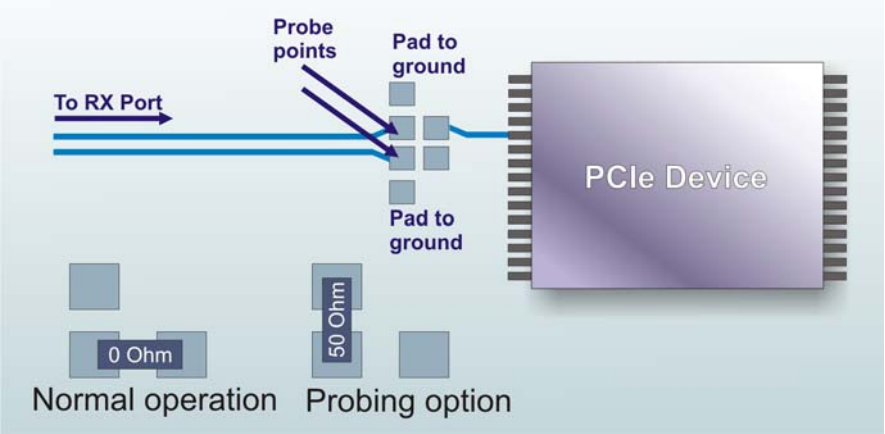


Figure 4-2: Intel Recommend Test Structure for PCI Express Data Eye Measurement

4.1.6 PCI Express Routing Guideline

4.1.6.1 Impedance Consideration

The PCI Express impedance considerations are listed in Table 4-4.

Table 4-4: PCI Express Impedance Consideration

Parameters	Routing
Transfer Rate / PCIe Lane	2.5 Gbits/sec
Maximum signal line length (coupled traces)	TX and RX path: 21.0 inches
Maximum signal length allowance on the COM Express module "	TX and RX path: 5.15 inches
Signal length allowance on the COM Express carrier board "	TX and RX path: 15.85 inches @ 0.28dB/GHz/inch to PCIe device 9.00 inches @ 0.28dB/GHz/inch to PCIe slot
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and	Min. 50mils

high-speed periodic signals	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plain	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the COM Express module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express" carrier board. Capacitor type: X7R

4.1.6.2 AC Coupling Capacitors

TX AC coupling capacitor is already embedded in the ICE modules. Users only need to add the RX AC coupling capacitor on the baseboard. The PCI Express specification requires that each lane of a PCI Express link be AC coupled between the driver and receiver. The specification allows for the AC coupling capacitors to be located either on or off the die. However, it is anticipated that in most cases the AC coupling will be separated from the die and in the form of discrete capacitors on the motherboard itself. While the 0603 size capacitors are acceptable, size 0402 capacitors are strongly encouraged. — The smaller package size reduces the series inductance. — The smaller package size reduces the overall board area needed to place the capacitors.

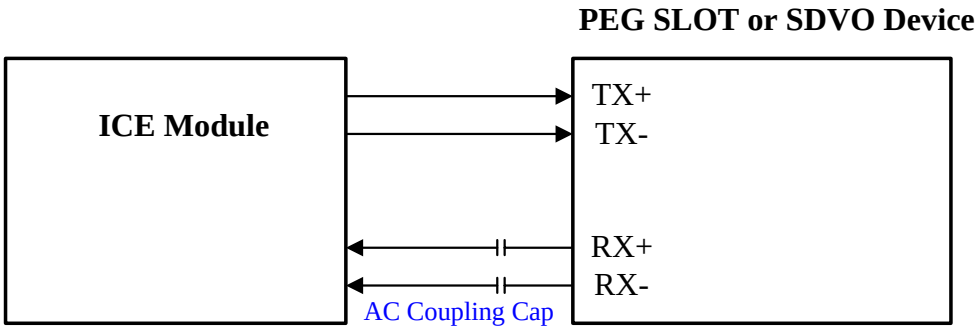


Figure 4-3: PEG Lane Connection Topology Example

4.1.6.3 Routing Notices

- Each signal and its complement in a differential pair should be length matched whenever possible on a segment-by-segment basis at the point of discontinuity. Examples of segments might include breakout areas, routes to connect vias, routes to connect an AC coupling capacitor, routes to connect a connector, and so forth.
- When trace length matching occurs, it should be made as close as possible to the point where the length variation occurs, as shown in Figure 4-4. For example, length matching in a chipset breakout area or connector pin field should occur within the first **125 mils** (3.175 mm) of the structure that causes the length mismatch.
- When serpentining is needed to match lengths, the trace spacing should not become greater than two times the original spacing. The length of the increased spacing should not be greater than three times the trace width. See Figure 4-4. In determining the overall length of a given signal in a differential pair, use pad or pin edge-to-edge distances rather than the total etch present, unless the amount of trace routing inside each pad is identical. The amount of etch within a given pad is electrically part of the pad itself. In other words, only the etch outside of the pad edge is relevant to the overall length of a differential pair.

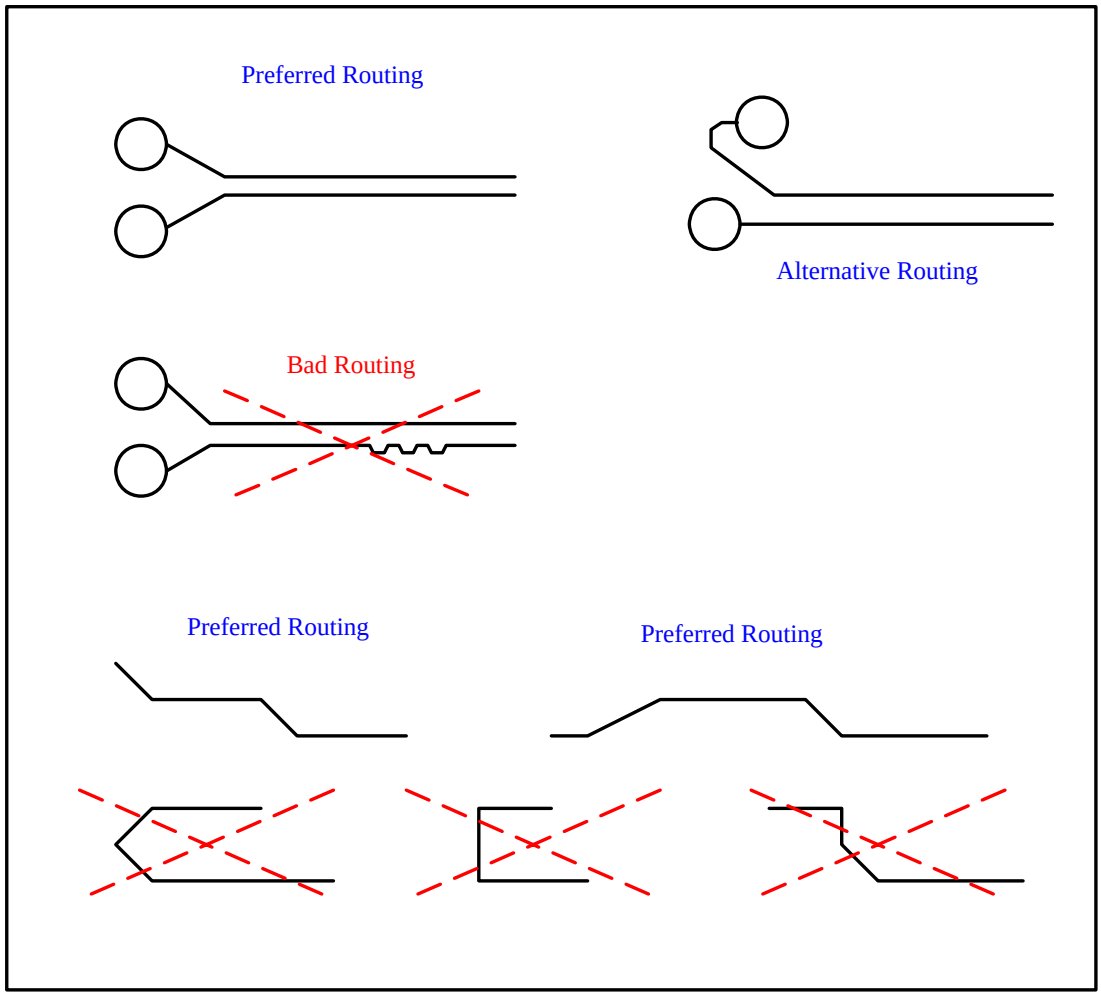


Figure 4-4: PEG Layout Trace Example

4.2 PCI Express

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. A PCI Express lane consists of dual simplex channels, each implemented as a low-voltage differentially driven transmit pair and receive pair. They are used for simultaneous transmission in each direction. The bandwidth of a PCI Express link can be scaled by adding signal pairs to form multiple lanes between two devices. The PCI Express specification defines x1, x4, x8, x16, and x32 link widths. Each single lane has a raw data transfer rate of 2.5Gbps @ 1.25GHz.

The PCI Express interface of the COM Express Type 2 module consists of up to 6 lanes, each with a receive and transmit differential signal pair designated from PCIE_RX0 (+ and -) to PCIE_RX5 (+ and -) and correspondingly from PCIE_TX0 (+ and -) to PCIE_TX5 (+ and -). According to the PCI Express specification, these six lanes can be configured as several PCI Express x1 links or to a combined x4 link plus two x1 links. These configuration possibilities are based on the COM Express module's chipset capabilities.

4.2.1 Signal Description

Table 4-5: PCI Express Signal Descriptions

Pin	Signal	I/O	Description
B68	PCIE_RX0+	I	PCIe Port 0. Receive Input differential pair.
B69	PCIE_RX0-		
A68	PCIE_TX0+	O	PCIe Port 0. Transmit Output differential pair.
A69	PCIE_TX0-		
B64	PCIE_RX1+	I	PCIe Port 1. Receive Input differential pair.
B65	PCIE_RX1-		
A64	PCIE_TX1+	O	PCIe Port 1. Transmit Output differential pair.
A65	PCIE_TX1-		
B61	PCIE_RX2+	I	PCIe Port 2,. Receive Input differential pair.
B62	PCIE_RX2-		
A61	PCIE_TX2+	O	PCIe Port 2. Transmit Output differential pair.
A62	PCIE_TX2-		
B58	PCIE_RX3+	I	PCIe Port 3.. Receive Input differential pair.
B59	PCIE_RX3-		
A58	PCIE_TX3+	O	PCIe Port 3. Transmit Output differential pair.
A59	PCIE_TX3-		
B55	PCIE_RX4+	I	PCIe Port 4. Receive Input differential pair.
B56	PCIE_RX4-		
A55	PCIE_TX4+	O	PCIe Port 4. Transmit Output differential pair.
A56	PCIE_TX4-		
B52	PCIE_RX5+	I	PCIe Port 5. Receive Input differential pair.
B53	PCIE_RX5-		
A52	PCIE_TX5+	O	PCIe Port 5. Transmit Output differential pair.
A53	PCIE_TX5-		
A88	PCIE_CLK_REF+	O	PCIe Reference Clock for all COM Express
A98	PCIE_CLK_REF-		PCIe lanes, and for PEG lanes
B66	WAKE0#	I PCIE	PCIe Wake Event: Sideband wake-up signal.
A49	EXCD0_CPPE#	I 3.3V CMOS	ExpressCard capable card request, slot 1.
B48	EXCD1_CPPE#	I 3.3V CMOS	ExpressCard capable card request, slot 2.
A48	EXCD0_PERST#	O 3.3V CMOS	ExpressCard reset, slot 1.
B47	EXCD1_PERST#	O 3.3V CMOS	ExpressCard reset, slot 2.

4.2.2 PCI Express Slot X1

Table 4-5 illustrates the pinout definition for the standard x1, x4, x8 and x16 PCI Express connectors. The dashed lines in the diagram depict where each different connector type ends. An example of an x1 PCIe slot is shown in Figure 4-5 below.

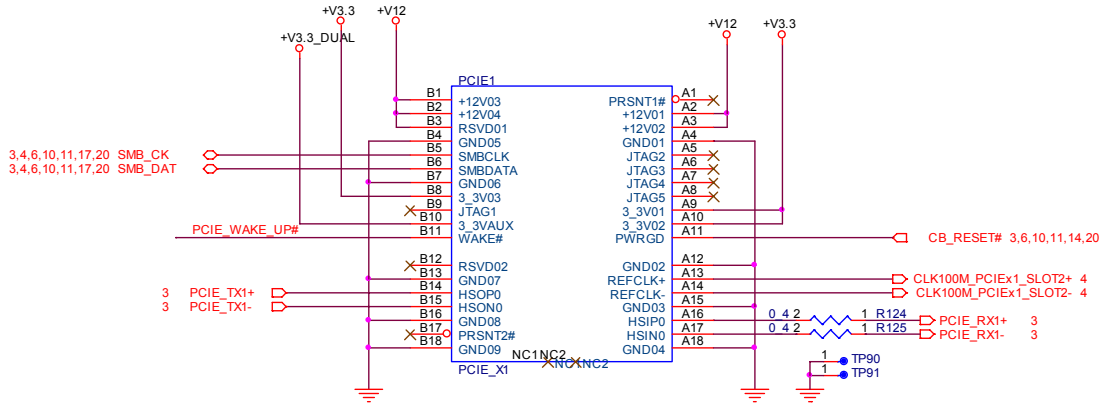


Figure 4-5: PCI Express x1 Slot Example

4.2.3 Express Card Connector

Hot-swappable Express Cards come in a small form factor and are designed primarily for mobile computing. The card's electrical interface is thru USB 2.0 or a single x1 PCIe link. Express Cards are the successor to Card Bus Cards (which are PCI-based). Card Bus cards, in turn, are the successors to PCMCIA cards. All three formats are defined by the PCMCIA Consortium.

ExpressCard is a small, modular add-in card designed to replace common PCMCIA and PC Cards. It takes advantage of the scalable, high-bandwidth serial PCI Express and USB 2.0 interfaces to provide much higher data rates. COM Express modules offer support for up to two ExpressCard slots. More information about the ExpressCard Standard can be found at http://www.expresscard.org.

In addition to the signals of a PCI Express x1 link and a USB 2.0 link, the ExpressCard interface requires the following control signals provided by the COM Express module. The corresponding signals can be found on the module connector rows A and B.

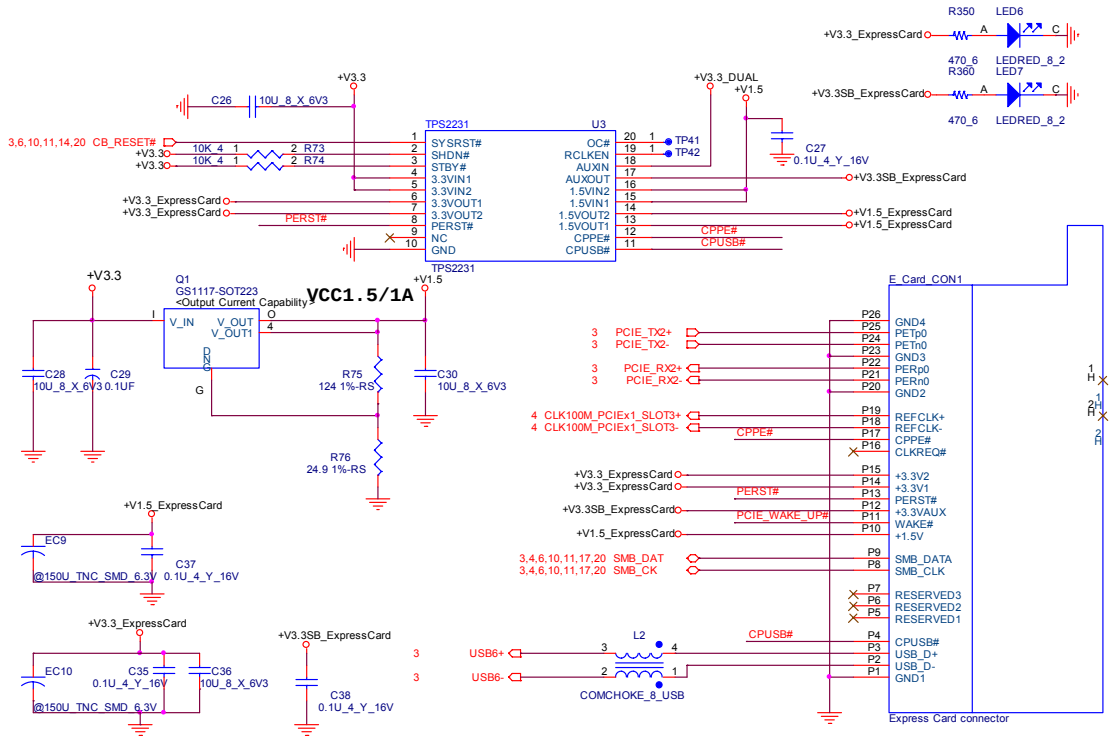


Figure 4-6: Express Card Slot Example

Table 4-6: Express Card Pin Definition

Pin	Signal	I/O	Description
1	GND	P	Ground
2	USB_D-	I/O USB	USB Serial Data Interface differential pair, negative signal
3	USB_D+	I/O USB	USB Serial Data Interface differential pair, positive signal
4	CPUSB#	I 3.3V	USB Interface presence detected
5	RSVD		Reserved
6	RSVD		Reserved
7	SMBCLK	I/O 3.3V	System Management Bus Clock
8	SMBDATA	I/O 3.3V	System Management Bus Data
9	+1.5V	P 1.5V	Secondary voltage source, 1.5V
10	+1.5V	P 1.5V	Secondary voltage source, 1.5V
11	WAKE#	I 3.3V	Request that the host interface return to full operation and respond to PCIe
12	+3.3VAUX	P 3.3V	Auxiliary voltage source, 3.3V
13	PERST#	I 3.3V	PCI Express Reset
14	+3.3V	P 3.3V	Primary voltage source, 3.3V
15	+3.3V	P 3.3V	Primary voltage source, 3.3V
16	CLKREQ#	I 3.3V	Request that REFCLK be enabled
17	CPPE#	I 3.3V	PCI Express interface presence detect
18	REFCLK-	I PCIe	PCI Express reference clock differential pair, negative signal
19	REFCLK+	I PCIe	PCI Express reference clock differential pair, positive signal
20	GND	P	Ground
21	PERn0	I/O PCIe	PCI Express Receiver differential pair negative signal
22	PERp0	I/O PCIe	PCI Express Receiver differential pair positive signal

23	GND	P	Ground
24	PETn0	I/O PCIe	PCI Express Transmitter differential pair negative signal
25	PETp0	I/O PCIe	PCI Express Transmitter differential pair positive signal
26	GND	P	Ground

The PCMCIA Consortium defines two form factors for Express Cards:

- Express Card/34 and Express Card/54 use a socket-style interconnect.
- There are two mechanical Form Factors with Express Card/34, which are useable in either socket. Each has the same electrical interface.
- Interface support for a PCIe x1 lane and USB 2.0 on the socket is required.
- Socket interface requirements for Carrier Boards include:
- PCIe x1 Lane and USB 2.0
- WAKE# and the SM Bus are optional at the socket and COM Express Module level.

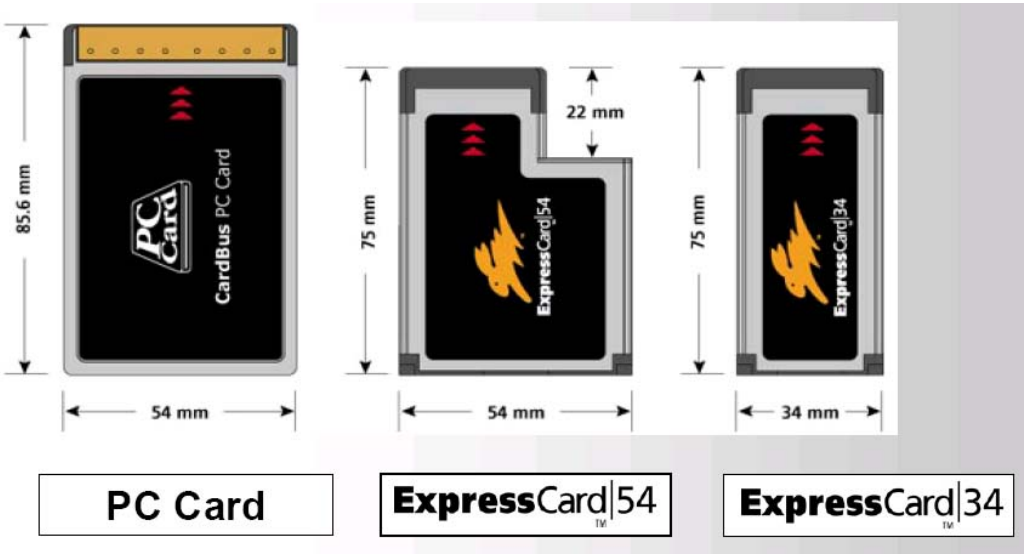


Figure 4-7: Express Card 54&34 Type (Refer to www.expresscard.org)

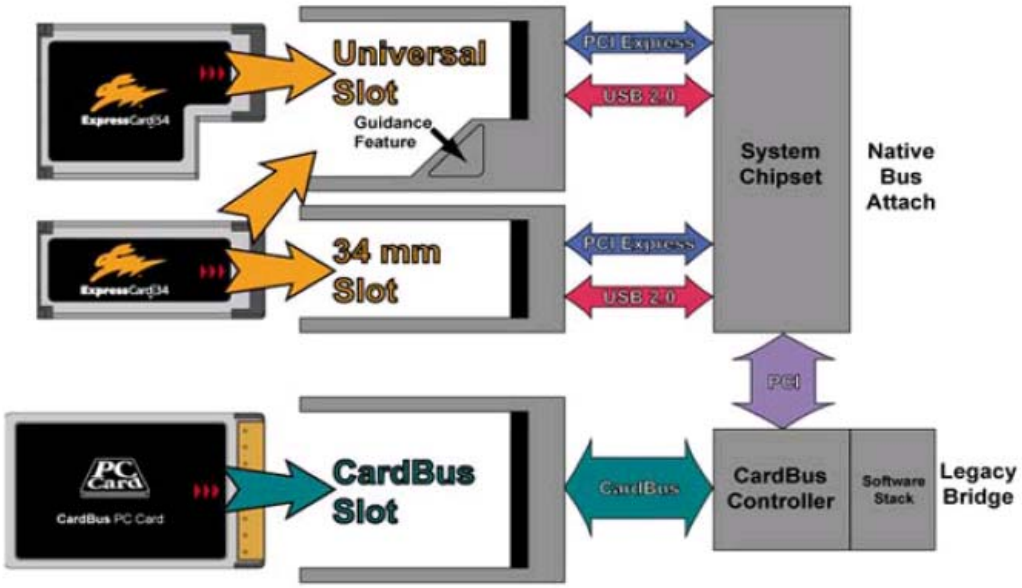


Figure 4-8: Express Card 54 & 34 Plug Way (Refer to www.expresscard.org)

4.2.4 PCIe Mini Card

The PCI Express Mini Card add-in card is a small size unique form factor optimized for mobile computing platforms equipped with communication applications such as Wireless LAN. A small footprint connector can be implemented on the carrier board providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradeable, standardized PCI Express Mini Card device to the carrier board without additional expenditure of a redesign. In addition to a PCI Express x1 link and a USB 2.0 link, the PCI Express Mini Card interface utilizes the following control and reset signals, which are provided by the COM Express module connector rows A and B.

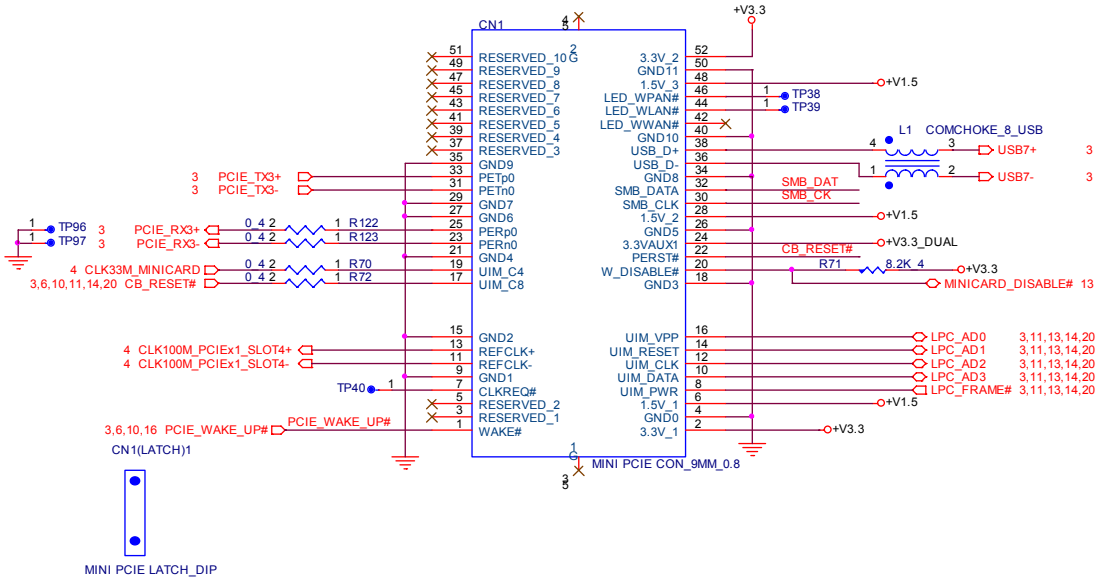


Figure 4-9: Express Card Slot Example

The following sections illustrate signal pin-outs for the system connector. Table 4-7 lists the pin-out for the system connector.

Table 4-7: Mini Card Pin-out

Pin #	Signal	Pin #	Signal
51	Reserved*	52	+3.3V
49	Reserved*	50	GND
47	Reserved*	48	+1.5V
45	Reserved*	46	LED_WPAN#
43	Reserved*	44	LED_WLAN#
41	Reserved*	42	LED_WWAN#
39	Reserved*	40	GND
37	Reserved*	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	Reserved	20	Reserved***
17	Reserved	18	GND
Mechanical Key			
15	GND	16	Reserved**
13	REFCLK+	14	Reserved**
11	REFCLK-	12	Reserved**
9	GND	10	Reserved**
7	CLKREQ#	8	Reserved**

5	Reserved****	6	1.5V
3	Reserved****	4	GND
1	WAKE#	2	3.3V

* Reserved for future second PCI Express Lane (if needed)

** Reserved for future Subscriber Identity Module (SIM) interface (if needed)

*** Reserved for future wireless disable signal (if needed)

**** Reserved for future wireless coexistence control interface (if needed)

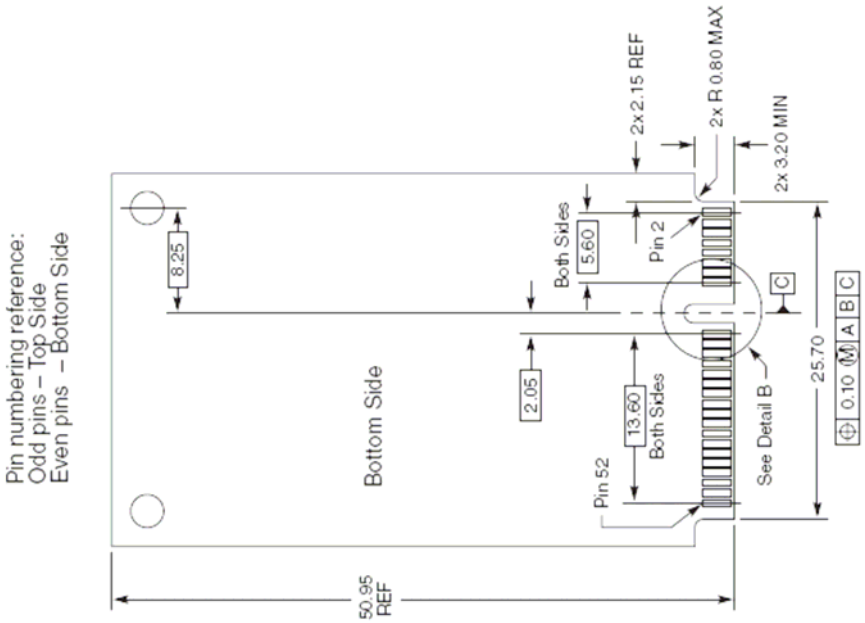


Figure 4-10: Mini Card Bottom Side Dimensions (Refer to www.pcisig.com)

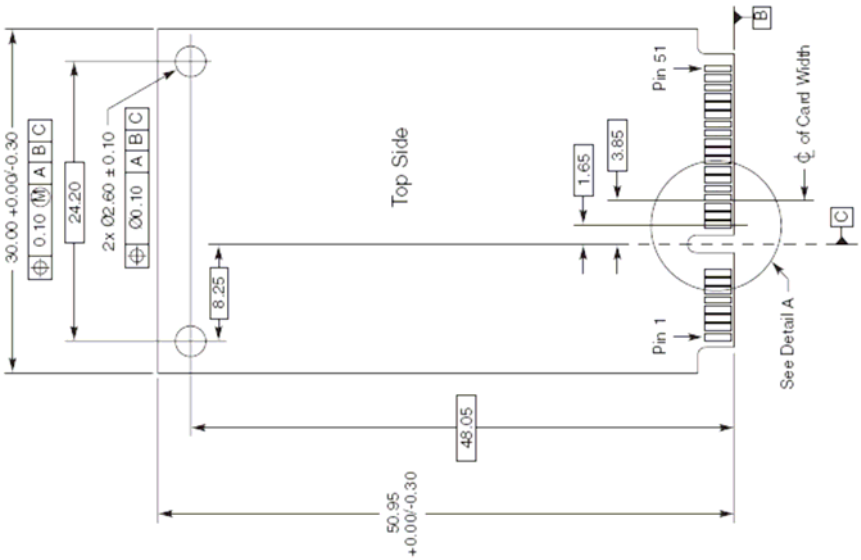


Figure 4-11: Mini Card Top Side Dimensions (Refer to www.pcisig.com)

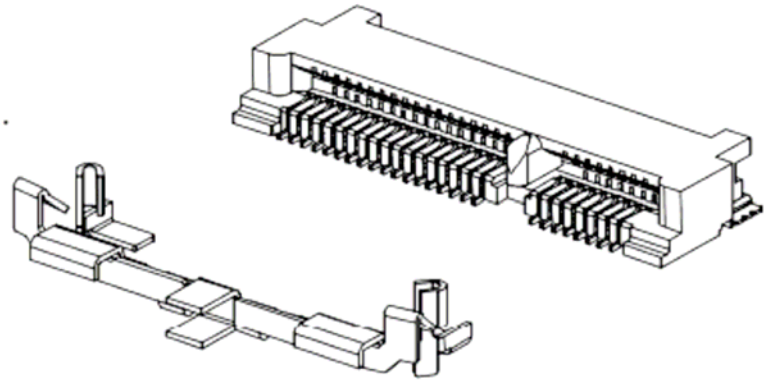


Figure 4-12: Mini Card Connector (Refer to www.pcisig.com)

4.2.5 PCI Express Clock Buffer

COM Express only provides a set of 100 MHz Clock for PCI Express Device. When there are more than one PCI Express modules used on the baseboard, the Clock Buffer must be used. Please refer to the schematic diagram (Figure 4-13) suggested by IEI.

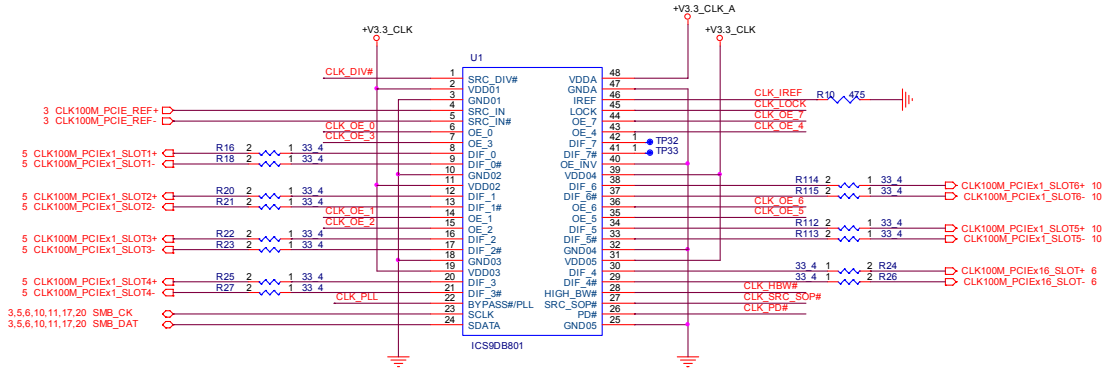


Figure 4-13: PCI Express Clock Buffer Example

4.2.5.1 PCI Express Routing Guideline

Please refer to **Section 4.1.6**

4.3 PCI

The COM Express provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification,* Revision 2.2. The implementation is optimized for high-performance data streaming when the COM Express is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification,* Revision 2.2.

4.3.1 Signal Description

Table 4-8 shows COM Express PCI bus signal, including pin number, signals, I/0, power plane, terminal resistors, damping resistors and descriptions.

Table 4-8: PCI Signal Description

Pin	Signal	I/O	Description
Note1	PCI_AD[0..31]	I/O 3.3V	PCI bus multiplexed address and data lines
Note1	PCI_C/BE[0..3]#	I/O 3.3V	PCI bus byte enable lines , active low
C36	PCI_DEVSEL#	I/O 3.3V	PCI bus Device Select, active low.
D36	PCI_FRAME#	I/O 3.3V	PCI bus Frame control line, active low.
C37	PCI_IRDY#	I/O 3.3V	PCI bus Initiator Ready control line, active low.
D35	PCI_TRDY#	I/O 3.3V	PCI bus Target Ready control line, active low.
D34	PCI_STOP#	I/O 3.3V	PCI bus STOP control line, active low.
D32	PCI_PAR	I/O 3.3V	PCI bus parity
C34	PCI_PERR#	I/O 3.3V	Parity Error: An external PCI device drives PERR# to low, when it receives data that has a parity error.
Note1	PCI_REQ[0..3]#	I 3.3V	PCI bus master request input line, active low.
Note1	PCI_GNT[0..3]#	O 3.3V	PCI bus master grant output lines, active low.
C23	PCI_RESET#	O 3.3V	PCI Reset output, active low.
C35	PCI_LOCK#	I/O 3.3V	PCI Lock control line, active low.
D33	PCI_SERR#	I/O 3.3V	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.
C15	PCI_PME#	I 3.3VSB	PCI Power Management Event: PCI peripherals drive PME# to low to wake up the system from low-power states S1 – S5.
D48	PCI_CLKRUN#	I/O 3.3V	Bidirectional pin used to support PCI clock run protocol for mobile systems.
Note1	PCI_IRQ[A..D]#	I 3.3V	PCI interrupt request lines.
D50	PCI_CLK	O 3.3V	PCI 33MHz clock output.
D49	PCI_M66EN	I 3.3V	Module input signal that indicates whether an carrier board PCI device is capable of 66MHz operation. It is pulled to ground by carrier board device or by slot card, if one of the devices are NOT capable of 66MHz operation.

Please refer to **Table 3-3: Module Type 2 Connector Pinout Rows (A and B)** or **Table 3-4: Module Type 2 Connector Pinout Rows (C and D)**.

4.3.2 PCI Connector

The PCI slot connection is shown in Figure 4-14.

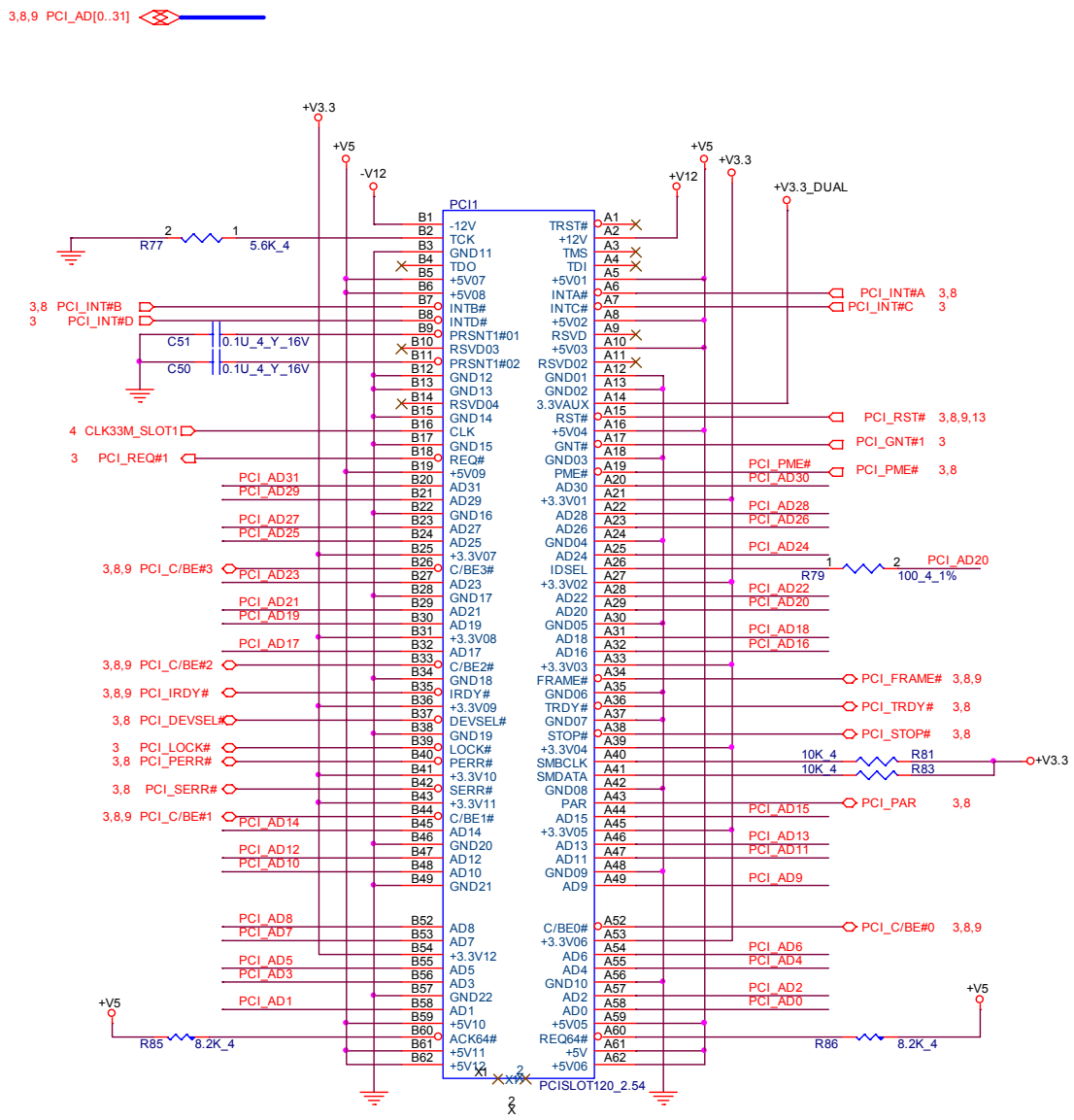


Figure 4-14: PCI Slot Connection Example

4.3.3 PCI IRQ Assignment

Most of this PCI devices only utilize the interrupt signal 'INTA#'. To distribute the interrupt source of the devices over the interrupt signals 'INTB#', 'INTC#' and 'INTD#', an interrupt cross routing has to be implemented on the COM Express carrier board design. Figure 5-14 and Table 5-16 illustrate the PCI bus interrupt routing for the PCI bus slots 1-4. The PCI REQ and GNT lines with the same index must be considered

as a pair. It is not permitted to combine REQ and GNT lines with a different index. A PCI REQ/GNT pair can only be used once for a single PCI bus-master device.

Table 4-9: PCI Slot Routing Table

	Slot1	Slot2	Slot3	Slot4
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#

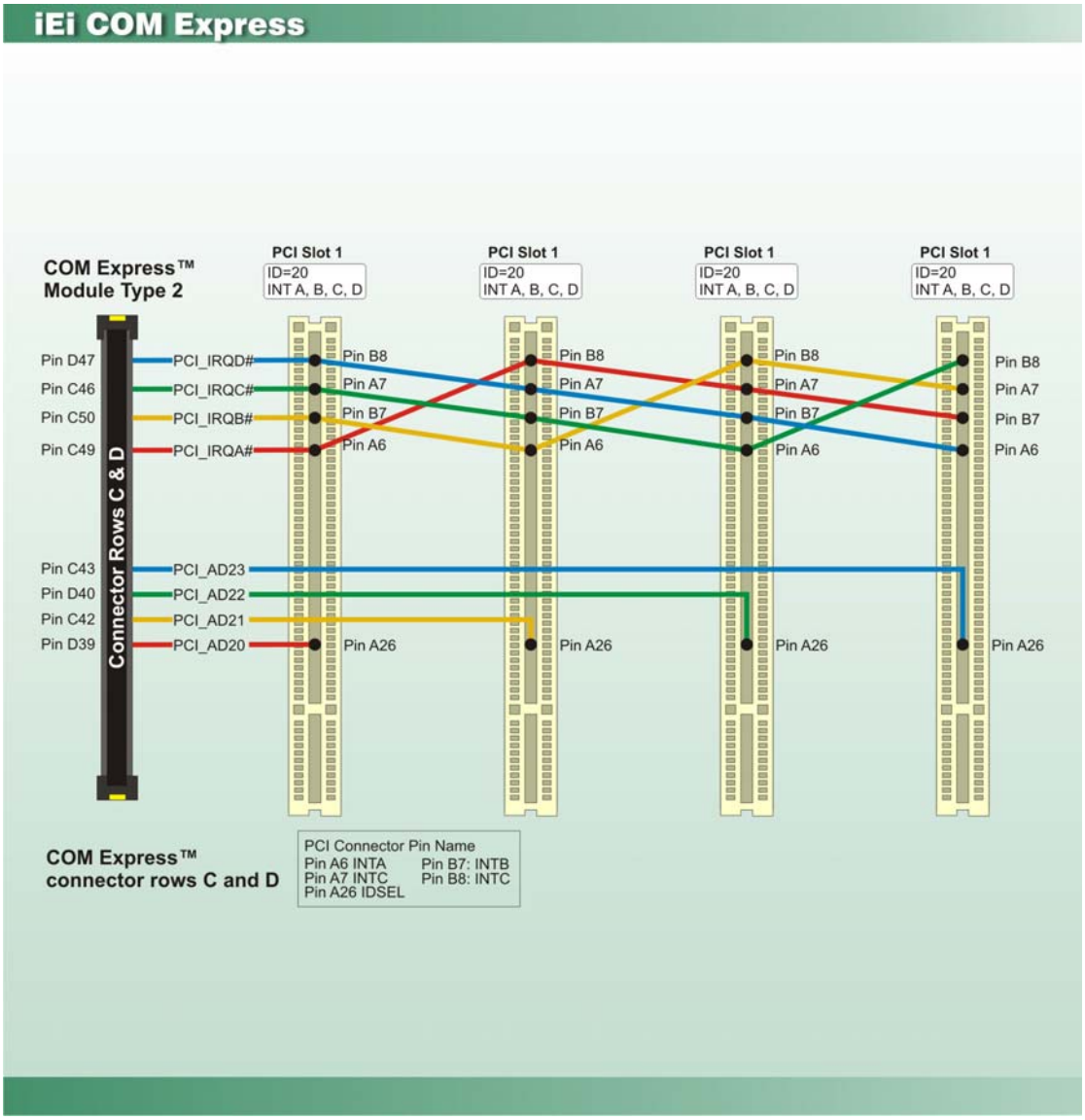


Figure 4-15: PCI Slot Routing Example

4.3.4 PCI Clock Buffer

The COM Express Specification only supports a single PCI clock signal called *'PCI_CLK'* to be used on the carrier board. If there are multiple devices or slots implemented on the carrier board, a zero delay clock buffer is required to expand the number of PCI clocks so that each device or each bus slot will be provided with a separate clock signal.

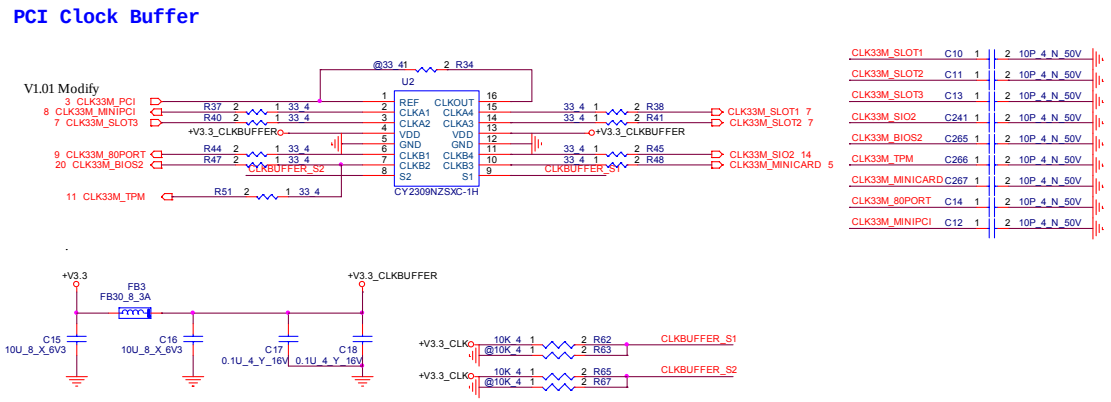


Figure 4-16: PCI Clock Buffer Example

4.3.5 PCI Routing Guideline

Particular attention must be paid to the PCI clock routing. The PCI Local Bus specification requires a maximum propagation delay for the clock signals of 10ns within a propagation skew of 2ns @ 33MHz between the several clock signals. The COM Express Specification allows 1.6ns ± 0.1ns @ 33MHz propagation delay for the PCI clock signal beginning from the module pin to the destination pin of the PCI device. The propagation delay is dependent on the trace geometries, PCB stack-up and the PCB dielectric constant. Calculating using a typical propagation delay value of 180ps/inch for an internal layer clock trace of the carrier board, a maximum trace length of 8.88 inches is allowed.

The clock trace from the COM Express module to a PCI bus slot should be 2.5 inches shorter because PCI cards are specified to have 2.5 inches of clock trace length on the card itself. PCI clock signals should be routed as a single ended trace with a trace impedance of 55Ω. To reduce EMI, a single ground referenced internal layer is recommended. The clock traces should be separated as far as possible from other

signal traces. Refer to section 8.1 'PCI Trace Routing Guidelines' and the 'PCI Local Bus Specification Revision 2.3' to get more information about this subject.

Table 4-10: PCI Impedance Consideration

Parameters	Routing
Transfer Rate @ 33MHz	132 MB/sec
Signal length used on COM Express module (including the COM Express" carrier board connector) "	3.0 inches
Maximum data and control signal length allowance for the COM Express carrier board. "	10 inches
Maximum clock signal length allowance for the COM Express carrier board. "	8.88 inches
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between signals (inter-signal) (S)	7mils (microstrip routing) (*)
Length matching between single ended signals	Max. 200mils
Length matching between clock signals	Max. 200mils
Spacing from edge of plane	Min. 40mils
Reference plain	GND referenced preferred
Via Usage	Try to minimize number of vias
Decoupling capacitors for each PCI slot.	Min. 1x22µF, 2x 100nF @ VCC 5V Min. 2x22µF, 4x 100nF @ VCC 3.3V Min. 1x22µF, 2x 100nF @ +12V (if used) Min. 1x22µF, 2x 100nF @ -12V (if used)

4.4 SATA (Serial ATA Interface)

Serial ATA is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. SATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard SATA provides a maximum effective data transfer rate of 150 MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300 MB/s per port is possible. Serial ATA is completely software transparent to the IDE interface while providing a lower pin count and higher performance.

4.4.1 Signal Description

All COM Express modules provide up to 4 Serial ATA channels, each with a receive and transmit differential signal pair designated from *'SATA0_RX'* (+ and -) to *'SATA3_RX'* (+ and -) and correspondingly from *'SATA0_TX'* (+ and -) to *'SATA3_TX'* (+ and -). The appropriate signals can be found on the COM Express module connector row A and row B.

Table 4-11: Serial ATA Signal Descriptions

Pin	Signal	I/O	Description
A19	SATA0_RX+	I SATA	Serial ATA channel 0 Receive input differential pair.
A20	SATA0_RX-		
A16	SATA0_TX+	O SATA	Serial ATA channel 0 Transmit output differential pair.
A17	SATA0_TX-		
B19	SATA1_RX+	I SATA	Serial ATA channel 1 Receive input differential pair.
B20	SATA1_RX-		
B16	SATA1_TX+	O SATA	Serial ATA channel 1 Transmit output differential pair.
B17	SATA1_TX-		
A25	SATA2_RX+	I SATA	Serial ATA channel 2 Receive input differential pair.
A26	SATA2_RX-		
A22	SATA2_TX+	O SATA	Serial ATA channel 2 Transmit output differential pair.
A23	SATA2_TX-		
B25	SATA3_RX+	I SATA	Serial ATA channel 3 Receive input differential pair.
B26	SATA3_RX-		
B22	SATA3_TX+	O SATA	Serial ATA channel 3 Transmit output differential pair.
B23	SATA3_TX-		
A28	SATA_ACT#	O 3.3V CMOS OC	Serial ATA activity LED. Open collector output pin driven during SATA command activity.

4.4.2 SATA Connector

Each ICE module provides four SATA port at maximum. Users can use these SATA ports for their applications. Figure 4-17 shows the standard SATA port connection.

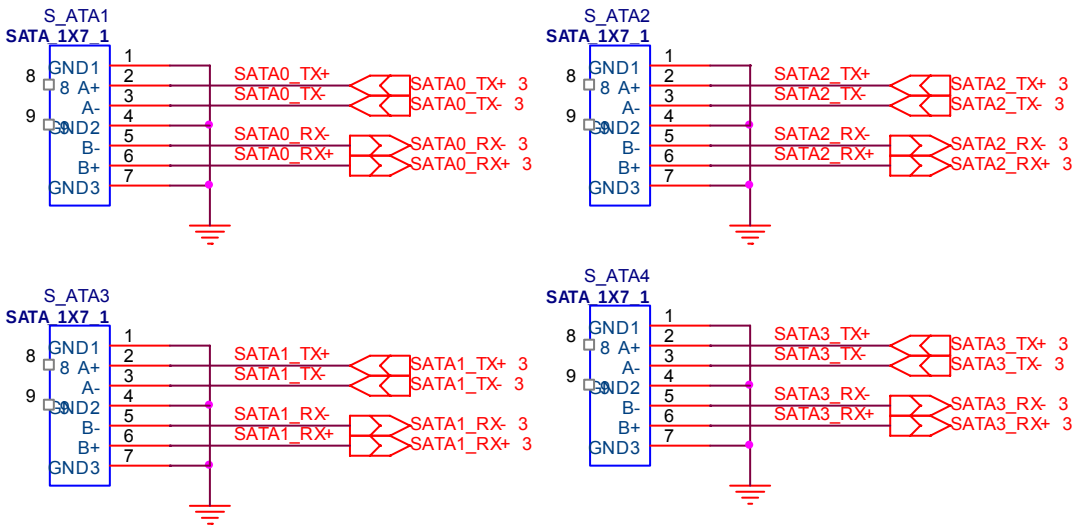


Figure 4-17: SATA 7-pin Connector Example

4.4.3 SATA LED#

The SATA LED can be used with the HDD LED. Please refer to the following schematic diagram.

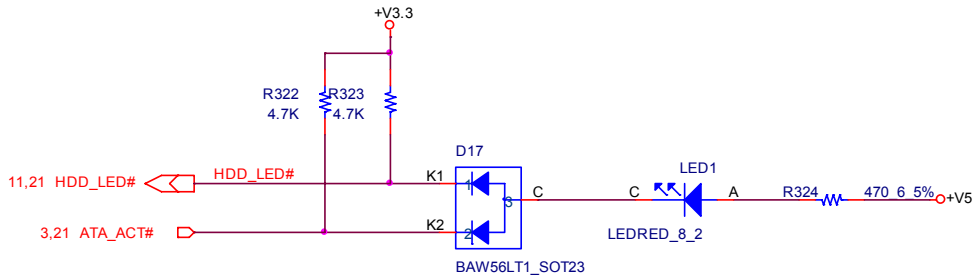


Figure 4-18: SATA LED Connection Example

4.4.4 SATA Routing Guideline

Table 4-12: SATA Impedance Consideration

Parameters	Routing
Transfer Rate	3.0 Gbits/sec
Maximum signal line length (coupled traces)	7.0 inches on PCB (COM Express module and carrier board. The length of the SATA cable is specified between 0 and 40 inches) "
Signal length used on COM Express module (including the COM Express" carrier board connector) "	2.5 inches
Signal length available for the COM Express carrier board "	4.5 inches
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency. Do not serpentine to meet trace length guidelines for the RX and TX path.
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express module. "

4.5 Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices such as game controllers, communication devices and input devices on a single bus. A COM Express Module must provide a minimum of four USB ports and can support up to eight USB ports.

USB stands for Universal Serial Bus, an industry-standard specification for attaching peripherals to a computer. It delivers high performance, the ability to plug in and unplug devices while the computer is running, great expandability, and a wide variety of solutions.

The USB physical topology consists of connecting the downstream hub port to the upstream port of another hub or to a device. The USB can operate at three speeds. High-speed (480 Mb/s) and full-speed (12 Mb/s) require the use of a shielded cable with two power conductors and twisted pair signal conductors. Low-speed (1.5 Mb/s) recommends, but does not require the use of a cable with twisted pair signal conductors. The connectors are designed to be hot plugged. The USB Icon on the plugs provides tactile feedback making it easy to obtain proper orientation.

4.5.1 Signal Description

Table 4-13 shows COM Express USB signals, including pin number, signals, I/0, power plane, terminal resistors, damping resistors and descriptions.

Table 4-13: USB Signal Description

Pin	Signal	I/O	Description
A46 A45	USB0+ USB0-	I/O	USB Differential Data Port 0.
B46 B45	USB1+ USB1-	I/O	USB Differential Data Port 1.
A43 A42	USB2+ USB2-	I/O	USB Differential Data Port 2.
B43 B42	USB3+ USB3-	I/O	USB Differential Data Port 3.
A40 A39	USB4+ USB4-	I/O	USB Differential Data Port 4.
B40 B39	USB5+ USB5-	I/O	USB Differential Data Port 5.
A37 A36	USB6+ USB6-	I/O	USB Differential Data Port 6.

B37 B36	USB7+ USB7-	I/O	USB Differential Data Port 7.
B44	USB_0_1_OC#	I 3.3V CMOS	USB over-current sense, USB ports 0 and 1. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
A44	USB_2_3_OC#	I 3.3V CMOS	USB over-current sense, USB ports 2 and3. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
B38	USB_4_5_OC#	I 3.3V CMOS	USB over-current sense, USB ports 4 and 5. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.

4.5.2 USB Keyed Connector Protocol

To minimize end user termination problems, USB uses a “keyed connector” protocol. The physical difference in the Series “A” and “B” connectors insures proper end user connectivity. The “A” connector is the principle means of connecting USB devices directly to a host or to the downstream port of a hub. All USB devices must have the standard Series “A” connector specified in this chapter. The “B” connector allows device vendors to provide a standard detachable cable. This facilitates end user cable replacement.

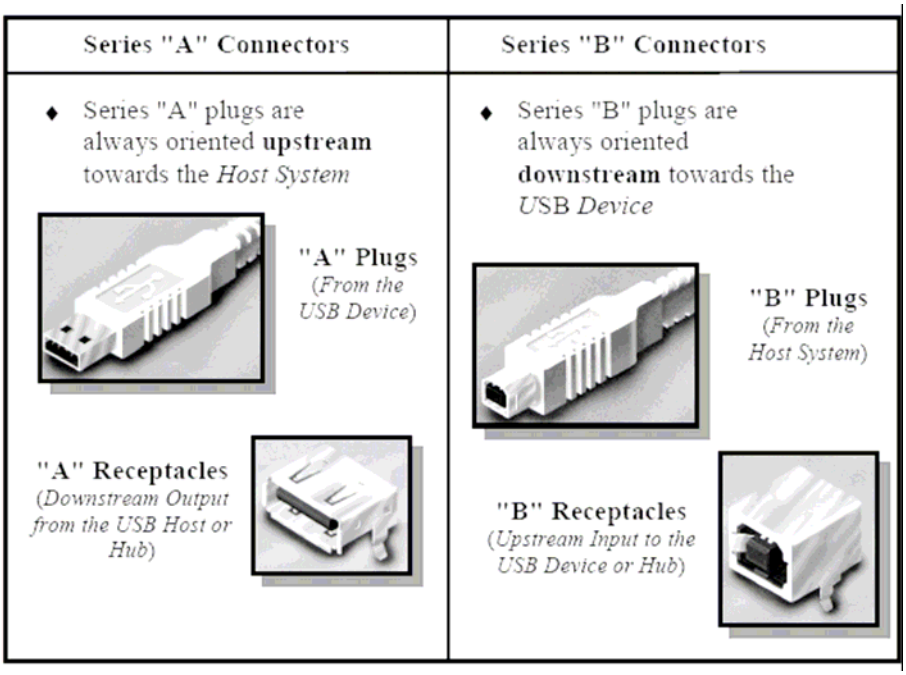


Figure 4-19: Keyed Connector Protocol (Refer to USB2.0 Spec.)

The following list explains how the plugs and receptacles can be mated:

- Series “A” receptacle mates with a Series “A” plug. Electrically, Series “A” receptacles function as outputs from host systems and/or hubs.
- Series “A” plug mates with a Series “A” receptacle. The Series “A” plug always is oriented towards the host system.
- Series “B” receptacle mates with a Series “B” plug (male). Electrically, Series “B” receptacles function as inputs to hubs or devices.
- Series “B” plug mates with a Series “B” receptacle. The Series “B” plug is always oriented towards the USB hub or device.

USB connector usually used connector of Type A.

Figure 4-20: USB Connector

Table 4-14: USB Connector Signal Description

Pin	Signal	I/O	Description
1	VCC	P	+5V Power supply
2	DATA-	I/O	USB Data, negative differential signal.
3	DATA+	I/O	USB Data, positive differential signal.
4	GND	P	Ground

4.5.3 ESD/EMI

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the carrier board design.

To protect the USB host interface of the module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the carrier board design.

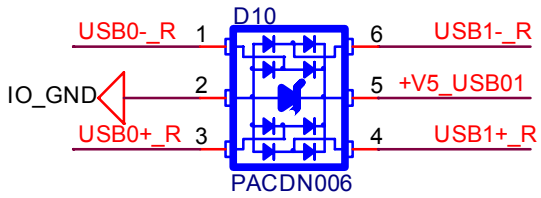


Figure 4-21: RailClamp SRV05-4 Low Capacitance TVS Diode Array for ESD

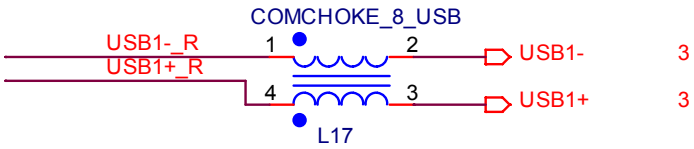


Figure 4-22: 90 ohm Common Mode Choke at 100MHz for EMI

4.5.4 Over Current Protection

Over-current protection for USB ports can be implemented by using power distribution switches on the carrier board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered. Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express modules USB over-current sense signals. IEI uses MIC2026 for carrier board.

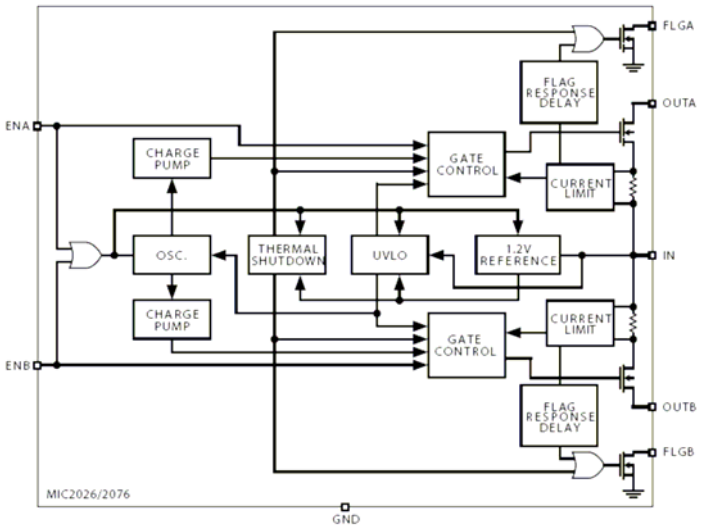


Figure 4-23: MIC2026 Block Diagram(Please refer the datasheet from MICREL)

4.5.5 Reference Schematics

The following notes apply to Figure 4-24 below.

LAN_USB and CN26 incorporate two USB Type A receptacles, LAN_USB in addition includes an RJ-45 (LANKom LJ -G40BU1-10-F).

The reference design uses an over-current detection and protection device. The Micrel MIC2026 is dual channel power distribution switch. Power to the USB Port is filtered using a ferrite (30 Ω @100MHz, 600mA) to minimize emissions. The ferrite should be placed adjacent to the USB Port connector pins. The OC# signal is asserted until the over-current or over-temperature condition is resolved.

USB0+/- through USB4+/- from the COM Express Module are routed through a common mode choke to reduce radiated cable emissions. The part shown is a AXIS POWER BCCUB-T4P-2012-900T; this device has a common mode impedance of approximately 90 Ω at 100MHz. The common-mode choke should be placed close to the USB connector.

ESD protection diodes D10、D11 and D12 provide over-voltage protection caused by ESD and electrical fast transients. Low capacitance diodes and transient voltage suppression diodes should be placed near the USB connector. The example design uses a RailClamp SRV05-4 low capacitance TVS Diode Array from Semtech (http://www.semtech.com).

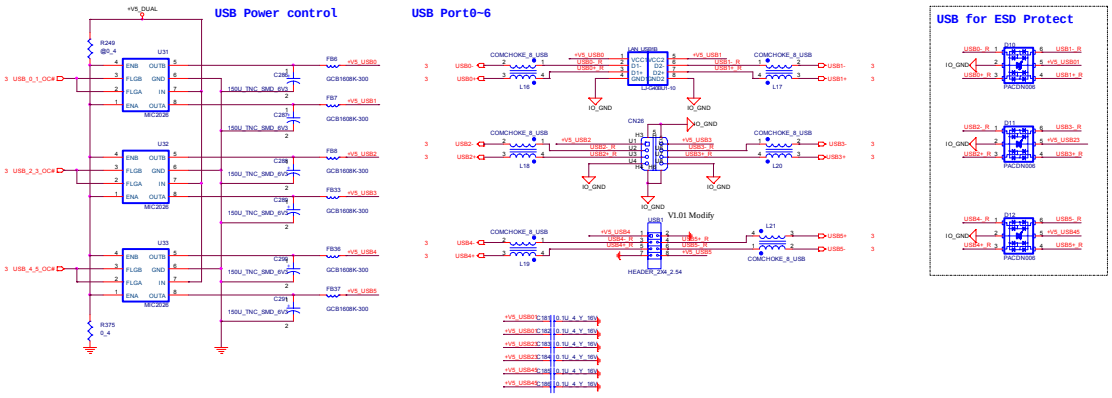


Figure 4-24: USB Reference Design

4.5.6 USB Routing Guideline

4.5.6.1 Impedance

Parameters	Routing
Transfer rate / Port	480 Mbit/s
Maximum signal line length (coupled traces)	Max. 17.0 inches
Signal length used on COM Express module (including the COM Express" connector) "	3.0 inches
Signal length allowance for the COM Express carrier board "	14.0 inches
Differential Impedance	90 Ohms +/-15%
Single-ended Impedance	45 Ohms +/-10%
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Reference plain	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias

4.5.6.2 General Routing and Placement

- USB 2.0 signals should be ***ground referenced***.
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Avoid stubs on high-speed USB signals, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes, with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split.

- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

4.6 LVDS

4.6.1 Signal Description

Table 4-15 shows COM Express LVDS and LCD signals, including pin number, signals, I/O and descriptions.

Table 4-15: LVDS Signals Description

Pin	Signal	I/O	Description
A71	LVDS_A0+	O	LVDS channel A differential signal pair 0
A72	LVDS_A0-		
A73	LVDS_A1+	O	LVDS channel A differential signal pair 1
A74	LVDS_A1-		
A75	LVDS_A2+	O	LVDS channel A differential signal pair 2
A76	LVDS_A2-		
A78	LVDS_A3+	O	LVDS channel A differential signal pair 3
A79	LVDS_A3-		
A81	LVDS_A_CK+	O	LVDS channel A differential clock pair
A82	LVDS_A_CK-		
B71	LVDS_B0+	O	LVDS channel B differential signal pair 0
B72	LVDS_B0-		
B73	LVDS_B1+	O	LVDS channel B differential signal pair 1
B74	LVDS_B1-		
B75	LVDS_B2+	O	LVDS channel B differential signal pair 2
B76	LVDS_B2-		
B77	LVDS_B3+	O	LVDS channel B differential signal pair 3
B78	LVDS_B3-		
B81	LVDS_B_CK+	O	LVDS channel B differential clock pair
B82	LVDS_B_CK-		
A77	LVDS_VDD_EN	O 3.3V CMOS	LVDS flat panel power enable.
B79	LVDS_BKLT_EN	O 3.3V CMOS	LVDS flat panel backlight enable high active signal
B83	LVDS_BKLT_CTRL	O 3.3V CMOS	LVDS flat panel backlight brightness control
A83	LVDS_I2C_CK	O 3.3V CMOS	DDC I2C clock signal used for flat panel detection and control.
A84	LVDS_I2C_DAT	I/O 3.3V OD CMOS	DDC I2C data signal used for flat panel detection and control.

4.6.2 LVDS Cable Consideration

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver. Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Ribbon cables are a cost effective and easy solution. Even though they are not well suited for high-speed differential signaling they do work fine for very short runs. Most cables will work effectively for cable distances of <0.5m.

4.6.3 Backlight and LCD Power Timing Control

Figure 4-25 is a reference design of backlight and LCD power timing control. In Figure 4-26, VIN is LCD power and lamp is LCD backlight power. Figure 4-27 shows the LCD power sequence, and design must conform to it's power sequence.

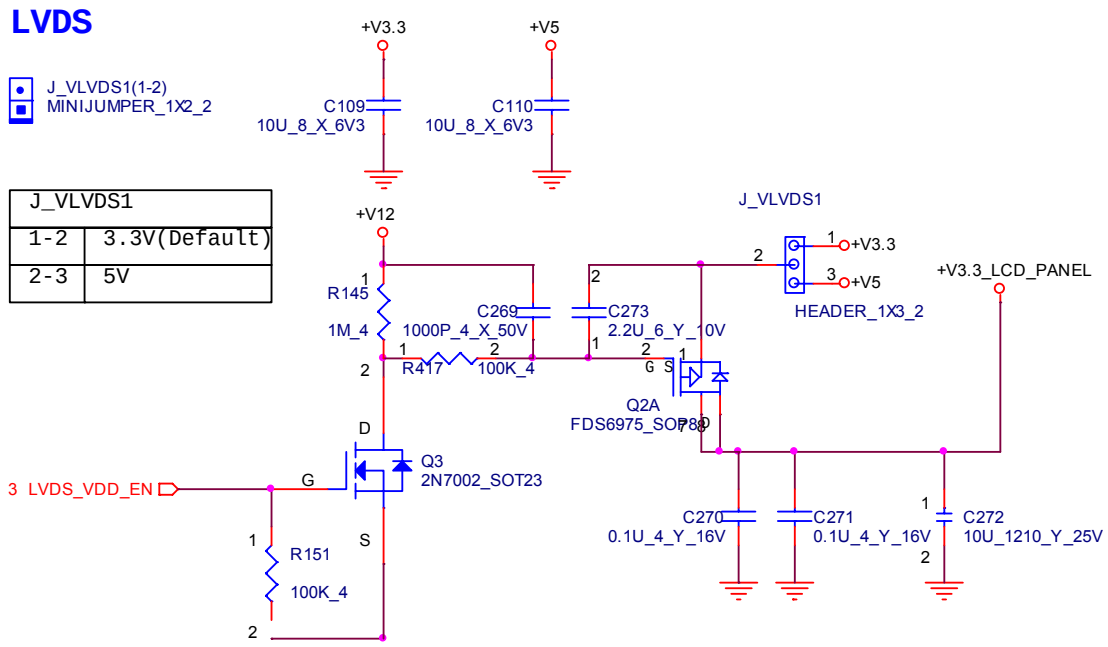


Figure 4-25: LVDS Power Control

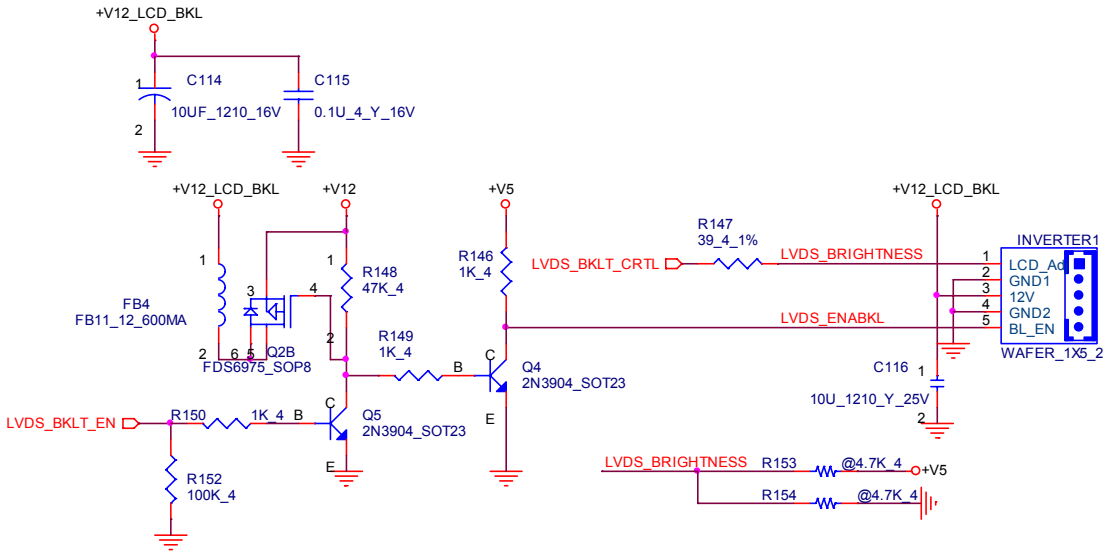
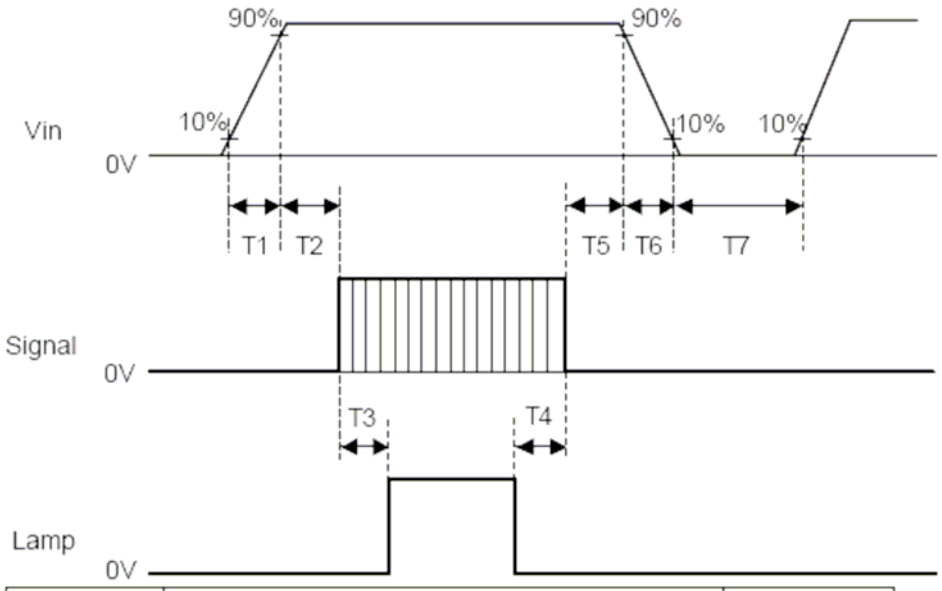


Figure 4-26: Backlight Control Circuit



Symbol	Values			Unit
	Min	Typ	Max	
T1	0.5	-	10	[ms]
T2	0.5	25	50	[ms]
T3	200	-	-	[ms]
T4	200	-	-	[ms]
T5	0.5	16	50	[ms]
T6	0.5	-	10	[ms]
T7	1000	-	-	[ms]

Figure 4-27: LCD Power Sequence Example(Refer to AUO G150XG01)

4.6.4 LVDS Routing Guideline

4.6.4.1 Impedance

Table 4-16: LVDS Impedance Consideration

Parameters	Routing
Transfer Rate	5.38 Gbits/sec
Maximum signal line length to the LVDS connector (coupled traces)	8.75 inches
Signal length used on COM Express module (including the COM Express" carrier board connector) "	2.0 inches
Signal length to the LVDS connector available for the COM Express carrier board "	6.75 inches
Differential Impedance	100 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Spacing between pair to pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	+/- 20mils
Length matching between clock and data pairs (inter-pair)	+/- 20mils
Length matching between data pairs (inter-pair)	+/- 40mils
Spacing from edge of plane	+/- 40mils

4.6.4.2 Implement

Many carrier board designs do not need the full range of LVDS performance offered by COM Express modules. It depends on the flat panel configuration of the COM Express module, as well as the carrier board design, as to how many LVDS signal pairs are supported. While the dual channel 24-bit LVDS configuration needs all 10 LVDS signal pairs, a single channel 18-bit LVDS configuration only requires 4 LVDS signal pairs. In this case all unused LVDS signal pairs should be left open on the carrier board. If the LVDS display interface of the COM Express module is not implemented, all signals associated with this interface should be left open.

4.7 Audio Codec Interface(AC'97/HDA)

All COM Express module types support Audio Codec '97 (AC'97) and/or High Definition Audio (HDA) Digital Interface (AC-link) specifically designed for implementing audio and modem I/O functionality. The corresponding signals can be found on the COM Express module connector rows A and B.

4.7.1 Signal Description

Table 4-17 shows COM Express audio bus signal, including pin number, signals, I/0, power plane, terminal resistors, damping resistors and descriptions.

Table 4-17: Audio Signals Description

Pin	Signal	I/O	Description
A30	AC_RST#	O 3.3VSB CMOS	CODEC Reset.
A29	AC_SYNC	O 3.3V CMOS	48kHz fixed-rate, sample-synchronization signal to the CODEC(s).
A32	AC_BITCLK	O 3.3V CMOS	12.228 MHz Serial Bit Clock for CODEC.
A33	AC_SDOUT	O 3.3V CMOS	Serial TDM data output to the CODEC.
B30 B29 B28	AC_SDIN0 AC_SDIN1 AC_SDIN2	I 3.3VSB CMOS	Serial TDM data inputs from up to 3 CODECs

4.8 Reference Circuit

Please refer to the schematic diagram of the baseboard. IEI baseboard is embedded with the Realtek ALC888 audio controller. For the detailed specifications of the Realtek ALC888, please go to http://www.realtek.com/ .

4.8.1 Audio Routing Guideline

4.8.1.1 Analog Power Delivery

Clean analog power delivery to the audio codec and other audio components utilizing the 5-V analog supply is critical. Excessive system noise on this supply will degrade the entire audio sub-system. Except the GND signal, users can use independent LDO to generate clean audio analog power.

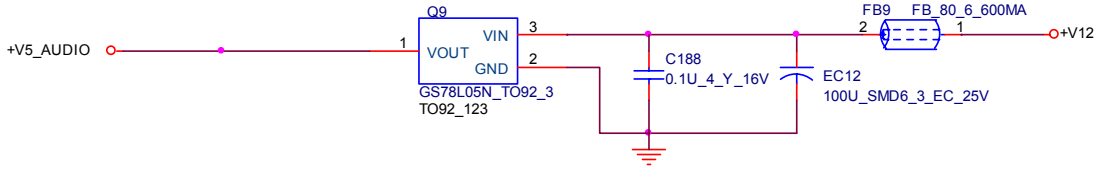


Figure 4-28: Audio Analog Power Example

4.8.1.2 Digital and Analog Signals Isolation

Analog audio signals and other digital signals should be routed as far as possible from each other. All audio circuits require careful PCB layout and grounding to avoid picking up digital noise on audio-signal lines.

4.8.1.3 EMI Consideration

Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

4.9 IDE

Type 2 and 4 COM Express modules provide a single channel IDE interface supporting two standard IDE hard drives or ATAPI devices with a maximum transfer rate of ATA100 (Ultra-DMA-100 with 100MB/s transfer rate). The corresponding signals can be found on the module connector rows C and D.

4.9.1 Signal Description

Table 4-18 shows COM Express PCI IDE signals, including pin number, signals, I/0, power plane, terminal resistors, damping resistors and descriptions.

Table 4-18: IDE signals description

Pin	Signal	I/O	Description
	IDE_D[0..15]	I/O 3.3V	Bidirectional data to / from IDE device.
D13 D14 D15	IDE_A[0:2]	O 3.3V	Address lines to IDE device.
D9	IDE_IOW#	O 3.3V	I/O write line to IDE device.
C14	IDE_IOR#	O 3.3V	I/O read line to IDE device.
D8	IDE_REQ	I 3.3V	IDE device DMA request. It is asserted by the IDE device to request a data transfer.

D10	IDE_ACK#	O 3.3V	IDE device DMA acknowledge.
D16	IDE_CS1#	O 3.3V	IDE device chip select for 1F0h to 1FFh range.
D17	IDE_CS3#	O 3.3V	IDE device chip select for 3F0h to 3FFh range.
C13	IDE_IORDY	I 3.3V	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.
D18	IDE_RESET#	O 3.3V	Reset output to IDE device, active low.
D12	IDE_IRQ	I 3.3V	Interrupt request from IDE device.
D77	IDE_CBLID#	I 3.3V	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 modes.

4.9.2 IDE Connector

To interface standard 3.5-inch parallel ATA drives, a standard 2.54mm, two row, 40-pin connector in combination with a ribbon conductor cable is used. For slower drive speeds up to ATA33, a normal 40-pin, 1.0mm-pitch conductor cable is sufficient. Higher transfer rates like ATA66 and ATA100 require 80-pin conductor cables, where the extra 40 conductors are tied to ground to isolate the adjacent signals for better signal integrity. The signal *'IDE_CBLID#'* of the COM Express carrier board indicates which conductor cable is used. It ties to ground if a 80-pin conductor cable is connected. This allows the module's BIOS to determine the maximum transfer rate that can be driven and set up the proper drive parameters for the IDE controller.

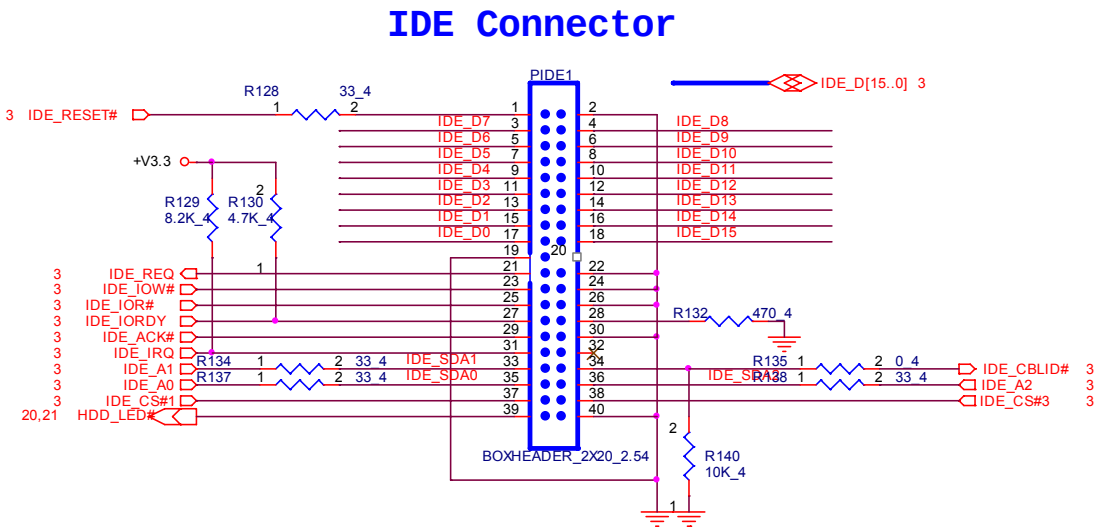


Figure 4-29: IDE Reference Design

Notes: When using a 44- pin IDE connector, pins 41 and 42 must be connected to VCC and pins 43 and 44 must be connected to ground. All other pins are equivalent to a 40-pin IDE connector. Additionally, decoupling capacitors should be connected to the VCC pins.

4.9.3 CF Connector

CompactFlash (CF) cards with DMA capability require that the two signals 'IDE_REQ' and 'IDE_ACK#' are routed to the CF card socket on the COM Express carrier board. If this is not done then some DMA capable CF cards may not work because they are not designed for non DMA mode. For more information about this subject refer to the datasheet of the CF card or contact your CF card manufacturer. If two CF cards are used in master/slave mode on the same IDE channel, the signal 'CSEL#' of the CF card socket that drives the slave CF card must be tied to ground. In master mode the 'CSEL#' signal must be left open. Figure 4-31 shows a circuitry implementing a CF card socket that is DMA capable.

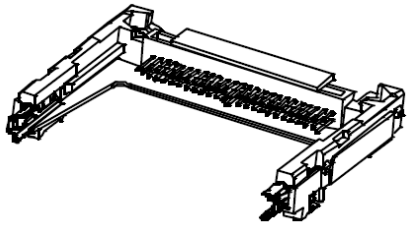


Figure 4-30: CF Connector

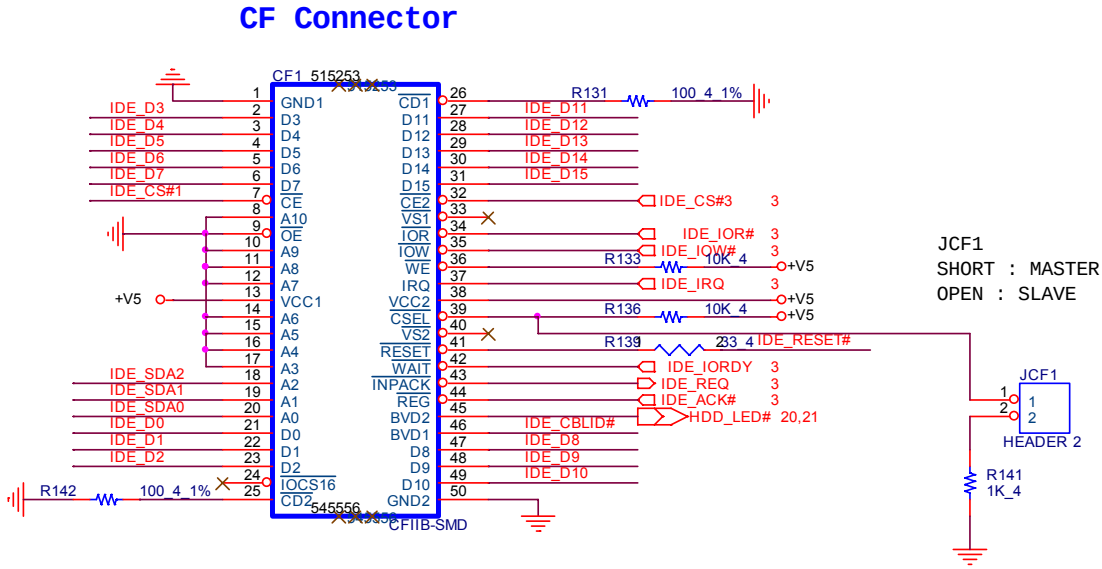


Figure 4-31: CompactFlash® Reference Design

4.10 TV-Out

The TV-Out display interface of the COM Express Module consists of three individual digital-to-analog converter (DAC) channels, which can be used in different combinations to support S-Video (Y/C), Composite Video or Component Video (YPbPr). The corresponding signals can be found on the COM Express module connector row B.

4.10.1 Signal Description

Table 4-19: TV-Out Signal Descriptions

Pin	Signal	I/O	Description
B97	TV_DAC_A	O Analog	TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used
B98	TV_DAC_B	O Analog	TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal. S-Video: Luminance analog signal.
B99	TV_DAC_C	O Analog	TVDAC Channel C Output supports the following: Composite video: not used Component: Chrominance (Pr) analog signal. S-Video: Chrominance analog signal.

4.10.2 TV-Out Routing Guideline

4.10.2.1 Signal Termination

Each of the TV-DAC channels should have a 150 Ω ±1% pull-down termination resistor connected from the TV-DAC output of the COM Express module to the carrier board ground. This termination resistor should be placed as close as possible to the TV-Out connector on the carrier board. A second 150 Ω ±1% termination resistor exists on the COM Express module itself.

4.10.2.2 Video Filter

There should be a PI-filter placed on each TV-DAC channel output to reduce high-frequency noise and EMI. The PI-filter consists of two 10pF capacitors with a 120Ω @ 30Mhz ferrite bead between them. It is recommended to place the PI-filters and the termination resistors as close as possible to the TV-Out connector on the carrier board. The PI-filters should be separated from each other by at least 50mils or more in order to minimize crosstalk between the TV-DAC channels.

4.10.2.3 ESD Protection

ESD clamp diodes are required for each TV-DAC channel. These low capacitance clamp diodes should be placed as near as possible to the TV-Out connector on the COM Express carrier board between +5V supply voltage and ground.

4.10.2.4 Reference Schematic

At least 30 mils of spacing should be used for the routing between each TV-DAC channel to prevent crosstalk between the TV-DAC signals. The maximum trace length distance of the TV-DAC signals between the COM Express connector and the 150Ω ±1% termination resistor should be within 12 inches. This distance should be routed with a 50 Ω trace impedance.

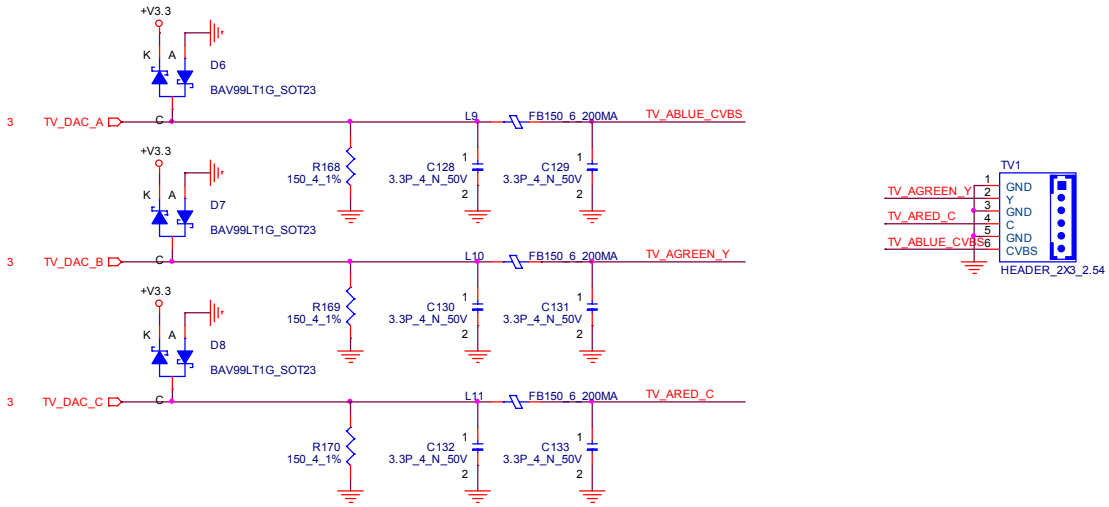


Figure 4-32: TV Out Schematic Reference

4.11 LAN (Local Area Network)

All COM Express modules provide at least one LAN port with the minimum capability of 10/100BaseTx Ethernet and optional 10/100/1000BaseT Gigabit Ethernet compliant to the IEEE 802.3ab specification.

The LAN interface of the COM Express module consists of 4 pairs of low voltage differential pair signals designated from *'GBE0_MDI0'* (+ and -) to *'GBE0_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect a 10/100/1000BaseT RJ-45 connector with integrated or external isolation magnetics to the carrier board. The corresponding LAN differential pair and control signals can be found on the modules connector rows A and B.

4.11.1 Signal Description

Table 4-20 shows COM Express Ethernet signals, including pin number, signals, I/O, power plane, terminal resistors, damping resistors and descriptions.

Table 4-20: Ethernet signals description

Pin	Signal	I/O	Description
A13 A12	GBE0_MDI0+ GBE0_MDI0-	I/O	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes.
A10 A9	GBE0_MDI1+ GBE0_MDI1-	I/O	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes.
A7 A6	GBE0_MDI2+ GBE0_MDI2-	I/O	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes.
A3 A2	GBE0_MDI3+ GBE0_MDI3-	I/O	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.
A14	GBE0_CTREF	REF	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V.
A8	GBE0_LINK#	O 3.3V CMOS OD	Ethernet controller 0 link indicator, active low.
A4	GBE0_LINK100#	O 3.3V CMOS OD	Ethernet controller 0 100Mbit/sec link indicator, active low.
A5	GBE0_LINK1000#	O 3.3V CMOS OD	Ethernet controller 0 1000Mbit/sec link indicator, active low.
B2	GBE0_ACT#	O 3.3V CMOS OD	Ethernet controller 0 activity indicator, active low.

4.11.2 Giga LAN Connector

IEI uses the RJ-45 connector including the transformer.

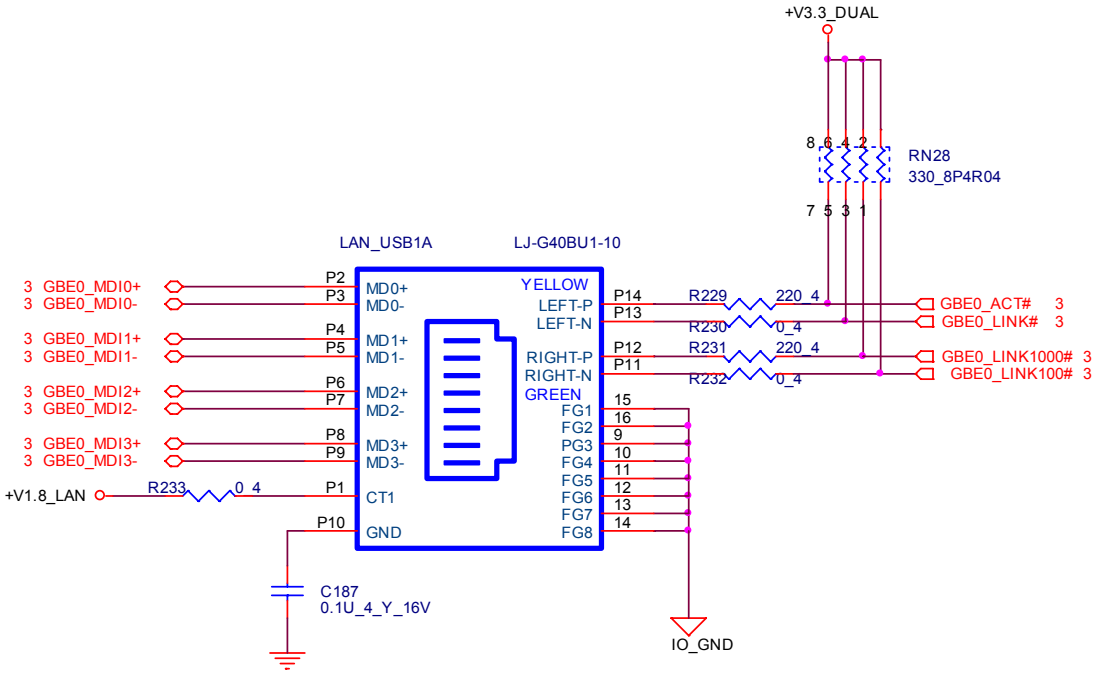


Figure 4-33: Giga Lan Connection Exampel (including Transformer)

4.11.3 LAN Link Activity and Speed LED

The COM Express module has four 3.3V open drain outputs to directly drive activity, speed indication and link status LEDs. The 3.3V standby voltage should be used as LED supply voltage so that the link activity can be viewed during system standby state. Since LEDs are likely to be integrated into a RJ-45 connector with integrated magnetics module, the LED traces need to be routed away from potential sources of EMI noise.

4.11.4 LAN Routing Guideline

4.11.4.1 Impedance

Table 4-21: LAN Impedance Consideration

Parameters	Routing
Transfer Rate	1.0 Gbits/sec
Maximum signal line length (coupled traces)	8.0 inches specified by COM Express "
Signal length used on COM Express module (including the carrier board connector) "	3.0 inches specified by COM Express "
Signal length allowance for the COM Express carrier board "	5.0 inches to the magnetics module
Maximum signal length between isolation magnetics module and RJ-45 connector on the carrier board	1.0 inch
Differential Impedance	95 Ohms +/-20%
Single-ended Impedance	55 Ohms +/-15%
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics module and RJ-45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

4.11.4.2 LAN Ground Plane Separation

Isolated separation between the analog ground plane and digital ground plane is recommended. If this is not implemented properly then bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise. The plane area underneath the magnetic module should be left void. The void area is to keep transformer induced noise away from the power and system ground planes. The isolated ground, also called chassis ground, connects directly to the fully shielded RJ-45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection a 3kV high voltage capability capacitor is recommended to connect to this chassis ground for ESD protection. Additionally, a ferrite bead can be placed parallel to the capacitor.

4.12 LPC (Low Pin Count Interface)

The Low Pin Count Interface was defined by the Intel Corporation to facilitate the industries transition toward legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface Firmware Hubs, Trusted Platform Module (TPM) devices and Embedded Controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. For more information about LPC bus refer to the 'Intel Low Pin Count Interface Specification Revision 1.1'.

4.12.1 Signal Description

Since COM Express is designed to be a legacy free standard for embedded modules, it does not support legacy functionality such as PS/2 keyboard/mouse, serial and parallel ports. Instead it provides an LPC interface that can be used to add peripheral devices to the carrier board design. The reduced pin count of the LPC interface makes it easy to implement such devices. All corresponding signals can be found on the modules connector rows A and B.

Table 4-22: LPC Interface Signal Descriptions

Pin	Signal	I/O	Description
A50	LPC_SERIRQ	I/O 3.3V CMOS	LPC serialized IRQ.
B3	LPC_FRAME#	O 3.3V CMOS	LPC frame indicates start of a new cycle or termination of a broken cycle.
B4	LPC_AD0	I/O 3.3V CMOS	LPC multiplexed command, address and data.
B5	LPC_AD1		
B6	LPC_AD2		
B7	LPC_AD3		
B8	LPC_DRQ0#	I 3.3V CMOS	LPC encoded DMA/Bus master request.
B9	LPC_DRQ1#		
B10	LPC_CLK	O 3.3V CMOS	LPC clock output 33MHz.

4.12.2 Clock and Reset Buffer

The ICE module already integrates reset buffer, therefore, the baseboard does not need reset buffer. For clock buffer, please refer to or integrate with the PCI clock buffer.

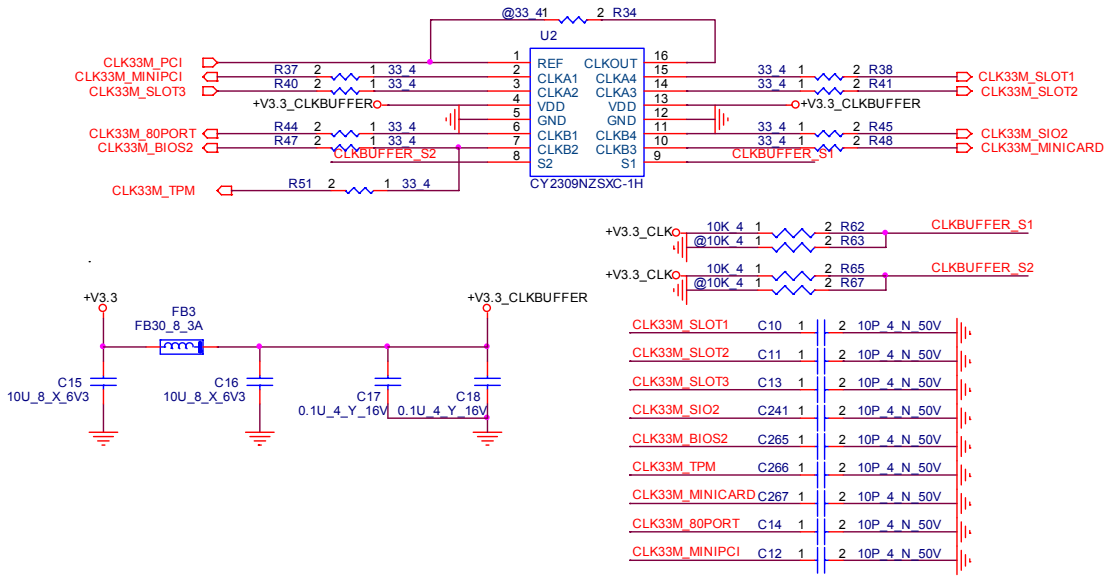


Figure 4-34: Clock Buffer

4.12.3 LPC SuperIO for Legacy IO Support

Some COM Express modules utilize BIOS that contains built-in support for an external Winbond W83627HG LPC Super I/O controller that can be implemented on the carrier board (http://www.winbond-usa.com). The base address for this Super I/O should be 0x2E to be sure that the legacy devices can be initialized by the BIOS. The implementation of this device on the COM Express carrier board will provide legacy interfaces such as PS/2 keyboard/mouse, floppy port, two serial ports (COM1 and COM2) and one parallel port (LPT1). The other functions of this Super I/O controller are not supported.

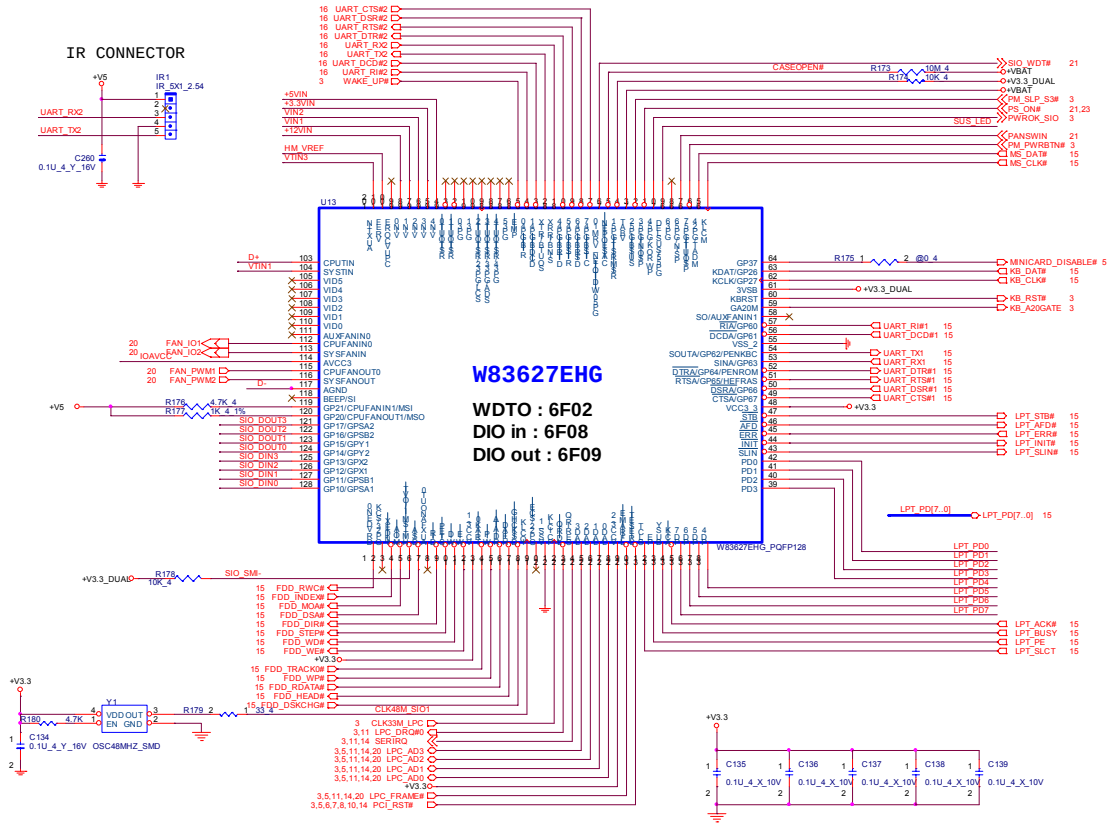


Figure 4-35: Windbond W83627EHG Reference Design

4.12.3.1 Keyboard/Mouse

The following figures display reference circuitries for the legacy I/O interfaces such as PS/2 keyboard/mouse, RS-232 serial port, parallel port and floppy port connected to the Winbond W83627HG Super I/O controller. The PS/2 connector has to be powered

up by the +5V standby voltage to support keyboard and mouse wake up functionality from low power system states (S1 and S3).

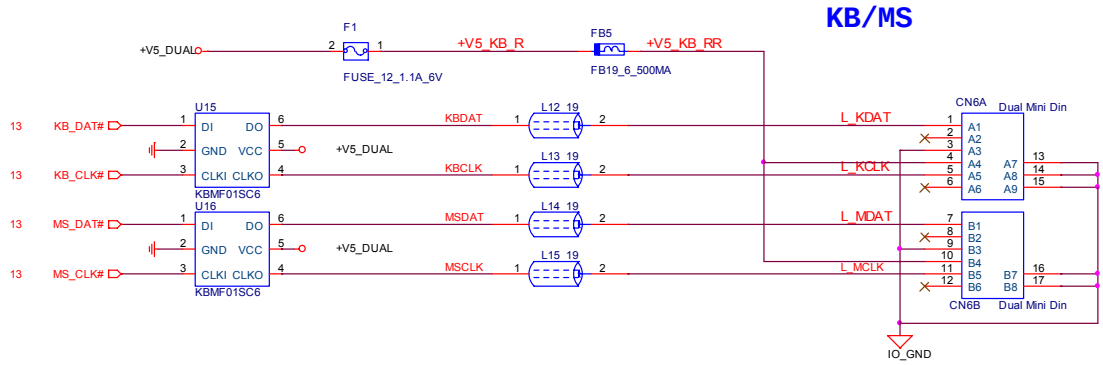


Figure 4-36: Keyboard/Mouse Reference Schematic

4.12.3.2 RS-232/Floppy/LPT/IR

The Winbond W83627provides some other legacy I/O. Please refer to the schematic diagrams suggested by Winbond.

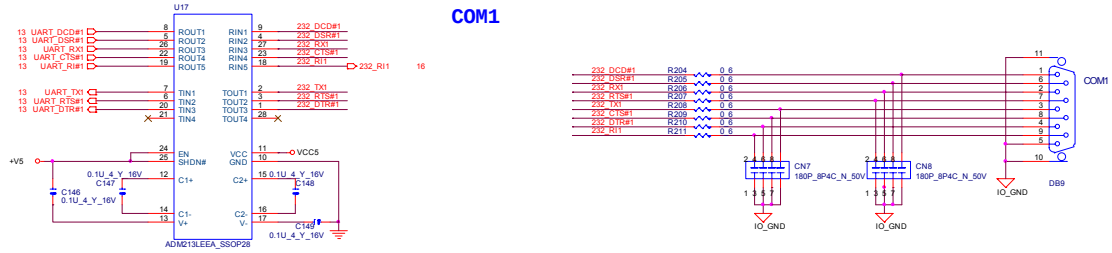


Figure 4-37: RS-232 Reference Schematic

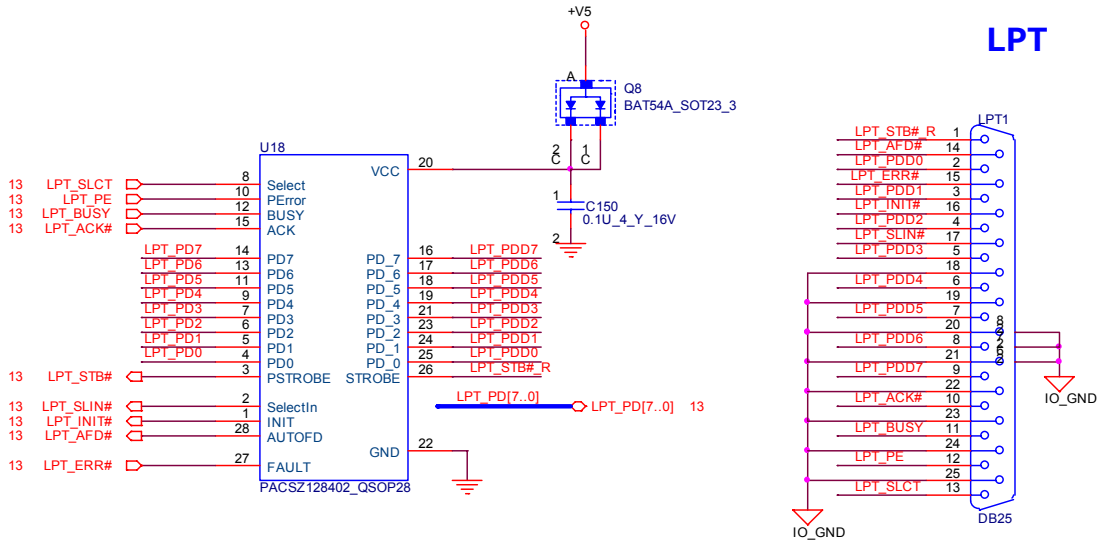


Figure 4-38: LPT Reference Schematic

FLOPPY(only Device A)

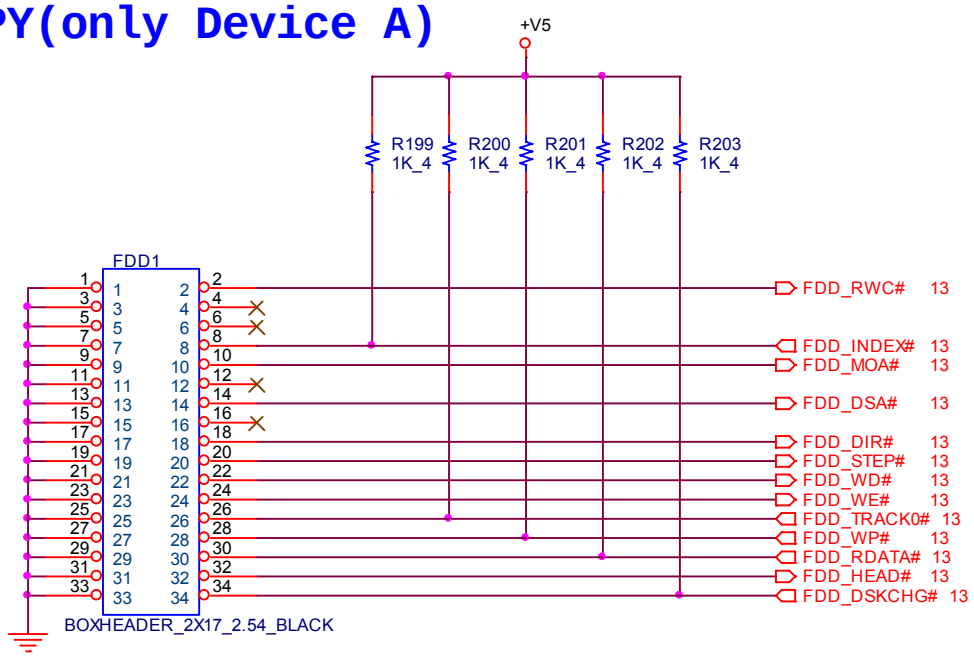


Figure 4-39: Floppy Reference Schematic

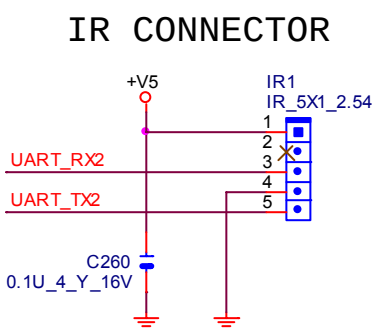


Figure 4-40: IR Reference Schematic

4.13 VGA

COM Express provides analog display signals. There are three signals -- red, green, and blue -- that send color information to a VGA monitor. These three signals each drive an electron gun that emits electrons which paint one primary color at a point on the monitor screen. Analog levels between 0 (completely dark) and 0.7 V (maximum brightness) on these control lines tell the monitor what intensities of these three primary colors to combine to make the color of a dot (or *pixel*) on the monitor's screen.

4.13.1 Signal Description

Table 4-23 shows COM Express VGA signals, including pin number, signals, I/0, power plane, terminal resistors, damping resistors and descriptions.

Table 4-23: VGA signals description

Pin	D-SUB15	Signal	I/O	Description
B89	1	VGA_RED	O Analog	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
B91	2	VGA_GRN	O Analog	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
B92	3	VGA_BLU	O Analog	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
B93	13	VGA_HSYNC	O 3.3V CMOS	Horizontal sync output to VGA monitor.
B94	14	VGA_VSYNC	O 3.3V CMOS	Vertical sync output to VGA monitor.
B95	15	VGA_I2C_CK	I/O 3.3V CMOS	DDC clock line (I2C port dedicated to identify VGA monitor capabilities). DDC data line.
B96		VGA_I2C_DAT	I/O 3.3V CMOS	DDC clock line (I2C port dedicated to identify VGA monitor capabilities). DDC data

		line.
5-8,10	GND	Analog and Digital GND
9	DDC_POWER	5V DDC supply voltage for monitor EEPROM
4,11	NC	Not Connected

4.13.2 VGA Connector

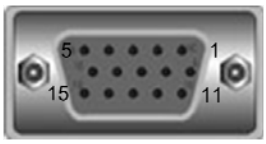


Figure 4-41: VGA Connector D-SUB15

4.13.3 VGA DAC Filter

A video filter is required for each CRT DAC output. This video filter is to be placed in close proximity to the VGA connector. The separation between each of the three video filters for the RGB channels should be maximized if possible to minimize crosstalk.

4.13.4 Routing Guide Line

4.13.4.1 HSYNC and VSYNC Signals

The horizontal and vertical sync signals *'VGA_HSYNC'* and *'VGA_VSYNC'* provided by the COM Express module are 3.3V tolerant outputs. Since VGA monitors may drive the monitor sync signals with 5V tolerance, it is necessary to implement high impedance unidirectional buffers. These buffers prevent potential electrical over-stress of the module and avoid that VGA monitors may attempt to drive the monitor sync signals back to the module

4.13.4.2 ESD

For optimal ESD protection, additional low capacitance clamp diodes should be implemented on the monitor sync signal and DAC. Please see the reference schematic.

4.13.4.3 DDC Interface

COM Express provides a dedicated I2C bus for the VGA interface. It corresponds to the VESA defined DDC interface that is used to read out the CRT monitor specific Extended Display Identification Data (EDID). The appropriate signals *'VGA_I2C_DAT'* and *'VGA_I2C_CK'* of the COM Express module are supposed to be 3.3V tolerant..

ICE Module implement the LVDS EDID ROM on board. If Customer want to fix the resolution or EDID information, please contact IEI for ODM Service.

4.13.5 VGA Reference Design

This reference design shows a circuitry implementing a VGA port.

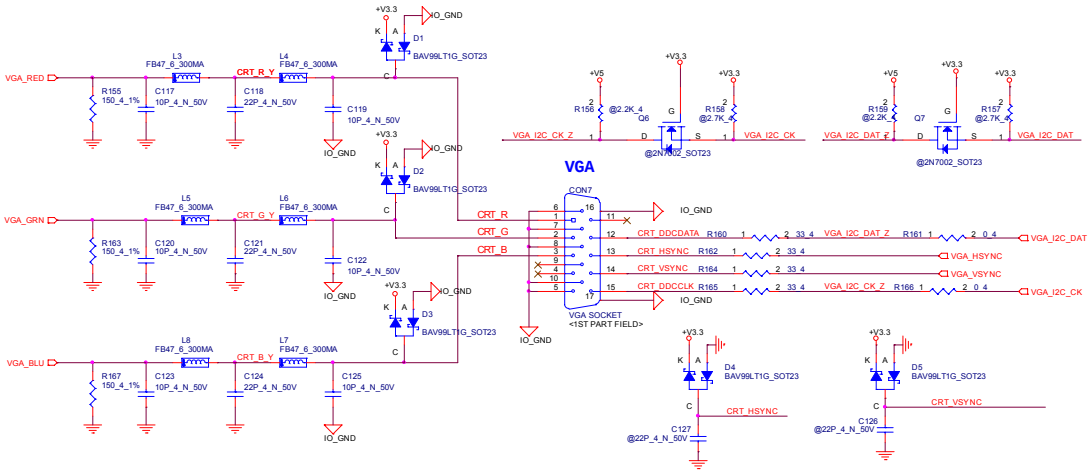


Figure 4-42: VGA Reference Design

4.14 Miscellaneous

This section describes some signals which are not described above, including PI[3:0], GPO[3:0], Watch Dog Timer, Speaker Out, System Reset, Carrier Board Reset, Suspend Control, Power Good, Smart Fan Control,I2C Data, Alert#.

4.14.1 Signal Description

Table 4-24: Miscellaneous pin assignment

Pin	Signal	I/O	Description
B12	PWRBTN#	I CMOS	Power button to bring system out of S5 (soft off), active on rising edge.
B49	SYS_RESET#	I CMOS	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.
B50	CB_RESET#	O CMOS	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.
	PWR_OK	I CMOS	Power OK from main power supply. A high value indicates that the power
B18	SUS_STAT#	O CMOS	Indicates imminent suspend operation; used to notify LPC devices.
A15	PM_SLP_S3#	O CMOS	Indicates system is in Suspend to RAM state. Active low output.
A18	PM_SLP_S4#	O CMOS	Indicates system is in Suspend to Disk state. Active low output.
A24	PM_SLP_S5#	O CMOS	Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.
B66	WAKE0#	I CMOS	PCI Express wake up signal.
B67	WAKE1#	I CMOS	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
A27	BATLOW#	I CMOS	Indicates that external battery is low.
B35	THRM#	I CMOS	Input from off-module temp sensor indicating an over-temp situation.
A35	THERMTRIP#	O CMOS	Active low output indicating that the CPU has entered thermal shutdown.
C77	FAN_TACHOIN	I CMOS	0V~5V Fan Tachometer Input
C67	FAN_PWMOUT	O CMOS	Fan Speed Control PWM Control
B13	SMB_C	I/O 3.3V	System Management Bus (SMBus) is used by the COM
B14	SMB_DAT	OD CMOS	Express module for memory configuration and clock synthesizer configuration. It is also used by the external PCI Express slots and ExpressCard slots.
B33	I2C_CK	I/O 3.3V	General purpose I2C bus for common usage on the carrier
B34	I2C_DAT	CMOS	board.
B15	SMB_ALERT#	I 3.3V CMOS	The SMBus alert signal used by the SMBus slave to inform the SMBus master " Optional signal used by the SMBus slave. that a slave transaction is pending.
B32	SPKR	O CMOS	Output for audio enunciator - the "speaker" in PC-AT

			systems
A34	BIOS_DISABLE#	I CMOS	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.
B27	WDT	O CMOS	Output indicating that a watchdog time-out event has occurred.
A86	KBD_RST#	I CMOS	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.
A87	KBD_A20GATE	I CMOS	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.
	GPO[0:3]	OI CMOS	General purpose output pins. Upon a hardware reset, these outputs should be low.
	GPI[0:3]	I CMOS	General purpose input pins. Pulled high internally on the module.
	TYPE[0:2]#	TBD	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pin-out Type 1, these pins are don't care (X).

TYPE2#	TYPE1#	TYPE0#	
X	X	X	Pin-out Type 1
NC	NC	NC	Pin-out Type 2
NC	NC	GND	Pin-out Type 3 (no IDE)
NC	GND	NC	Pin-out Type 4 (no PCI)
NC	GND	GND	Pin-out Type 5 (no IDE, no PCI)

The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.

PS: In IEI carrier board, these pins are for future use.

4.14.2 Speaker/FAN Control/RTC Reference

4.14.2.1 Speaker Out

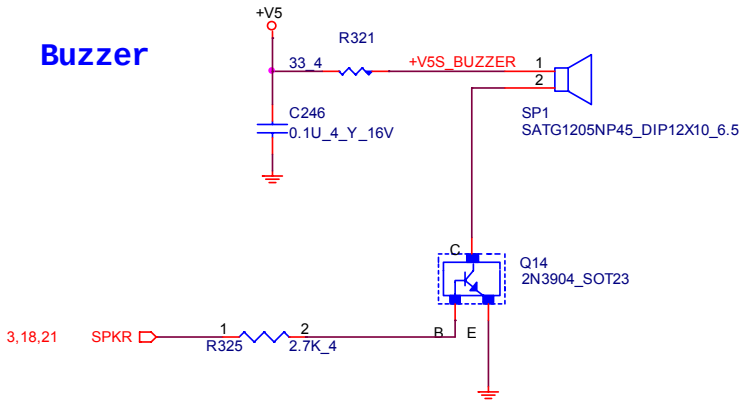


Figure 4-43: Speaker Out Reference Schematic

4.14.2.2 FAN Control

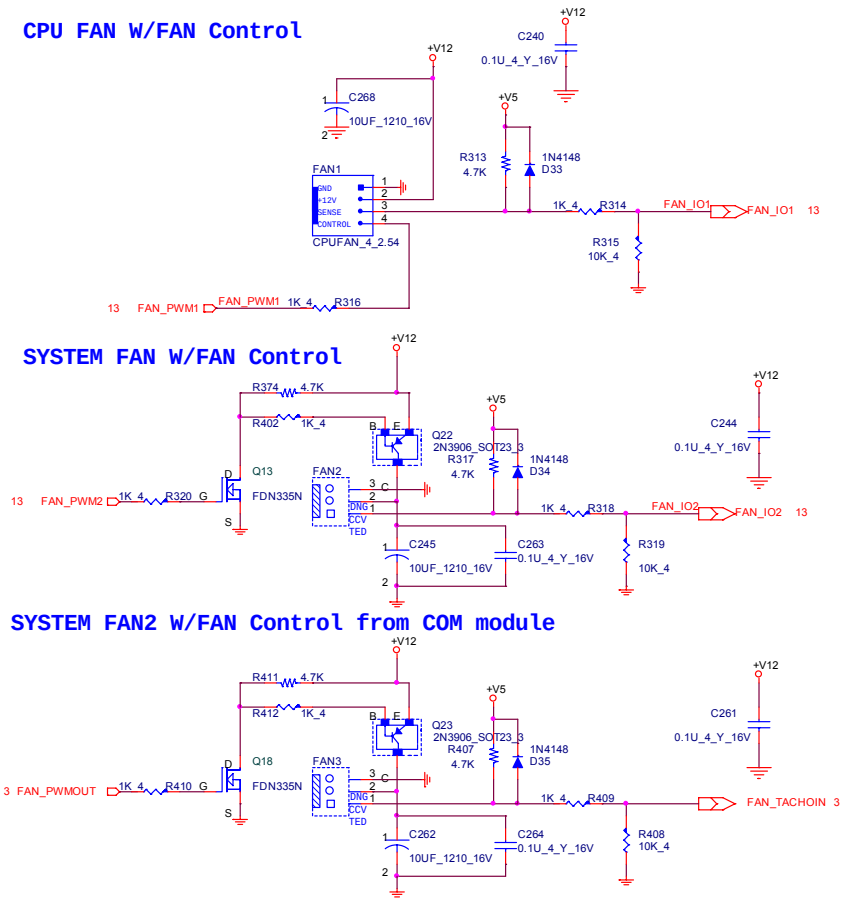


Figure 4-44: FAN Reference Schematic

4.14.2.3 RTC

Q10,C234 and R304 are for the no battery solution. Using super CAP to instead of Battery.

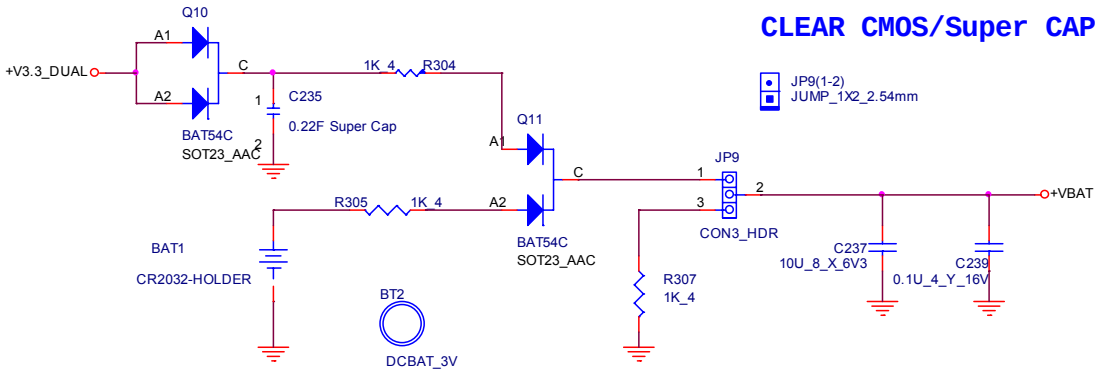


Figure 4-45: RTC Reference Schematic

Chapter

5

PCB Stack and Power Deliver Design

5.1 Chapter Overview

A brief description of the Printed Circuit Board (PCB) for COM Express based board is provided in this section. From a cost- effectiveness point of view, a four-layer board is the target platform for the motherboard design. For better quality, a six-layer or 8-layer board is preferred. This chapter also provides the ATX/AT power supply design recommendation for customer's reference. **IEI ICE module carrier board use 4-layer PCB stack.**

5.2 Microstrip or Stripline

Either edge-coupled microstrip, edge-coupled stripline, or broad-side striplines are recommended for designs with differential signals. Designs with microstrip lines offer the advantage that a lower number of layers can be used. Also, with microstrip lines it may be possible to route from a connector pad to the device pad without any via. This provides better signal quality on the signal path that connects devices. A limitation of microstrip lines is that they can only be routed on the two outside layers of the PCB, thus routing channel density is limited.

Stripline may be either edge-coupled or broad-side coupled lines. Stripline designs provide additional shielding since they are embedded in the board stack and are typically sandwiched between ground and power planes. This reduces radiation and coupling of noise onto the lines. Striplines have the disadvantage that they require the use of vias to connect to them.

5.3 PCB Stackup Example

It is recommended to use PCB's with at least a 4-layer stackup where the impedance controlled layer 1 (top layer) is used for differential signals and layer 4 (bottom layer) for other periodic signals (CMOS/TTL). The dedicated power planes (layer 2 – GND and layer 3 – VCC) are typically required for high-speed designs. The solid ground plane is necessary to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground planes will additionally create an excellent high frequency bypass capacitance. The following example shows a four layer PCB stackup using microstrip trace routing. A good rule to follow for microstrip designs is to keep S < W and S < H ("H" = space between differential signal layers and the reference plane). The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

5.3.1 Four-Layer Stack-up

Figure 5-1 below is an example of a four layer stack-up. Layers L1 and L4 are used for signal routing. Layers L2 and L3 are used for solid ground and power planes respectively. Microstrips on Layers 1 and 4 reference ground and power planes on Layers 2 and 3 respectively. In some cases, it may be advantageous to swap the GND and PWR planes. This allows Layer 4 to be GND referenced. Layer 4 is clear of parts and may be the preferred primary routing layer.

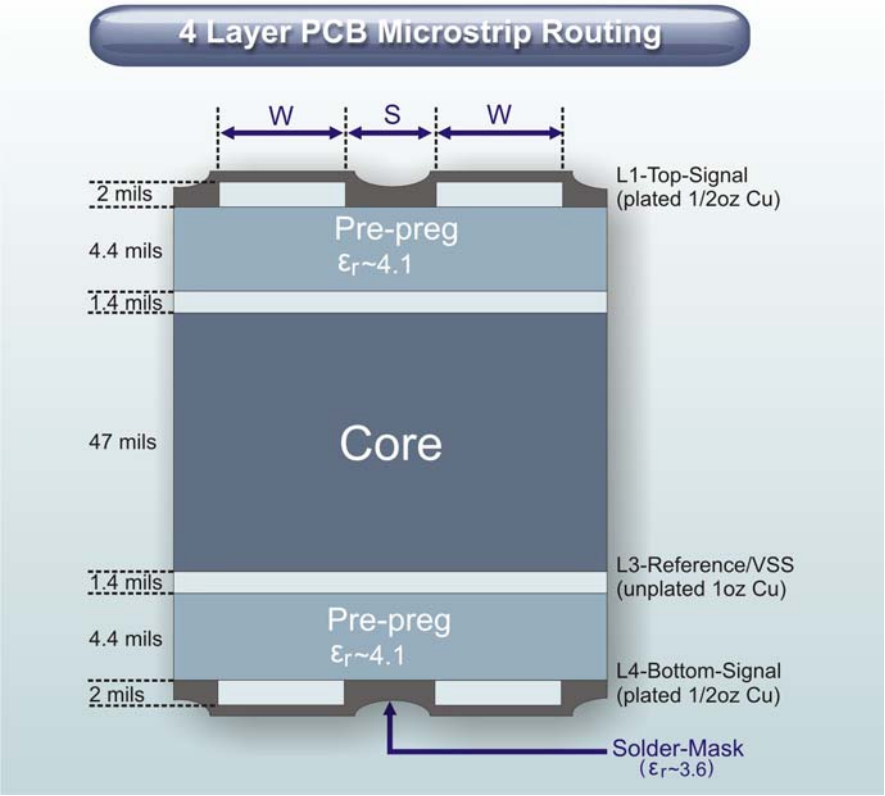


Figure 5-1: Four Layers Stack

5.3.2 Six-Layer Stack-up

Figure 5-2 below is an example of a six layer stack-up. Layers L1, L3, L4 and L6 are used for signal-routing. Layers L2 and L5 are power and ground planes respectively. Microstrips on Layers 1 and 6 reference solid ground and power planes on Layers 2 and 5 respectively. Inner Layers 3 and 4 are asymmetric striplines that are referenced to planes on Layers 2 and 5.

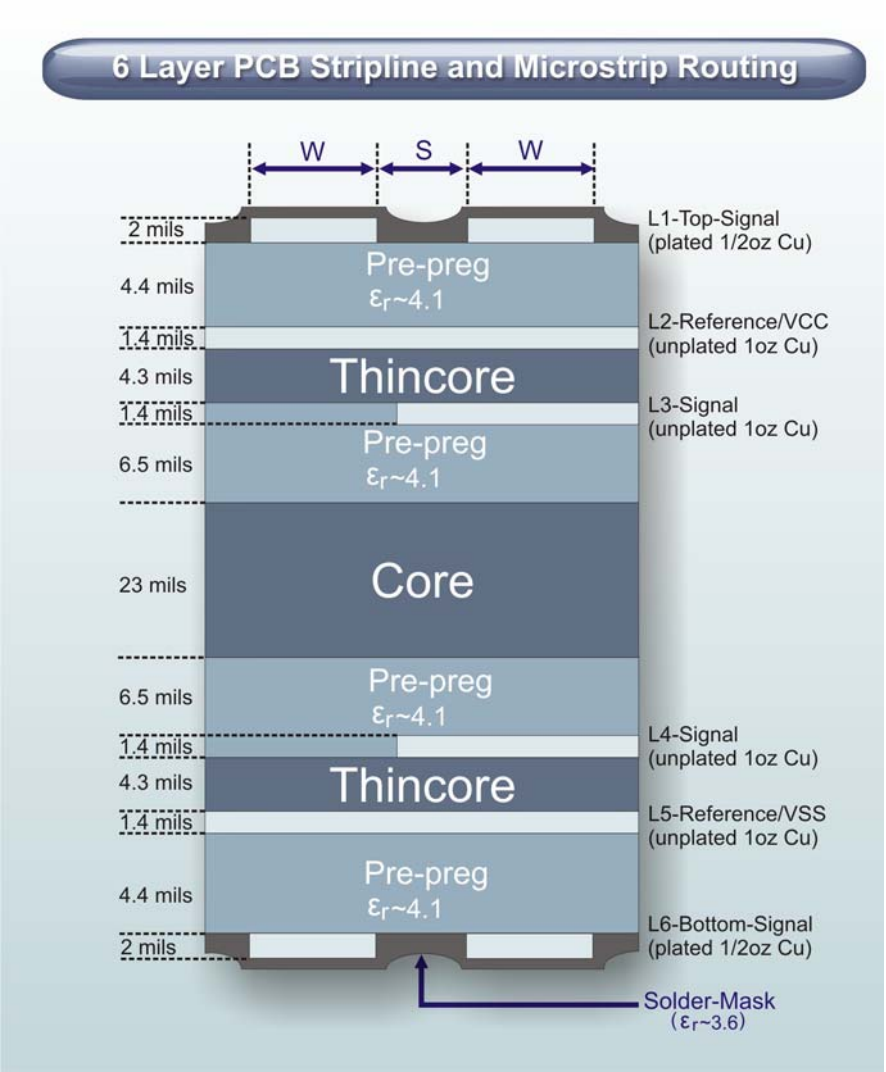


Figure 5-2: Six Layers Stack

NOTE:

- All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.
- IEI recommends that high-speed signal routing be done on internal, strip-line layers.
- For high-speed signals transitioning between layers next to the component, the signal pins should be accounted for by the GND stitching vias that would stitch all the GND plane layers in that area of the board.

- High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching if routing is done on both internal and external layers.

5.4 ATX Power Delivery Guidelines

The COM Express module uses a single main power rail with a nominal value of +12V. Two additional rails are specified: a +5V standby power rail and a +3V battery input to power the module Real-time Clock (RTC) circuit in the absence of other power sources. The +5V standby rail may be left unconnected on the Carrier Board if the standby functions are not required by the application. Likewise, the +3V battery input may be left open if the application does not require the RTC to keep time in the absence of the main and standby sources. There may be module specific concerns regarding storage of system setup parameters that may be affected by the absence of the +5V standby and / or the +3V battery.

The rationale for this power-delivery scheme is:

- Module pins are scarce. It is more pin-efficient to bring power in on a higher voltage rail.
- Lithium ion battery packs for mobile systems are most prevalent with a +14.4V output. This is well suited for the +12V main power rail.
- Contemporary chipsets have no power requirements for +5V other than to provide a reference voltage for +5V tolerant inputs. No COM Express module pins are allocated to accept +5V except for the +5V standby pins. In the case of an ATX supply, the switched (non standby) +5V line would not be used for the COM Express module, but it might be used elsewhere on the Carrier Board.

5.4.1 ATX Power Status (S0,S3,S4,S5,G3)

ATX power source will provide 12V , -12V , 5V , -5V , 3.3V , 5VSBY power , if other voltage is required (3.3VSBY , LAN1.8V….) on carried board. The additional switching regulator or LDO will be necessary. Power states are described by the following terms:

Table 5-1: Signal Tables Terminology Descriptions

State	Description	Comment
G3	Mechanical Off	AC power to system is removed, by a mechanical switch. System power consumption is near zero – the only power consumption is that of the RTC circuits powered by a backup battery.
S5	Soft Off	System is off except for a small subset that is powered by the 5V suspend rail. There is no system context preserved. VCC_5V_SBY current consumption is system dependent, and it may be from tens of milliamps up to several hundred milliamps.
S4	Suspend to Disk	System is off except for a small subset that is powered by the 5V suspend rail. System context is preserved on a non-volatile disk media (that is powered off). VCC_5V_SBY current consumption is system dependent, and it may be from tens of milliamps up to several hundred milliamps.
S3	Suspend to RAM	System is off except for system subset that includes the RAM. Suspend power is provided by the 5V suspend rail. System context is preserved in the RAM. VCC_5V_SBY current consumption is system dependent, and it may be from several hundred milliamps up to a maximum of 2A.
S0	On	System is on.

Table 5-2: Power State Behavior

State	SUS_S5#	SUS_S4#	SUS_S3#
G3	N/A	N/A	N/A
S5	Low	Low	Low
S4	High	Low	Low
S3	High	High	Low
S0	High	High	High

5.4.2 ATX Power Diagram

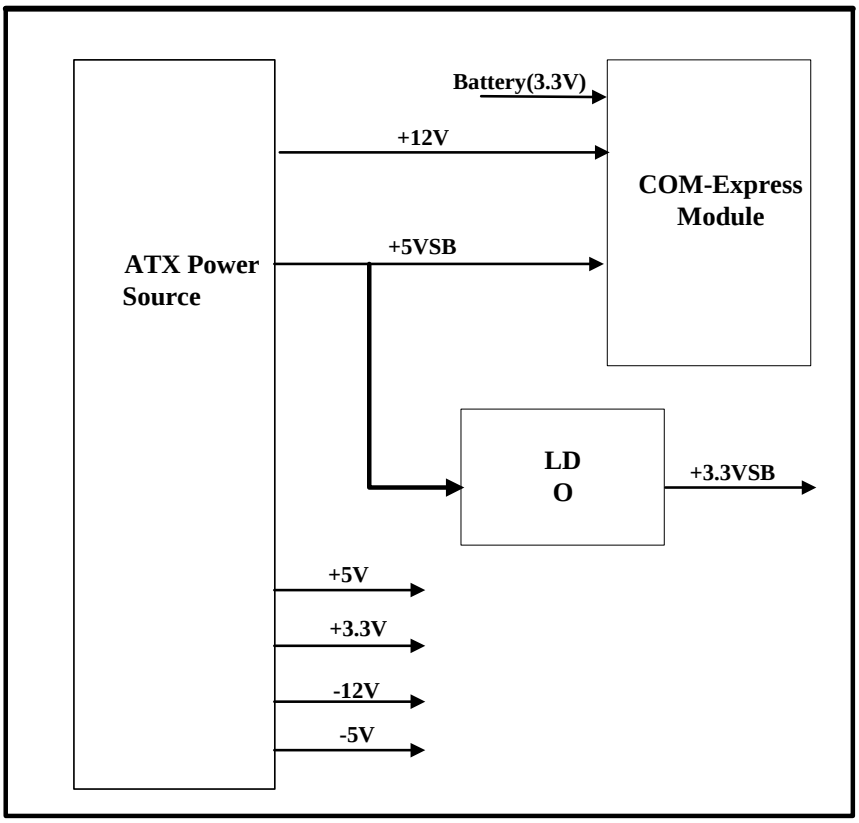


Figure 5-3: ATX Power Delivery Block Diagram

6.3.3 ATX Power On Timing

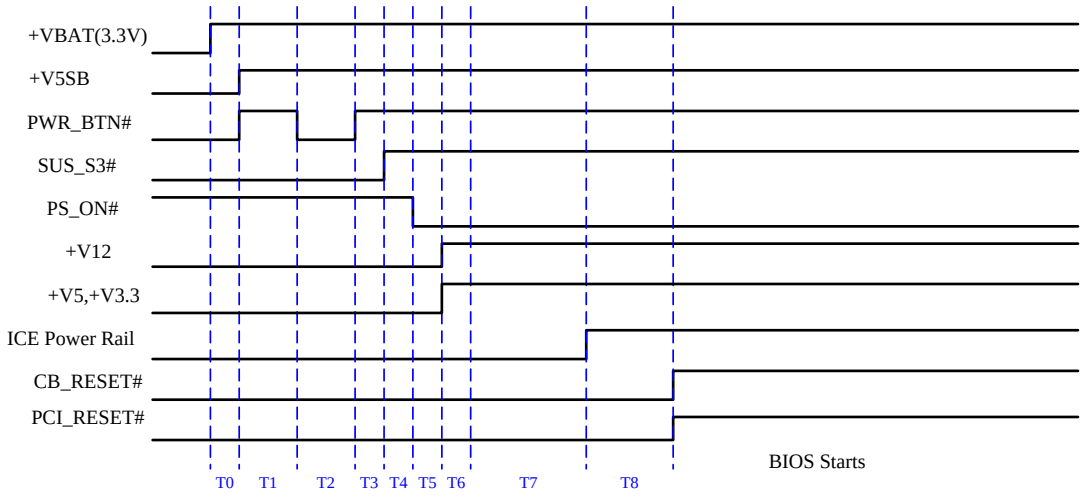


Figure 5-4: ATX Power On Sequence

Table 5-3: ATX Power On Sequence Timing

Parameters	min	Max	Description
T0			
T1			
T2			
T3			
T4			
T5			
T6			
T7			
T8			

5.5 AT Power Delivery Guideline

AT power source will provide 12V, 5V power. The additional switching regulator or LDO will be required to simulate the ATX power (3.3V…). There will be no standby voltage once AT power source be used.

5.5.1 AT Power Diagram

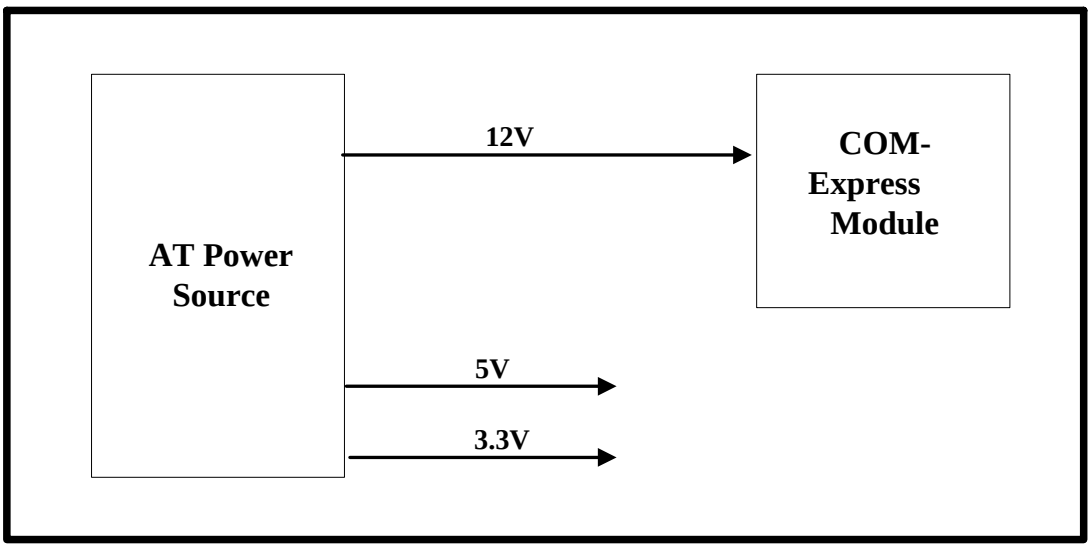
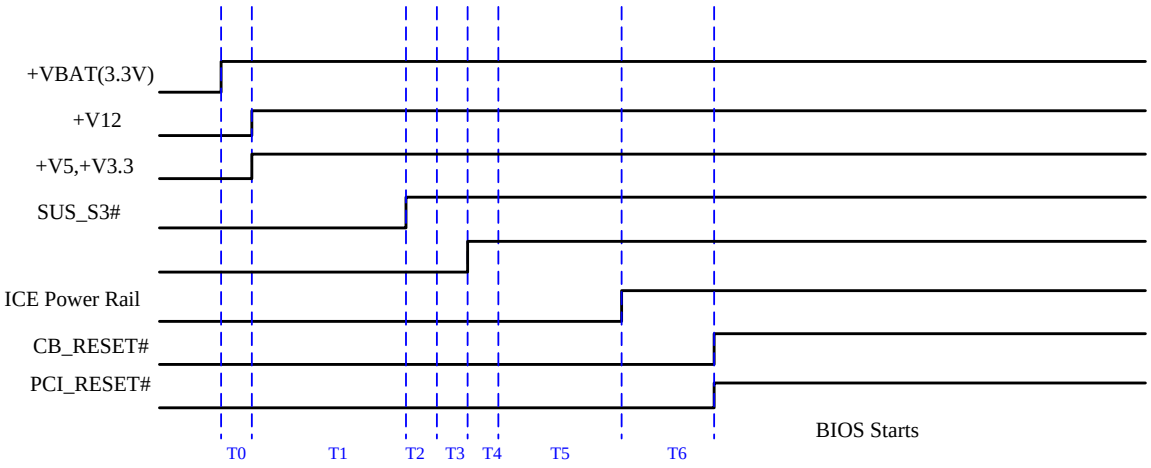


Figure 5-5: AT Power Delivery Block Diagram

5.5.2 AT Power On Timing



Notes: Do not need 5VSB.

Figure 5-6: AT Power On Sequence

Table 5-4: AT Power On Sequence Timing

Parameters	min	Max	Description
T0			
T1			
T2			
T3			
T4			
T5			
T6			

NOTE:

Please follow the power requirement provided in Chapter 2 to design the baseboard requested by the customer.

Chapter

6

Mechanical Design Guidelines

6.1 Chapter Overview

The interconnection between COM Express modules and the carrier board uses two 220 pin 0.5mm fine pitch board-to-board connectors. Each single 220-pin connector is split into two connector rows. This results in a total of 440 pins and 4 connector rows. These connectors should be capable of driving up to 6.25GHz Low Voltage Differential Signals to match the requirements for PCI Express signaling.

6.2 COM Module and Carrier Board Connector

6.2.1 Module Connector

The module connector for Pin-out Types 2 through 5 shall be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors may be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. Module Pin-out Type 1 shall use a single 220-pin, 0.5 mm pitch receptacle. The connectors shall be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds.

AMP / Tyco 3-1318490-6 0.5 mm pitch Free Height 220 pin 4H Receptacle, or equivalent

AMP / Tyco 8-1318490-6 0.5 mm pitch Free Height 220 pin 4H Receptacle, or equivalent

Sources for the individual 220-pin receptacle are (same as previous part, but with anti-wicking solution applied) A source for the combined 440-pin receptacle (composed of 2 pieces of the 220 pin receptacle held by a carrier) is: AMP / Tyco 3-1827231-6 0.5mm pitch Free Height 440 pin 4H Receptacle or equivalent. Note: the part number above shown with a leading ‘8’ has an anti-wicking solution applied that may help in processing with an aggressive flux. The other versions of the parts may also be made available with this solution by the vendor. The module connector is a receptacle by virtue of the vendor’s technical definition of a receptacle, and to some users it looks like a plug.

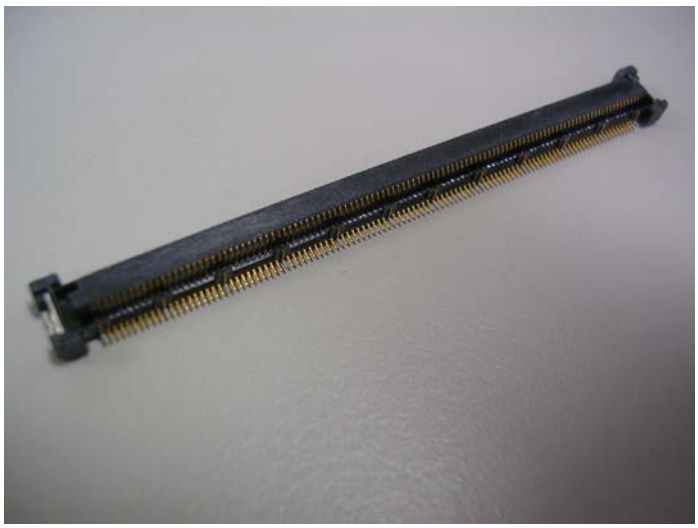


Figure 6-1: Module Connector Picture

6.2.2 Carrier Board Connector

The single 220-pin 0.5mm pitch carrier board connectors are 5H/8H plug in connectors with a board-to-board stack height of 5.0mm/8.0mm. A potential source for this plug-in board-to-board connector is:

3-1827253-6 AMP/Tyco HARD TRAY ASSY FH 0.5 BTB CONNECTOR 220POS PLUG 5H WITH GROUND PLATE (5.0mm stack height)

8-1318491-6 AMP/Tyco HARD TRAY ASSY FH 0.5 BTB CONNECTOR 220POS PLUG 8H WITH GROUND PLATE (8.0mm stack height)

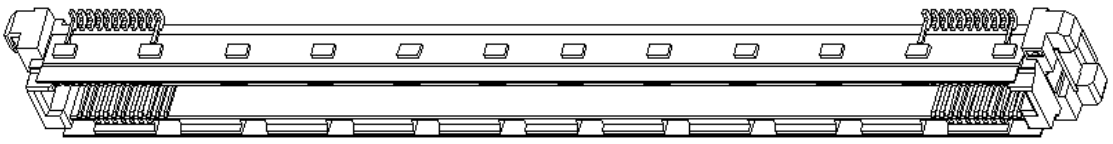


Figure 6-2: Carrier Board Connector

6.3 Connector Footprint

For carrier board designs it is essential that the distance and the alignment of the dual connector shape on the PCB comply to the dimensions defined by the COM Express Specification. The alignment between the two single connectors is guaranteed by the connectors peg holes shown in following drawings. It is very important that the PCB drill tolerances of these peg holes are within the recommended ranges mentioned below. Otherwise, the interconnection between module and carrier board may cause functional problems for the system. Instead of two single connectors, a dual connector model with a reinforcing bar spacer can be used to ensure the alignment between the two connectors during assembly. All dimensions of the following drawings are shown in millimeters or Hirose FX8-100S connector detail spec, please reference the Hirose website.

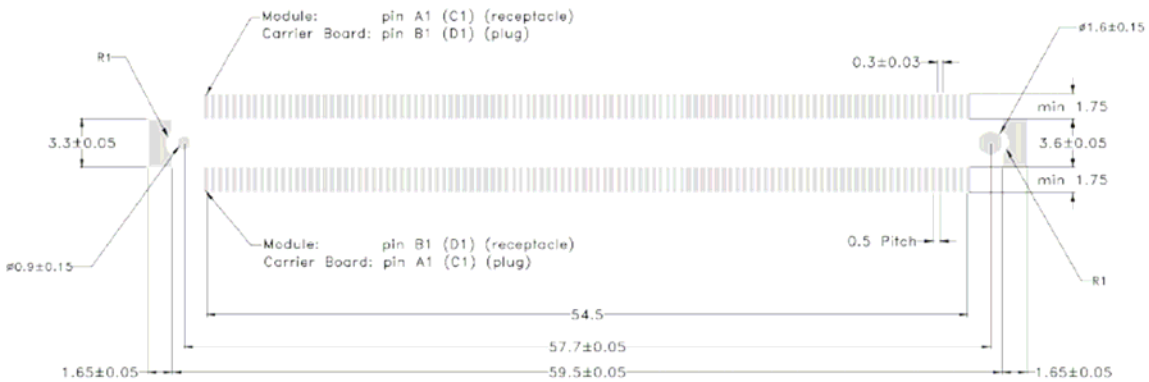


Figure 6-3: Single Connector Physical Dimensions

Figure 6-4: Dual Connector Footprint and Alignment

The COM Express PnP Initiative strongly recommends to use the following location
peg hole tolerances instead of those indicated in the footprint drawings from the
COM Express Specification as shown above:

- ***0.8mm +0.075/-0.025mm***
- ***1.5mm +0.075/-0.025mm***

6.4 COM Express Form Factors

The COM Express specification was developed by the PCI Industrial Computer Manufacturing Group (PICMG) in close collaboration with many leading companies across the embedded industry in order to find an implementation solution to handle upcoming new high speed serial I/Os, processors and chipsets. COM Express specifies two form factors, as well as five different types of connector pinouts. The two form factors are referred to as Basic and Extended. The Basic module footprint is 125mm x 95mm and focuses on space-constrained, low power systems which typically do not contain more than one horizontal mounted SO-DIMM. The Extended footprint is slightly larger at 155mm x 110mm and supports up to two full size, vertically mounted DIMM modules to accommodate larger memory configurations for high-performance CPUs, chipsets and multiprocessor systems. The placement of the shielded 220-pin connectors and the mounting holes are identical between these two footprints.

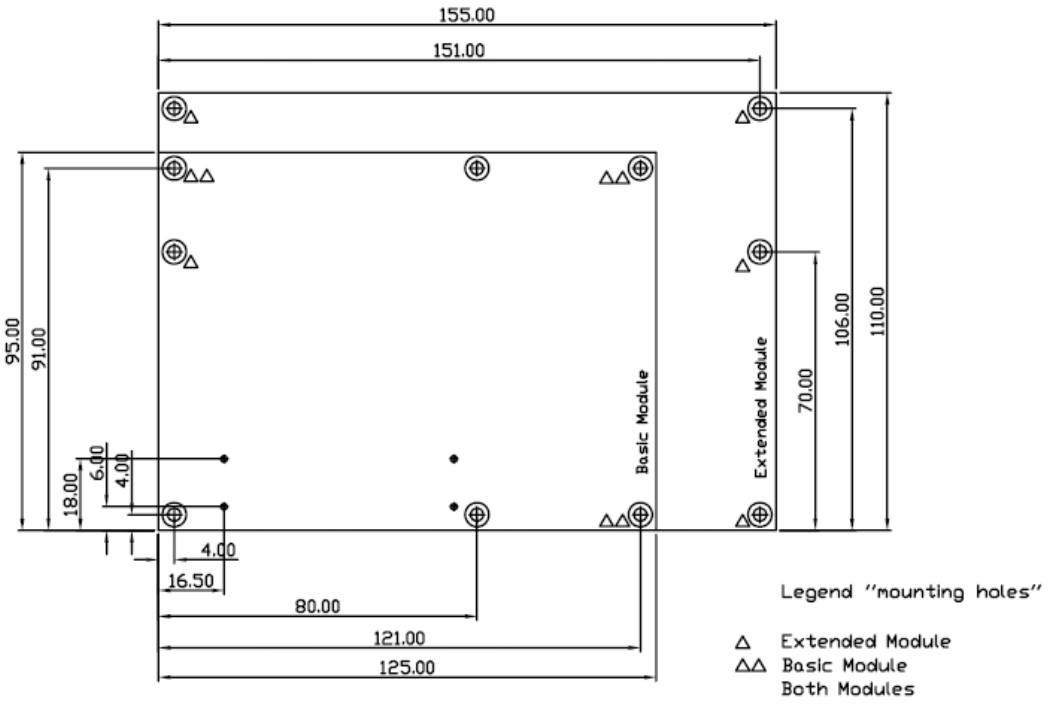


Figure 6-5: Compact, Basic and Extended Form Factor

6.5 Heat Spread

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the Module. Usually It is a 3mm thick aluminum plate. The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some Modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers. Although the heatspreader is the thermal interface where most of the heat generated by the Module is dissipated, it is not to be considered as a heat sink. It has been designed to be used as a thermal interface between the Module and the application specific thermal solution.

The application specific thermal solution may use heat sinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater. The main mechanical mounting solutions for systems based on COM Express Modules have proven to be the 'top-mounting' and 'bottom-mounting' solutions. The decision as to which solution will be used is determined by the mechanical construction and the cooling solution of the customer's system. There are two variants of the heatspreader, one for each mounting possibility.

One version has threaded standoffs and the other has non-threaded standoffs (bore hole). The following sections describe these two common mounting possibilities and the additional components (standoffs, screws, etc...) that are necessary to implement the respective solution.

Modules should be equipped with a heat-spreader. This heat-spreader by it self does not constitute the complete thermal solution for a module but provides a common interface between modules and implementation-specific thermal solutions. The overall module height from the bottom surface of the module board to the heat-spreader top surface shall be 13 mm for both the Basic and Extended Modules. The module PCB and heat-spreader plate thickness are vendor implementation specific, however, a 2-mm PCB with a 3-mm heat-spreader may be used which allows use of readily available standoffs.

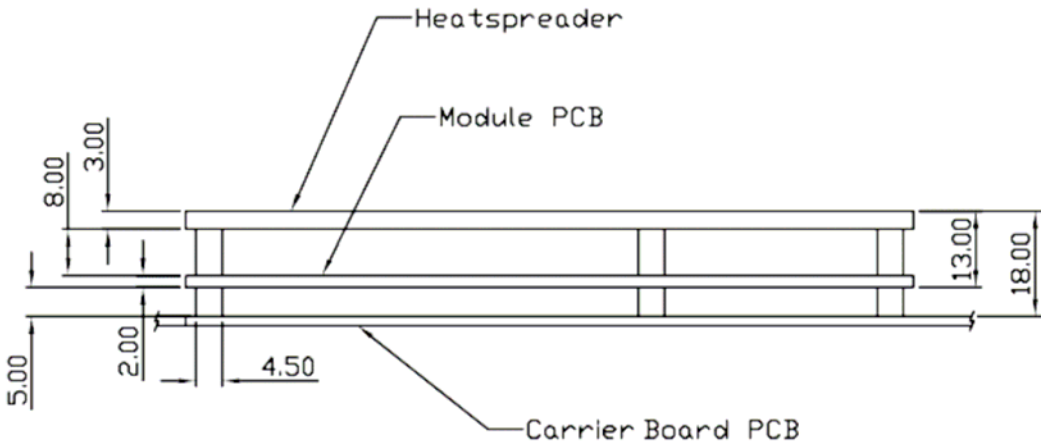


Figure 6-6: Overall Height for Heat-Spreader in Basic and Extended Modules

All dimensions in mm. Tolerances (unless otherwise specified): Z (height) dimensions should be ± 0.8mm [±0.031”] from top of Carrier Board to top of heat-spreader. Heat-spreader surface should be flat within 0.2mm [.008"] after assembly. Interface surface finish should have a maximum roughness average (Ra) of 1.6µm [63µin]. The critical dimension in Figure 6-8 is the module PCB bottom side to heat-spreader top side. This dimension shall be 13.00mm ± 0.65mm [±0.026”]. Figure 6-8 shows a cross section of a module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.

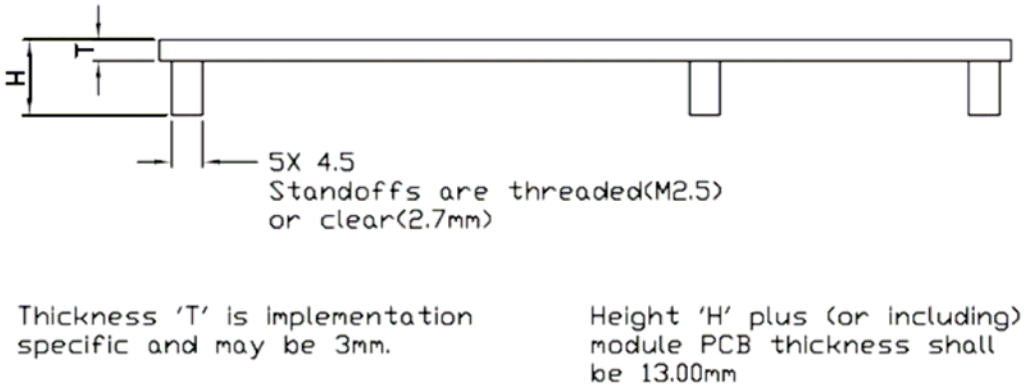


Figure 6-7: Basic Module Heat-Spreader

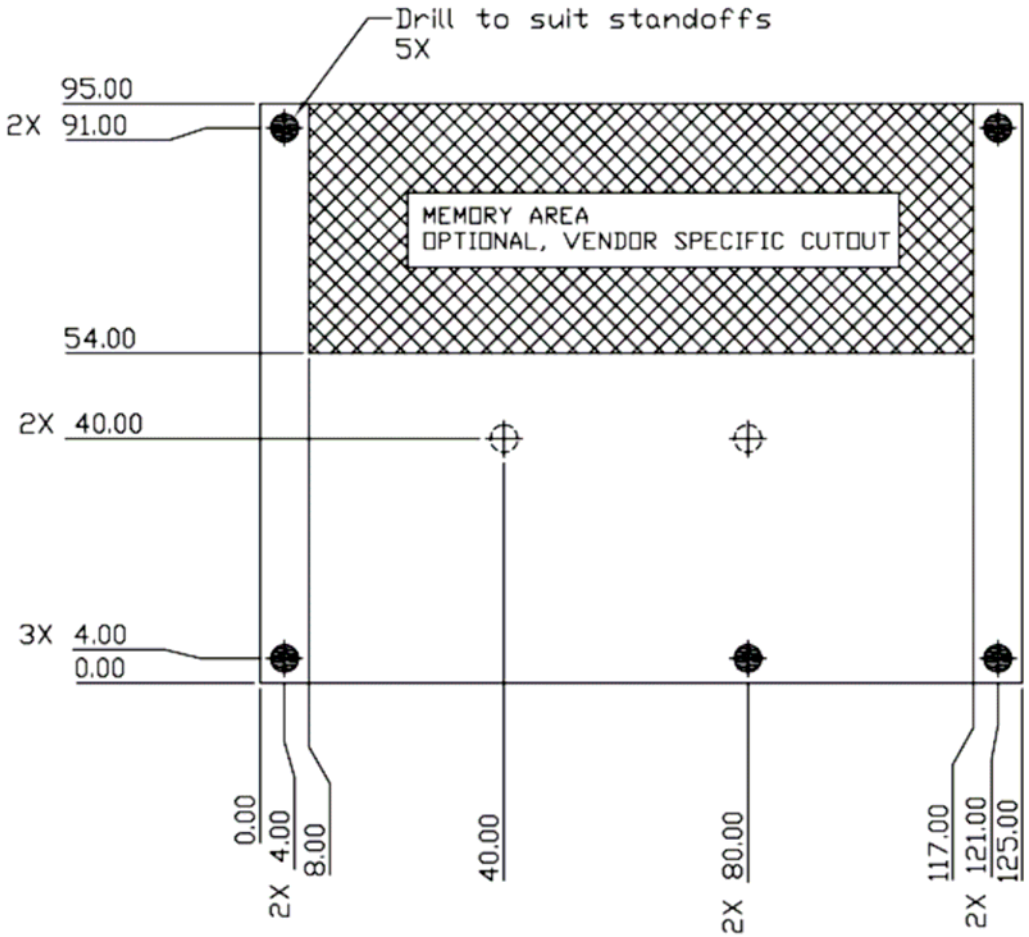


Figure 6-8: Basic Module Heat-Spreader Footprint

All dimensions are in mm. X-Y tolerances shall be ± 0.3mm [±0.012"].

The interior holes at coordinates (40, 40) and (80, 40) are tapped through holes with a M2.5 thread. The interior holes do not receive standoffs. These holes may be sealed on the module side by an adhesive backed foil, or they may be blind tapped holes with a minimum thread depth of 2.5 mm. They are intended to allow additional attachment points to the heat-spreader from outside the module.

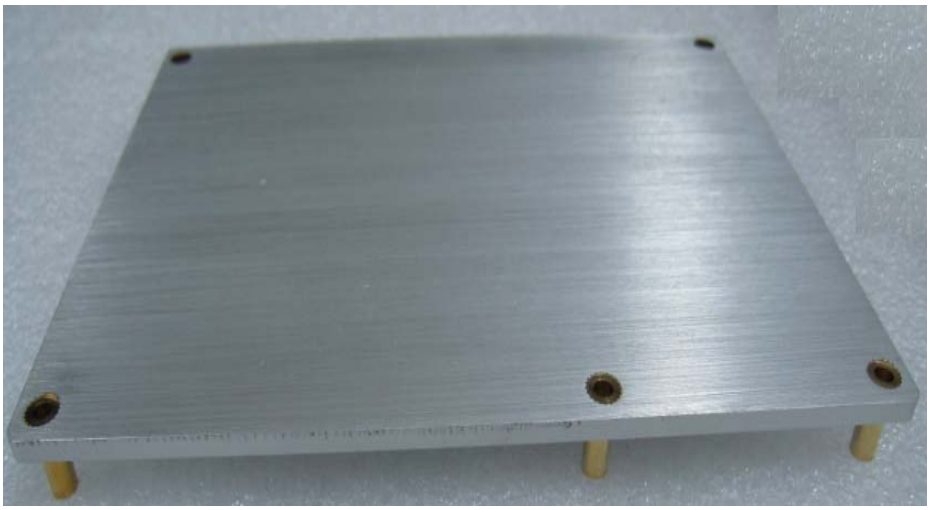


Figure 6-9: IEI Heat Spread Module

6.6 Design Notes

6.6.1 Component Height — Module Back and Carrier Board Top

Parts mounted on the backside of the module (in the space between the bottom surface of the module PCB and the Carrier Board) shall have a maximum height of 3.8 mm (dimension 'B' in Figure 6-11). With the 5 mm stack option, the clearance between the Carrier Board and the bottom surface of the module's PCB is 5 mm (dimension 'A' in Figure 6-11). Using the 5 mm stack option, components placed on the Carrier Board topside under the module envelope shall be limited to a maximum height of 1 mm (dimension 'C' in Figure 6-11), with the exception of the mating connectors. Using Carrier Board topside components up to 1mm allows a gap of 0.2 mm between Carrier Board module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height should be restricted to a value less than 1mm that yields a clearance that is sufficient for the application. If the Carrier Board uses the 8 mm stack option (dimension 'A' in Figure 6-11), then the

Carrier Board topside components within the module envelope shall be limited to a height of 4 mm (dimension ‘C’ in Figure 6-11), with the exception of the mating connectors. Using Carrier Board topside components up to 4mm allows a gap of 0.2 mm between Carrier Board topside components and module bottom side components. This may not be sufficient in some situations. In Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height should be restricted to a value less than 4 mm that yields a clearance that is sufficient for the application.

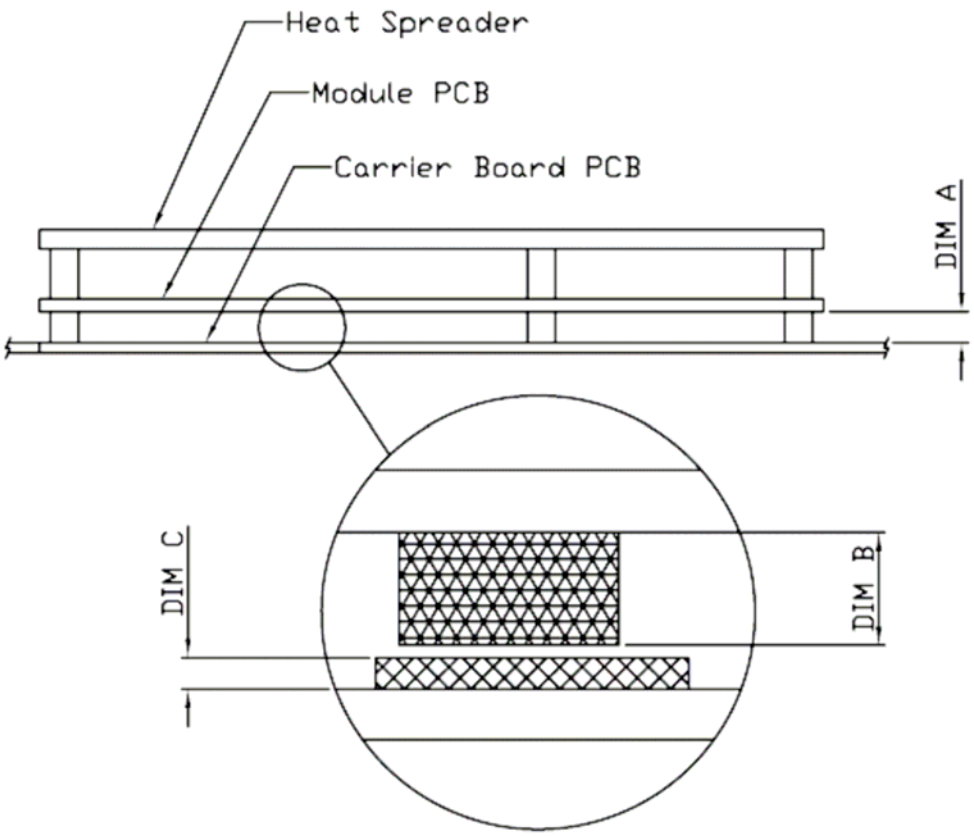


Figure 6-10: Component Clearances Underneath Module

6.6.2 Air Follow Issue

The air flow of the IEI COM Express fan module must be considered when installing a COM Express system. Please refer to Figure 6-11 for air flow consideration.

6.6.3 Grounding Issue

The mounting holes on all ICE COM modules are connected to digital circuit ground (GND) for improved EMC performance. Using conductive screws and distance keepers will also connect the heat spreader and attached heat sink to GND. In some applications the heat sink or heat spreader will be directly screwed with the inner surface of the chassis. In some cases, however, it may not be desirable to have a direct connection of circuit ground (GND) and chassis ground through the heat sink and / or heat spreader. System designers should take this into account when defining system grounding.

6.7 Others Kits Specification

6.7.1 Heat Sink

IEI provides a standard heat sink specially designed for COM Express module. The fan in the heat sink can be removed if the fan is not needed.

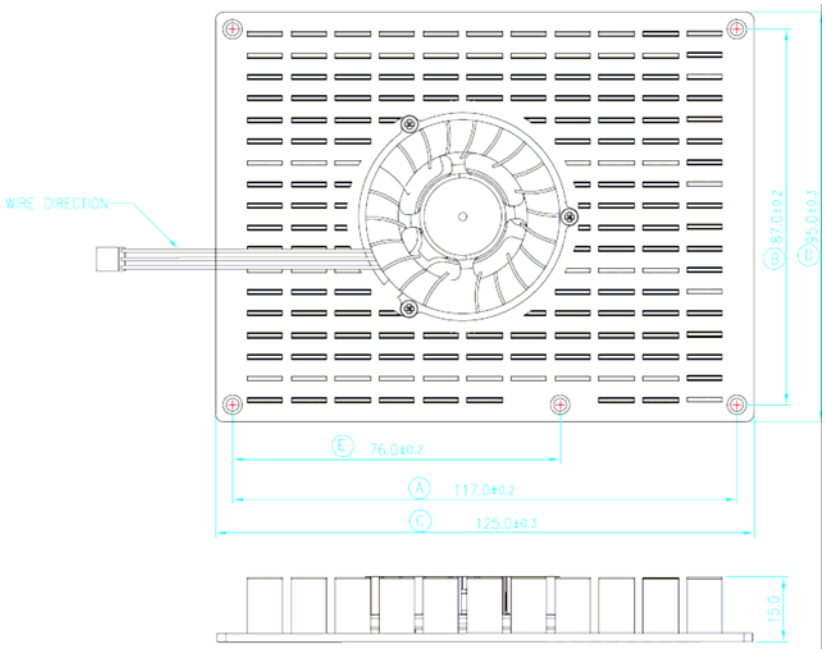


Figure 6-11: IEI Heat Sink Module Dimensions

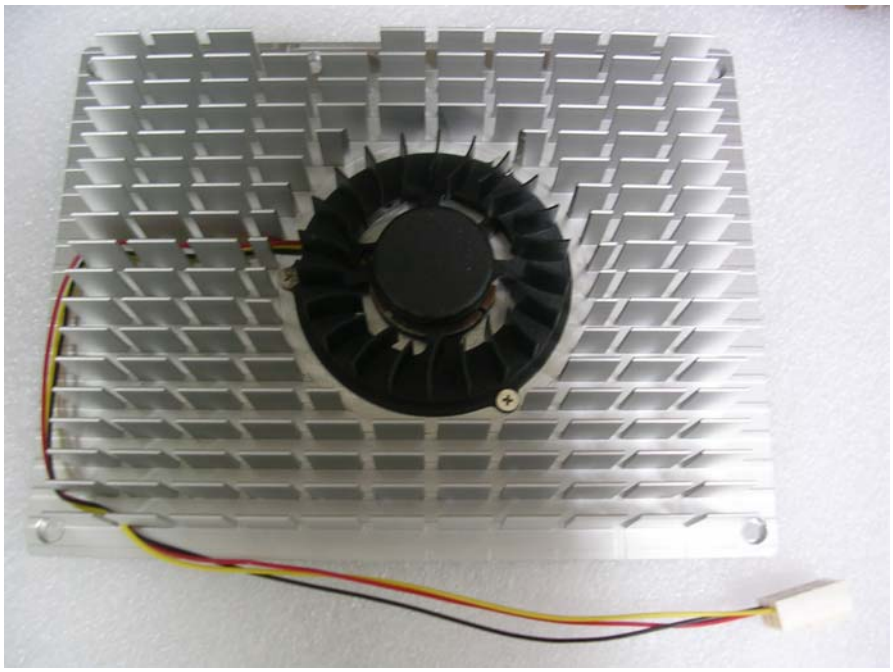


Figure 6-12: IEI Heat Sink Module Picture

Appendix

A

ICE Module Design Schematic Check List

		COM Module			
Pin	Signal	PU/PD	Series	Notes	V
C52 C53	PEG_RX0+ PEG_RX0-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D52 D53	PEG_TX0+ PEG_TX0-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C55 C56	PEG_RX1+ PEG_RX1-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D55 D56	PEG_TX1+ PEG_TX1-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C58 C59	PEG_RX2+ PEG_RX2-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D58 D59	PEG_TX2+ PEG_TX2-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C61 C62	PEG_RX3+ PEG_RX3-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D61 D62	PEG_TX3+ PEG_TX3-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C65 C66	PEG_RX4+ PEG_RX4-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D65 D66	PEG_TX4+ PEG_TX4-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C68 C69	PEG_RX5+ PEG_RX5-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D68 D69	PEG_TX5+ PEG_TX5-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C71 C72	PEG_RX6+ PEG_RX6-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D71 D72	PEG_TX6+ PEG_TX6-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C74 C75	PEG_RX7+ PEG_RX7-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them	

				near to TX side (near to destination) as per PCI-E Device	
D74 D75	PEG_TX7+ PEG_TX7-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C78 C79	PEG_RX8+ PEG_RX8-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D78 D79	PEG_TX8+ PEG_TX8-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C81 C82	PEG_RX9+ PEG_RX9-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D81 D82	PEG_TX9+ PEG_TX9-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C85 C86	PEG_RX10+ PEG_RX10-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D85 D86	PEG_TX10+ PEG_TX10-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C88 C89	PEG_RX11+ PEG_RX11-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D88 D89	PEG_TX11+ PEG_TX11-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C91 C92	PEG_RX12+ PEG_RX12-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D91 D92	PEG_TX12+ PEG_TX12-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C94 C95	PEG_RX13+ PEG_RX13-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D94 D95	PEG_TX13+ PEG_TX13-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C98 C99	PEG_RX14+ PEG_RX14-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
D98 D99	PEG_TX14+ PEG_TX14-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
C101 C102	PEG_RX15+ PEG_RX15-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package)	

				and place them near to TX side (near to destination) as per PCI-E Device	
D101 D102	PEG_TX15+ PEG_TX15-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
A88 A98	PCIE_CLK_REF+ PCIE_CLK_REF-	-	33 ohm	Directly connect to PCIe Device or Buffer IC	
D73	SDVO_I2C_CLK	-	-	Directly connect to SDVO Transmitter. Using 4.7K to 10K pull up to 2.5V.	
C73	SDVO_I2C_DATA	-	-	Directly connect to SDVO Transmitter. Using 4.7K to 10K pull up to 2.5V.	
B66	WAKE0#	PU		Connect to PCIE wake up signal	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
B68 B69	PCIE_RX0+ PCIE_RX0-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
A68 A69	PCIE_TX0+ PCIE_TX0-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
B64 B65	PCIE_RX1+ PCIE_RX1-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
A64 A65	PCIE_TX1+ PCIE_TX1-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
B61 B62	PCIE_RX2+ PCIE_RX2-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
A61 A62	PCIE_TX2+ PCIE_TX2-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
B58 B59	PCIE_RX3+ PCIE_RX3-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
A58 A59	PCIE_TX3+ PCIE_TX3-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
B55 B56	PCIE_RX4+ PCIE_RX4-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination) as per PCI-E Device	
A55 A56	PCIE_TX4+ PCIE_TX4-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
B52 B53	PCIE_RX5+ PCIE_RX5-	-	-	Provide 0.1-µF AC coupling capacitors (0402 or 0603 package) and place them near to TX side (near to destination)	

				as per PCI-E Device	
A52 A53	PCIE_TX5+ PCIE_TX5-	-	0.1U Cap 0.1U Cap	Directly connect to PCIe Device or Slot.	
A88 A98	PCIE_CLK_REF+ PCIE_CLK_REF-	-	33 ohm	Directly connect to PCIe Device or Buffer IC	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
	PCI_AD[0..31]	-	-	Directly connect to PCI Device	
	PCI_C/BE[0..3]#	-	-	Directly connect to PCI Device	
C36	PCI_DEVSEL#	PU	-	Directly connect to PCI Device	
D36	PCI_FRAME#	PU	-	Directly connect to PCI Device	
C37	PCI_IRDY#	PU	-	Directly connect to PCI Device	
D35	PCI_TRDY#	PU	-	Directly connect to PCI Device	
D34	PCI_STOP#	PU	-	Directly connect to PCI Device	
D32	PCI_PAR	-	-	Directly connect to PCI Device	
C34	PCI_PERR#	PU	-	Directly connect to PCI Device	
	PCI_REQ[0..3]#	PU	-	Directly connect to PCI Device	
	PCI_GNT[0..3]#	-	-	Directly connect to PCI Device	
C23	PCI_RESET#	-	-	PCI_RESET# should be connected to PCI slots and PCI down devices.	
C35	PCI_LOCK#	PU		Directly connect to PCI Device	
D33	PCI_SERR#	PU	-	Directly connect to PCI Device	
C15	PCI_PME#	PU	-	Directly connect to PCI Device	
D48	PCI_CLKRUN#	PU	-	Directly connect to PCI Device	
	PCI_IRQ[A..D]#	PU	-	Directly connect to PCI Device	
D50	PCI_CLK		33 ohm	Directly connect to PCIe Device or Buffer IC	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A19 A20	SATA0_RX+ SATA0_RX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
A16 A17	SATA0_TX+ SATA0_TX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
B19 B20	SATA1_RX+ SATA1_RX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
B16 B17	SATA1_TX+ SATA1_TX-	-	0.01U Cap	Directly connect to SATA Connector	

			0.01U Cap		
A25 A26	SATA2_RX+ SATA2_RX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
A22 A23	SATA2_TX+ SATA2_TX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
B25 B26	SATA3_RX+ SATA3_RX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
B22 B23	SATA3_TX+ SATA3_TX-	-	0.01U Cap 0.01U Cap	Directly connect to SATA Connector	
A28	SATA_ACT#	PU	-	Please refer to ICE Demo Board	
If unused, these signals can be left as NC.					
				-	
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A46 A45	USB0+ USB0-	-	-	Directly connect to USB Device	
B46 B45	USB1+ USB1-	-	-	Directly connect to USB Device	
A43 A42	USB2+ USB2-	-	-	Directly connect to USB Device	
B43 B42	USB3+ USB3-	-	-	Directly connect to USB Device	
A40 A39	USB4+ USB4-	-	-	Directly connect to USB Device	
B40 B39	USB5+ USB5-	-	-	Directly connect to USB Device	
A37 A36	USB6+ USB6-	-	-	Directly connect to USB Device	
B37 B36	USB7+ USB7-	-	-	Directly connect to USB Device	
B44	USB_0_1_OC#	PU	-	-	
A44	USB_2_3_OC#	PU	-	-	
B38	USB_4_5_OC#	PU	-		
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A30	AC_RST#	-	33 ohm	Directly connect to HAD Chip	
A29	AC_SYNC	-	33 ohm	Directly connect to HAD Chip	
A32	AC_BITCLK	-	33 ohm	Directly connect to HAD Chip	
A33	AC_SDOUT	-	33 ohm	Directly connect to HAD Chip	
B30 B29 B28	AC_SDIN0 AC_SDIN1 AC_SDIN2	-	33 ohm	Directly connect to HAD Chip	

If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
B89	VGA_RED	PD	-	Please refer to chapter 4	
B91	VGA_GRN	PD	-	Please refer to chapter 4	
B92	VGA_BLU	PD	-	Please refer to chapter 4	
B93	VGA_HSYNC	-	Buffer	Please refer to chapter 4	
B94	VGA_VSYNC	-	Buffer	Please refer to chapter 4	
B95	VGA_I2C_CK	PU	-	Please refer to chapter 4	
B96	VGA_I2C_DAT	PU	-	Please refer to chapter 4	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A71 A72	LVDS_A0+ LVDS_A0-	-	-	Directly connect to LCD panel	
A73 A74	LVDS_A1+ LVDS_A1-	-	-	Directly connect to LCD panel	
A75 A76	LVDS_A2+ LVDS_A2-	-	-	Directly connect to LCD panel	
A78 A79	LVDS_A3+ LVDS_A3-	-	-	Directly connect to LCD panel	
A81 A82	LVDS_A_CK+ LVDS_A_CK-	-	-	Directly connect to LCD panel	
B71 B72	LVDS_B0+ LVDS_B0-	-	-	Directly connect to LCD panel	
B73 B74	LVDS_B1+ LVDS_B1-	-	-	Directly connect to LCD panel	
B75 B76	LVDS_B2+ LVDS_B2-	-	-	Directly connect to LCD panel	
B77 B78	LVDS_B3+ LVDS_B3-	-	-	Directly connect to LCD panel	
B81 B82	LVDS_B_CK+ LVDS_B_CK-	-	-	Directly connect to LCD panel	
A77	LVDS_VDD_EN	PD	-	Please refer to chapter 4	
B79	LVDS_BKLT_EN	-	-	Please refer to chapter 4	
B83	LVDS_BKLT_CTRL	-	-	Please refer to chapter 4	
A83	LVDS_I2C_CK	PU	-	Directly connect to LCD panel	
A84	LVDS_I2C_DAT	PU		Directly connect to LCD panel	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
B97	TV_DAC_A	PD-	-	Please refer to chapter 4	
B98	TV_DAC_B	PD	-	Please refer to chapter 4	
B99	TV_DAC_C	PD	-	Please refer to chapter 4	

If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
D7	IDE_D[0..15]	-	-	Please refer to chapter 4	
D13 D14 D15	IDE_A[0:2]	-	-	Please refer to chapter 4	
D9	IDE_IOW#	-	-	Please refer to chapter 4	
C14	IDE_IOR#	-	-	Please refer to chapter 4	
D8	IDE_REQ	-	-	Please refer to chapter 4	
D10	IDE_ACK#	-	-	Please refer to chapter 4	
D16	IDE_CS1#	-	-	Please refer to chapter 4	
D17	IDE_CS3#	-	-	Please refer to chapter 4	
C13	IDE_IORDY	PU	-	Please refer to chapter 4	
D18	IDE_RESET#	-	-	Please refer to chapter 4	
D12	IDE_IRQ	PU	-	Please refer to chapter 4	
D77	IDE_CBLID#	-	-	Please refer to chapter 4	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A13 A12	GBE0_MDI0+ GBE0_MDI0-	PD RC	-	Directly connect to LAN transformer	
A10 A9	GBE0_MDI1+ GBE0_MDI1-	PD RC	-	Directly connect to LAN transformer	
A7 A6	GBE0_MDI2+ GBE0_MDI2-	PD RC	-	Directly connect to LAN transformer	
A3 A2	GBE0_MDI3+ GBE0_MDI3-	PD RC	-	Directly connect to LAN transformer	
A14	GBE0_CTREF	-	-	Please refer to chapter 4	
A8	GBE0_LINK#	-	-	Please refer to chapter 4	
A4	GBE0_LINK100#	-	-	Please refer to chapter 4	
A5	GBE0_LINK1000#	-	-	Please refer to chapter 4	
B2	GBE0_ACT#			Please refer to chapter 4	
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
A50	LPC_SERIRQ	-	-	Please refer to chapter 4	
B3	LPC_FRAME#	-	-	Please refer to chapter 4	
B4 B5 B6 B7	LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	-	-	Please refer to chapter 4	

B8 B9	LPC_DRQ0# LPC_DRQ1#	-	-	Please refer to chapter 4	
B10	LPC_CLK	-	33ohm		
If unused, these signals can be left as NC.					
Pin	**Signal**	**PU/PD**	**Series**	**Notes**	**V**
B12	PWRBTN#	PU	-	Please refer to chapter 4	
B49	SYS_RESET#	PU	-	Please refer to chapter 4	
B50	CB_RESET#	PU	-	Please refer to chapter 4	
	PWR_OK	PU	-	Please refer to chapter 4	
B18	SUS_STAT#	-	-	Please refer to chapter 4	
A15	PM_SLP_S3#	-	-	Please refer to chapter 4	
A18	PM_SLP_S4#	-	-	Please refer to chapter 4	
A24	PM_SLP_S5#	-	-	Please refer to chapter 4	
B66	WAKE0#	PU	-	Please refer to chapter 4	
B67	WAKE1#	PU	-	Please refer to chapter 4	
A27	BATLOW#	PU	-	Please refer to chapter 4	
B35	THRM#	PU	-	Please refer to chapter 4	
A35	THERMTRIP#	PU	-	Please refer to chapter 4	
C77	FAN_TACHOIN	PU	-	Please refer to chapter 4	
C67	FAN_PWMOUT	PU	-	Please refer to chapter 4	
B13 B14	SMB_CK SMB_DAT	PU	-	Please refer to chapter 4	

Appendix

B

Application Notes

NOTE:

IEI is able to provide customers with the ICE module design guide and information as well as many other application notes. IEI will keep the ICE module information most updated. Please contact IEI for the latest design guide and related information.

B.1 Terminology

Some of the following terms may be used throughout this section.

Term	Description
BIOS	Basic Input Output System. BIOS is actually firmware, the software that is programmed into a ROM (Read-Only Memory) chip built onto the motherboard of a computer
AFUWIN	AMI BIOS Update Tool
RTC	Real-Time Clock

B.2 Updating BIOS Version

There are two ways to update the BIOS version.

- In the OS environment, use AFUWIN application to update BIOS.
- In the DOS environment, use “GO” command to update BIOS.

The following sections describe how to use these two methods to update BIOS version. Before updating BIOS, please check the BIOS version in the BIOS menu (Figure 6-13). To get the BIOS menu, press the Delete key when the system is booting up.

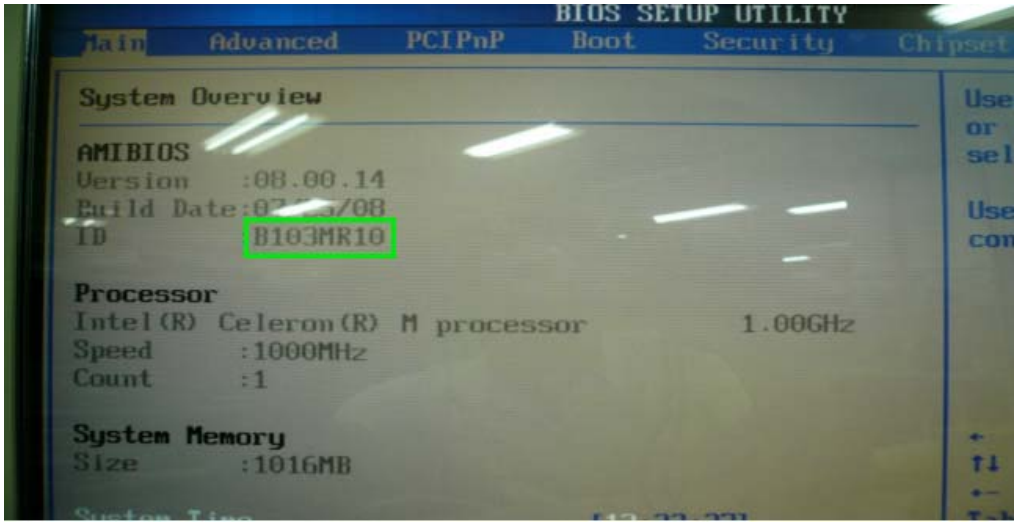


Figure 6-13: BIOS Main Menu (BIOS Version: MR10)

B.2.1 Using AFUWIN

To use AFUWIN application to update the BIOS version, follow the steps below.

Step 1: Install and launch AFUWIN.

Step 2: Click Open button to open the BIOS file (Figure 6-14).

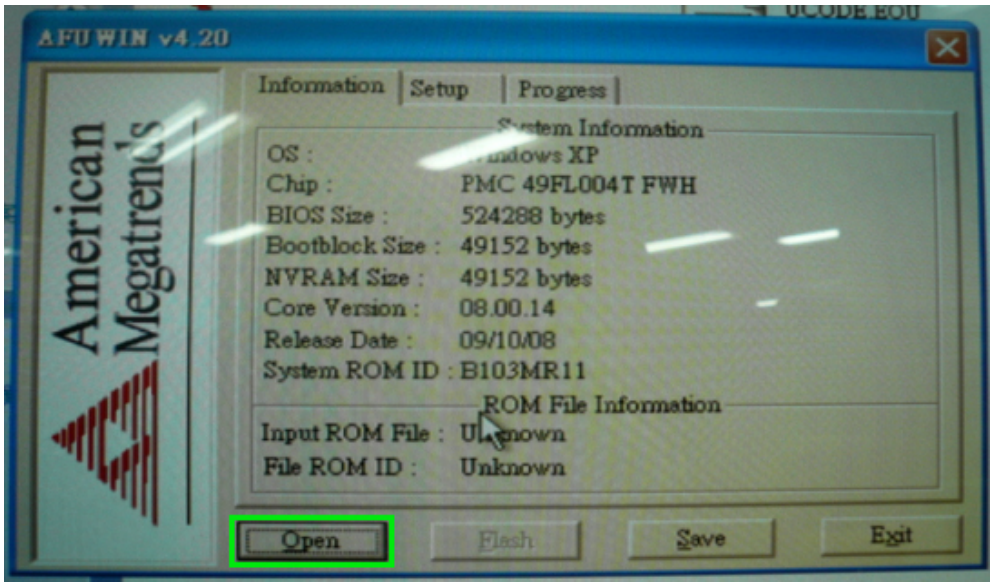


Figure 6-14: AFUWIN – Open BIOS File

Step 3: Locate the BIOS file that needs to be updated (Figure 6-15).

Figure 6-15: Locate BIOS File

Step 4: Check ”Program All Block” option (Figure 6-16).

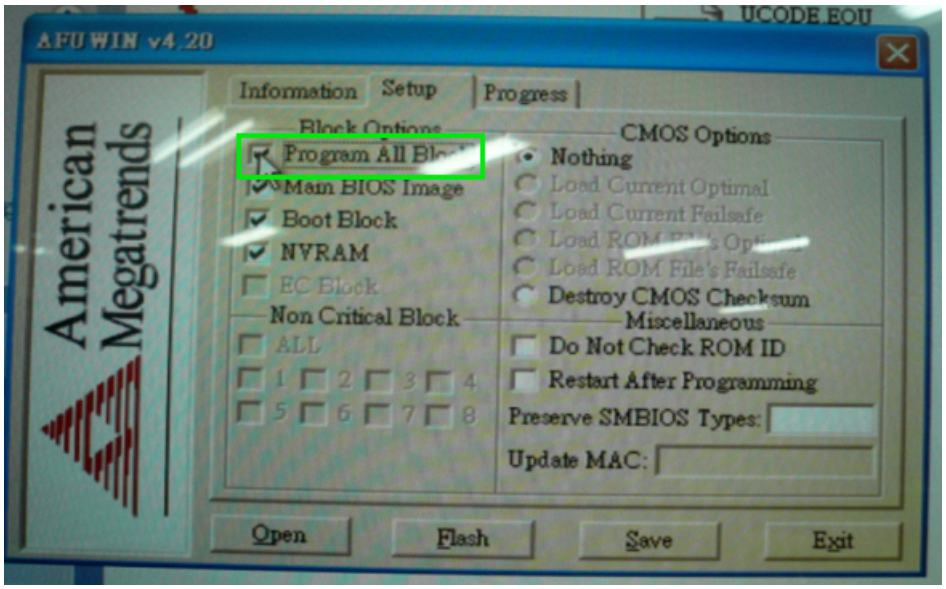


Figure 6-16: Check Program All Block

Step 5: Click **Flash** button to start updating BIOS (Figure 6-17).

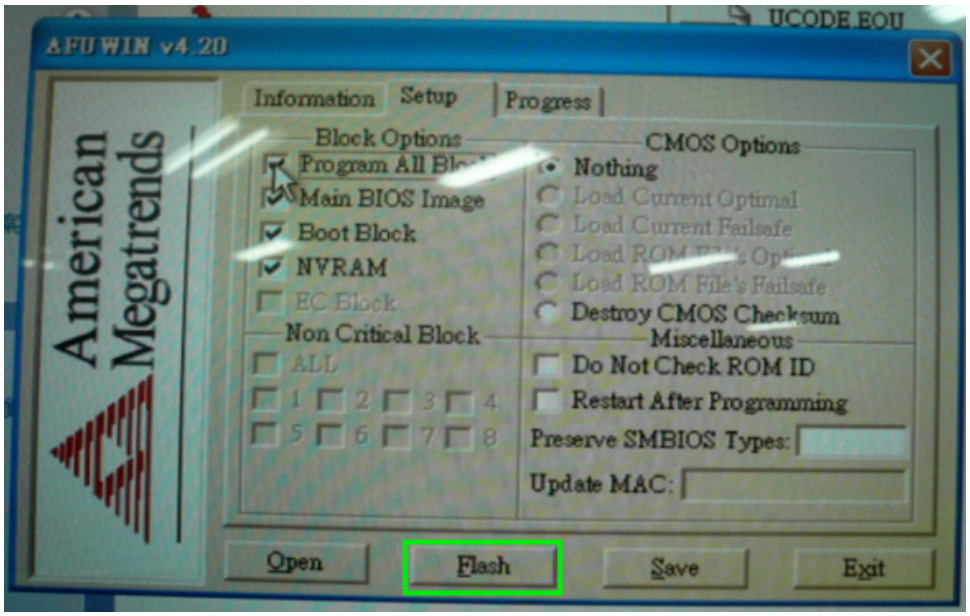


Figure 6-17: AFUWIN – Flash

Step 6: Restart the system and check the BIOS menu. The BIOS version is changed to MR11 (Figure 6-18).

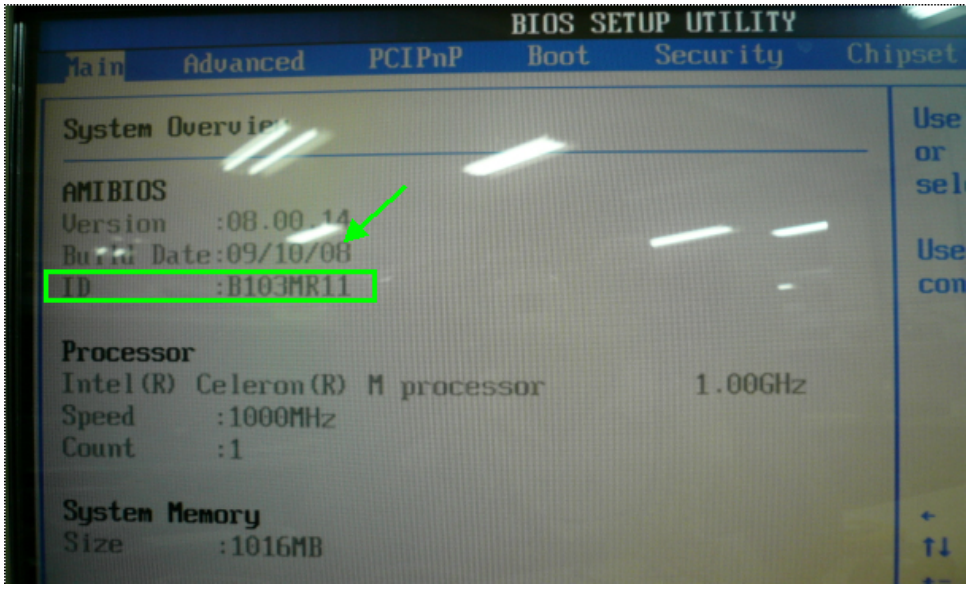


Figure 6-18: BIOS Main Menu – Updated BIOS Version (MR11)

6.7.2 Using DOS Command

To update BIOS in the DOS environment, prepare a USB flash drive that contains boot files and BIOS updating files shown in Figure 6-19 and follow the steps below to update BIOS.

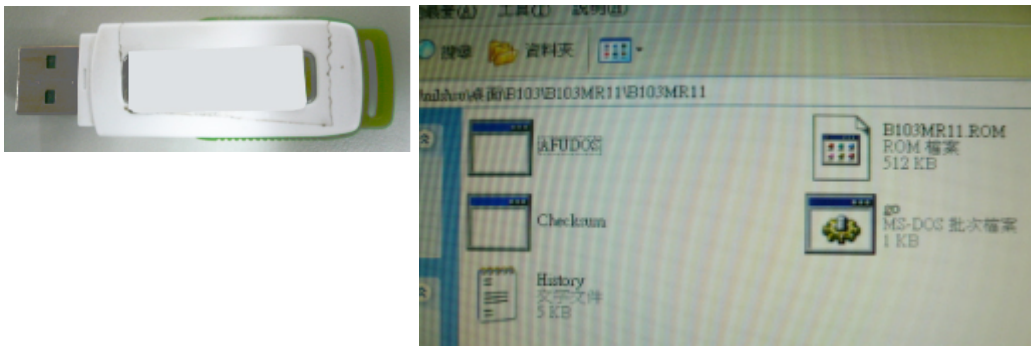


Figure 6-19: USB Flash Drive and BIOS Updating Files

Step 1: Connect the USB flash drive to the system. Boot-up the system into DOS. Input commands to get into the directory of the BIOS updating files (ex. cd (folder name)). See Figure 6-20.

Figure 6-20: BIOS Updating File Directory

Step 2: Input command **GO** and press Enter (Figure 6-21). The system starts updating BIOS.

Figure 6-21: GO Command

Step 3: Figure 6-22 shows the screen when the updating is completed.

Figure 6-22: BIOS Updating Complete (DOS)

Step 4: Restart the system and check the BIOS menu. The BIOS version has been changed to MR11 (Figure 6-23).

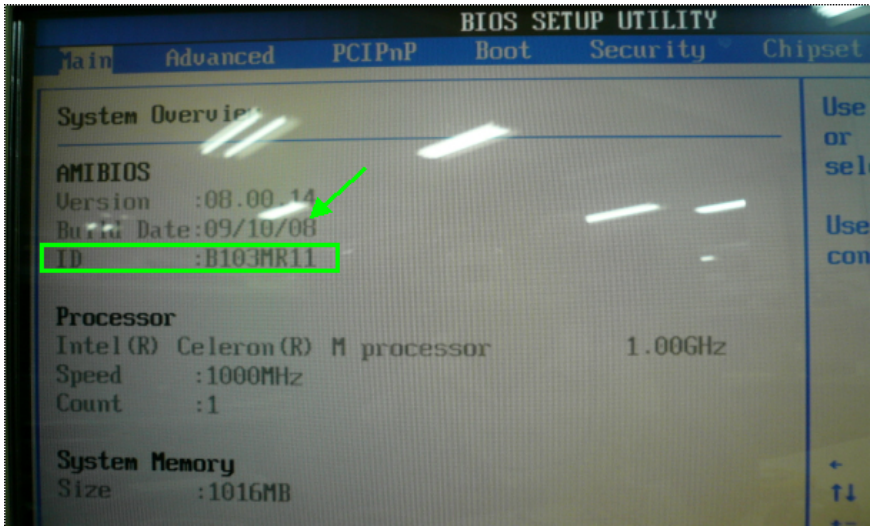


Figure 6-23: BIOS Main Menu – Updated BIOS Version (MR11)

A.1 RTC Overview

A Real-time clock (RTC) is a basic hardware device that keeps track of the current time of the computer. A RTC can be built in a chip or embedded in the system. When the computer is turned off, the battery on the motherboard provides power to the RTC to keep track of the current time. The RTC is usually used in personal computers and embedded systems.

A.1.1 How to Calculate the Battery Life

The RTC requires an external battery connection to maintain functionality and its RAM while the south bridge is not powered by the system.

The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh(assumed usable)and the average current required is 6 μA, the battery life will be at least:

170,000μAh / 6 μA=28,333 h=3.2 years

The voltage oh the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases.

Appendix

C

Reference Carrier Board Schematic

Cover Page

PCI ROUTING

IDSEL	PREQ#	PGNT#	INT#	DEVICE
AD23	0	0	D,A,B,C	Mini PCI
AD22	3	3	C,D,A,B	PCISA SLOT3
AD21	2	2	B,C,D,A	PCISA SLOT2
AD20	1	1	A,B,C,D	PCISA SLOT1

Value Rule

@: Didn't install component.

P/N:Part_Number.

R: R_Package_(Precision) ; Package 4=0402, 6=0603, 8=0805, 12=1206, 1210=1210

L: L_Package_Current ; Package 4=0402, 6=0603, 8=0805, 12=1206, 1210=1210, DIP13.5X12, DIP16X8

C: C_Package_Material_Voltage ;
Package 4=0402, 6=0603, 8=0805, 12=1206, 1210=1210, DIP8=DIP phi=8, DIP10=DIP phi=10;
Material Y=Y5V, X=X7R, N=NPO, OS=OS CON, SP=SP CAP, POS=POS CAP, EC=EC CAP;
Voltage 6V3=6.3V..

D: D_Package_(Others) ; Package=SOT23...

Q: Q_Package_(Others) ; Package=SOT23, TO252, TO263, TO223, SO8

U: U_Package_(Others) ; Package=SSOP20, PQFP128, SO14...

X: X_Package_(Others)

CN: CN function_Pin Count_Pin Pitch_(Others) ;
HEADER_2X6_2.54, ATX12V_2X2_4, DDRII_240_2

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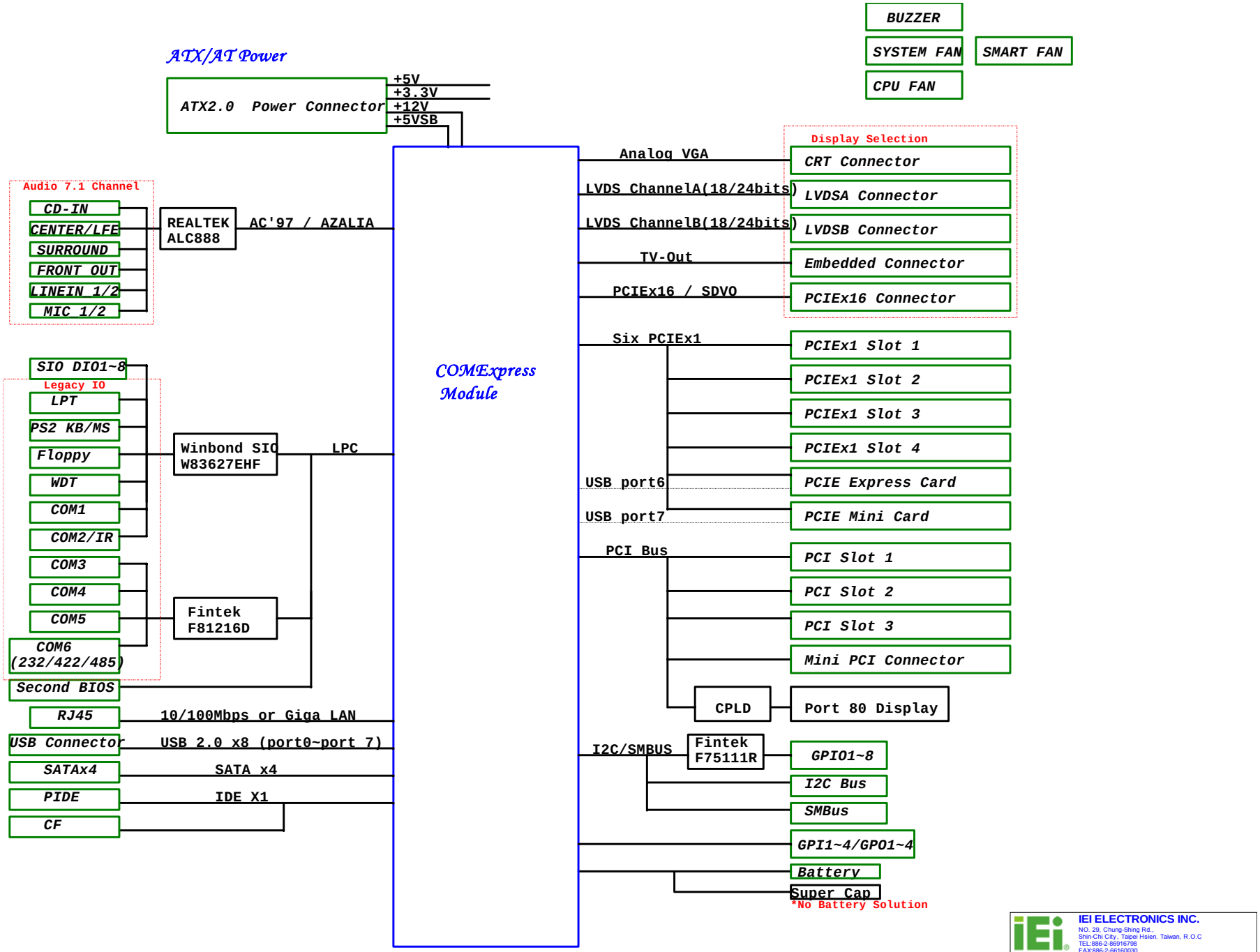

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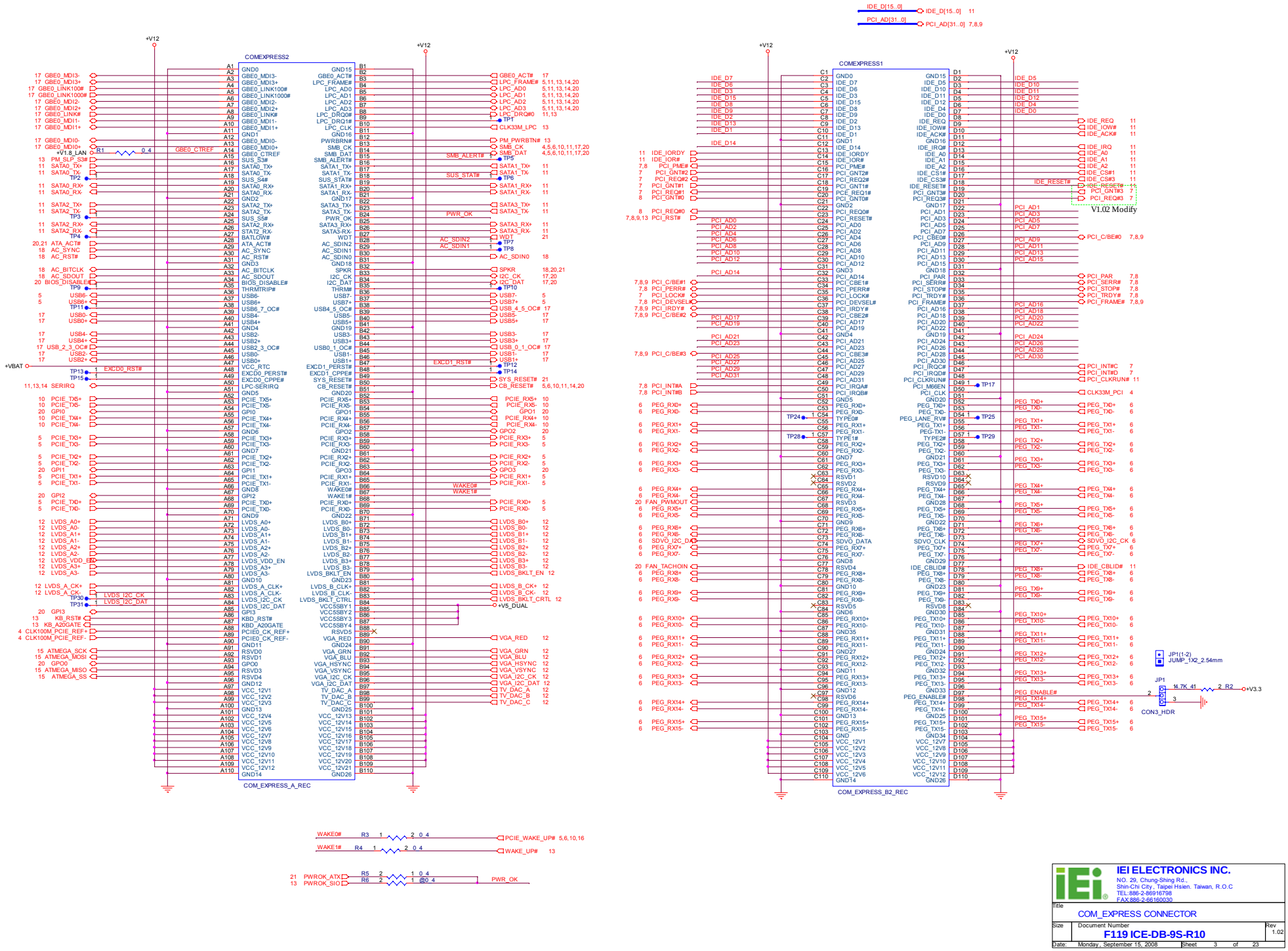

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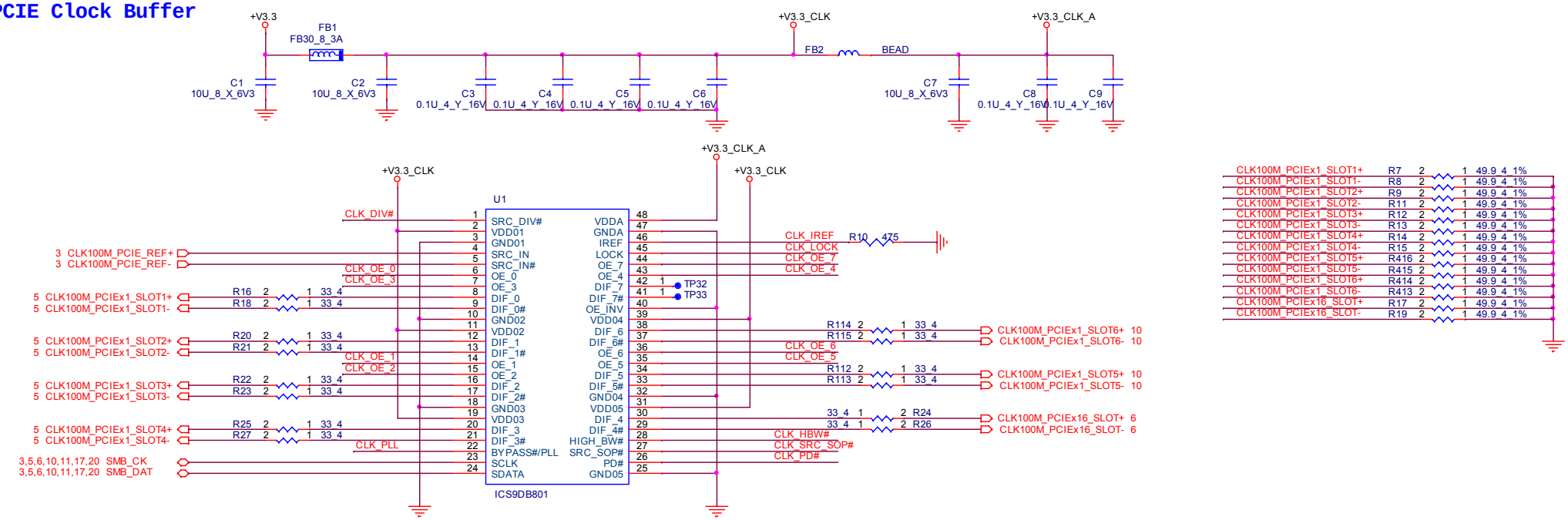
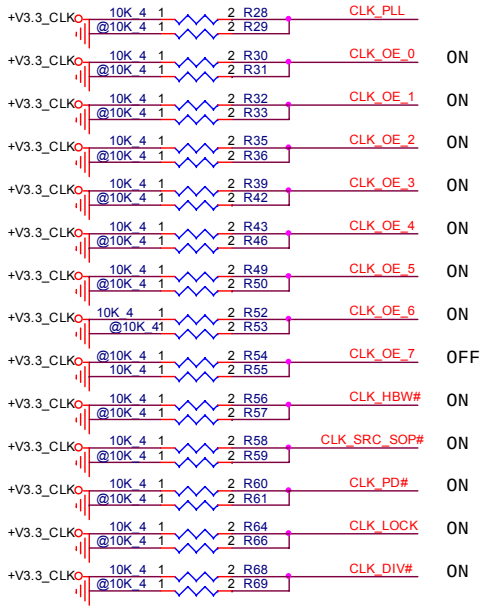
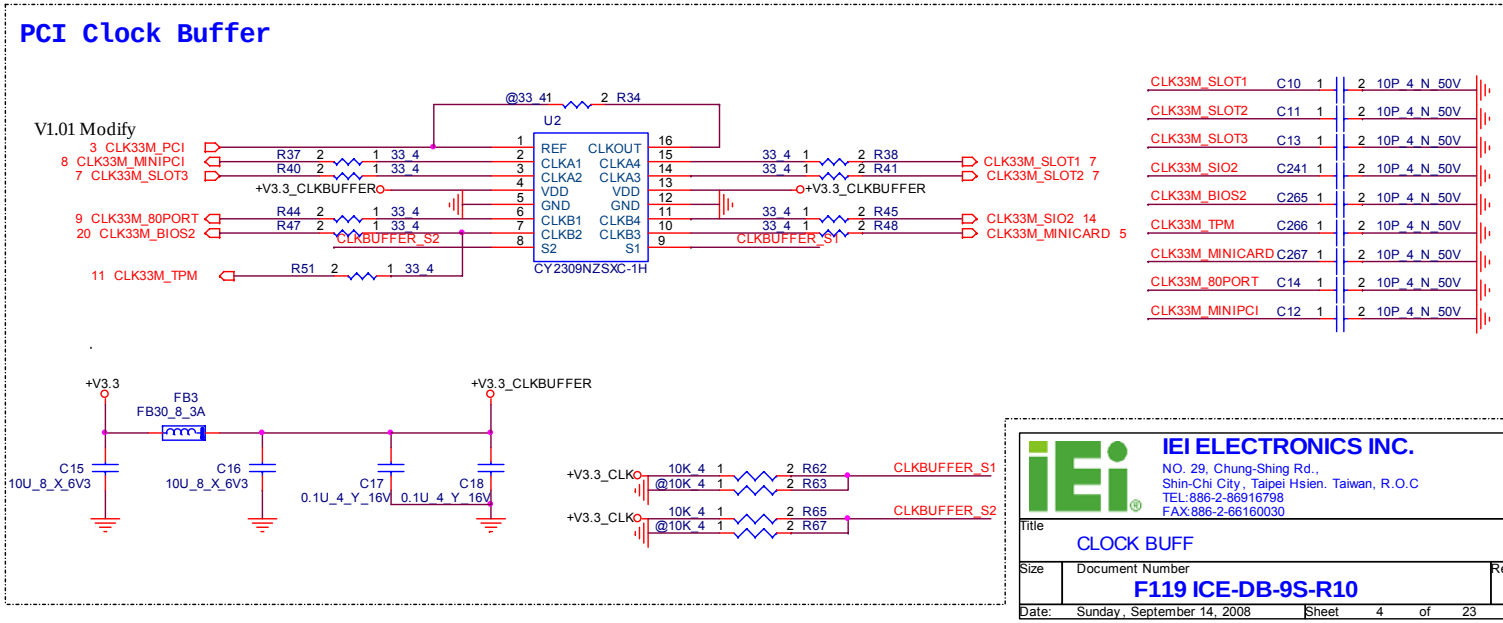
PCIE Clock Buffer





PCI Clock Buffer



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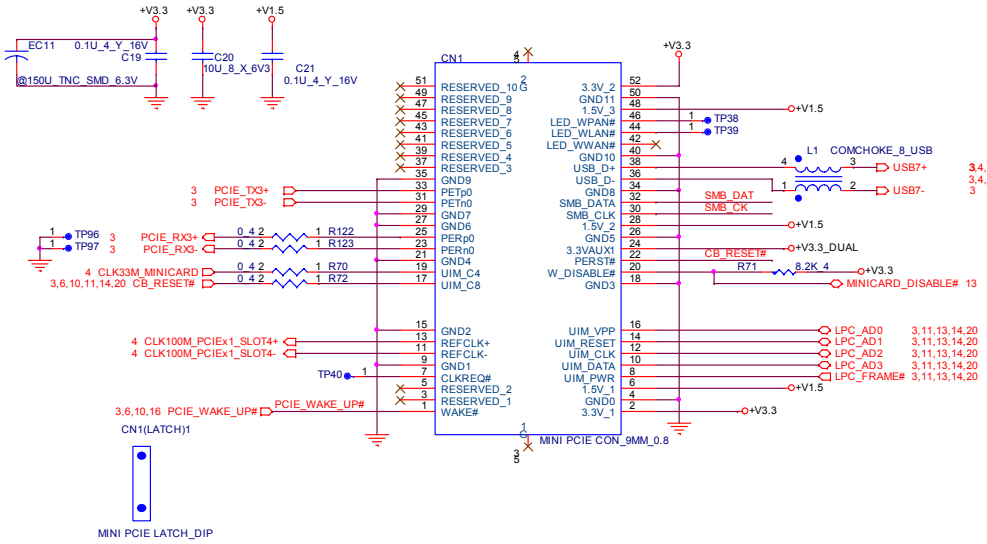
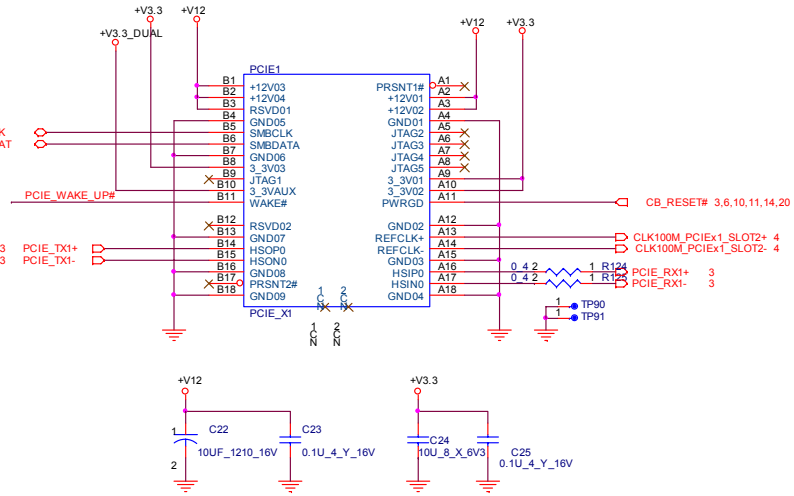
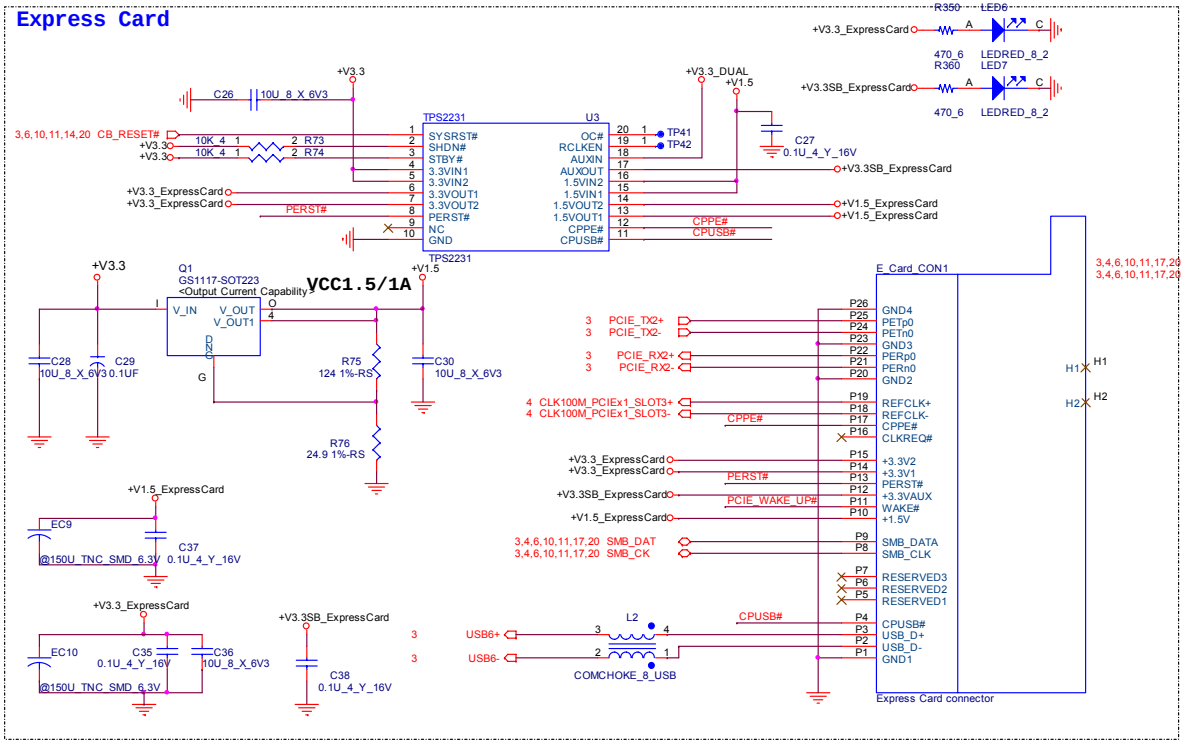
Mini PCI Express



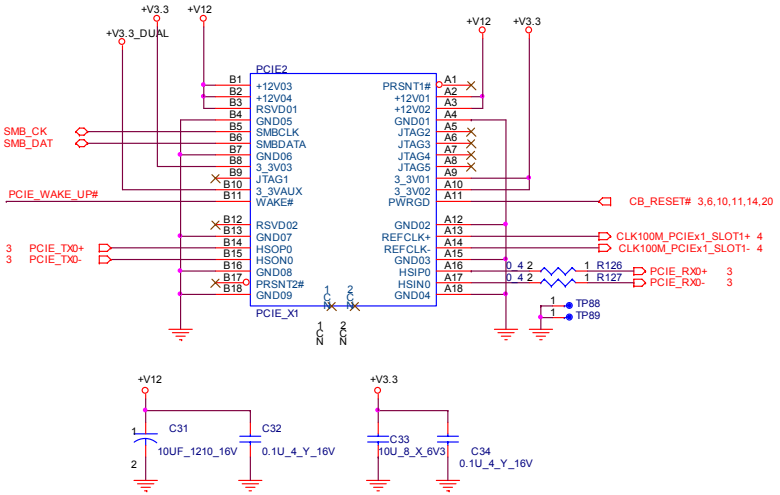
PCIEX1_Slot1



Express Card



PCIEX1_Slot2



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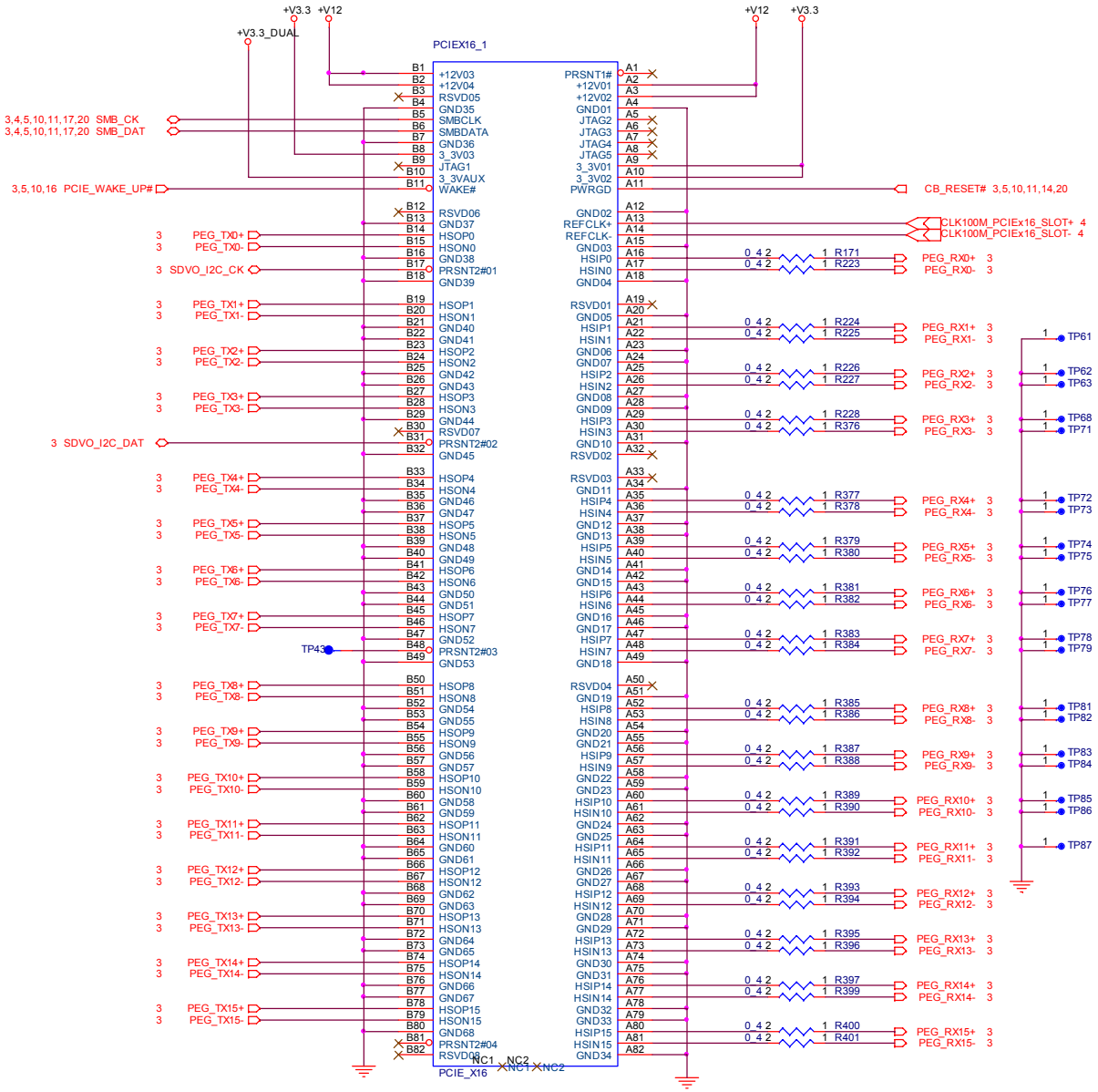
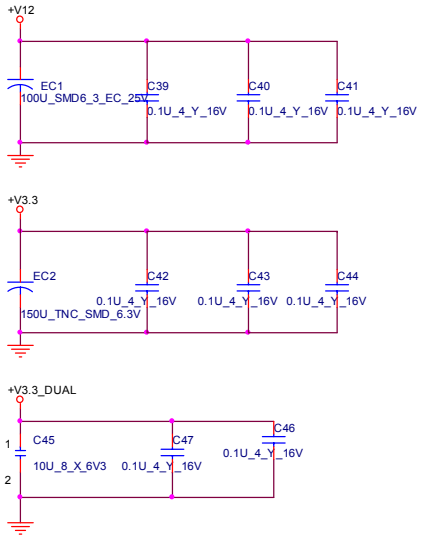
TEL:886-2-86916798
FAX:886-2-66160030

Title	PCIEX1/Express & Mini Card	
Size	Document Number F119 ICE-DB-9S-R10	Rev 1.02
Date: Sunday, September 14, 2008	Sheet 5 of 23	





V1.01 Modify

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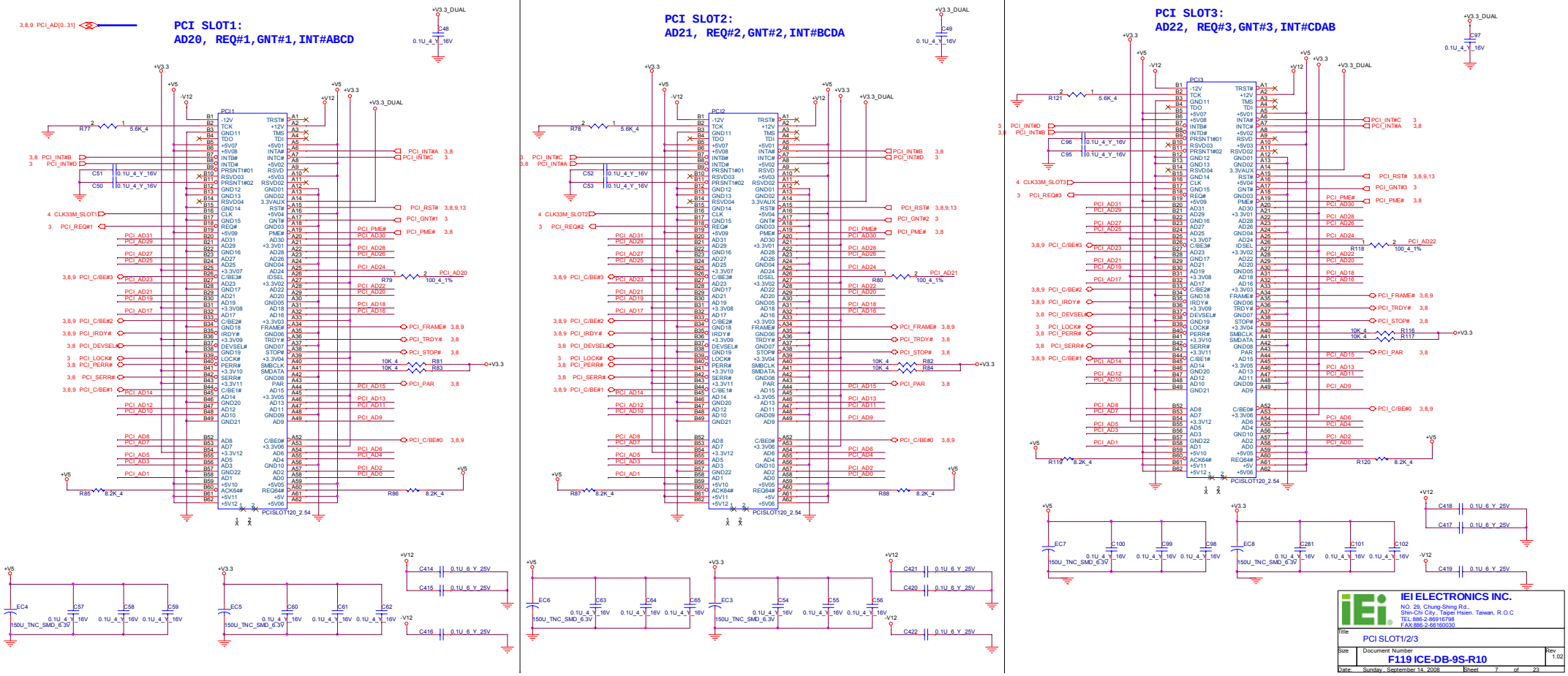
Title: PCIEx16		
Size	Document Number: F119 ICE-DB-9S-R10	Rev: 1.02
Date: Sunday, September 14, 2008	Sheet 6 of 23	


PCI SLOT1:
AD20, REQ#1,GNT#1,INT#ABCD
PCI SLOT2:
AD21, REQ#2,GNT#2,INT#BCDA
PCI SLOT3:
AD22, REQ#3,GNT#3,INT#CDAB
PCISLOT120_2.54
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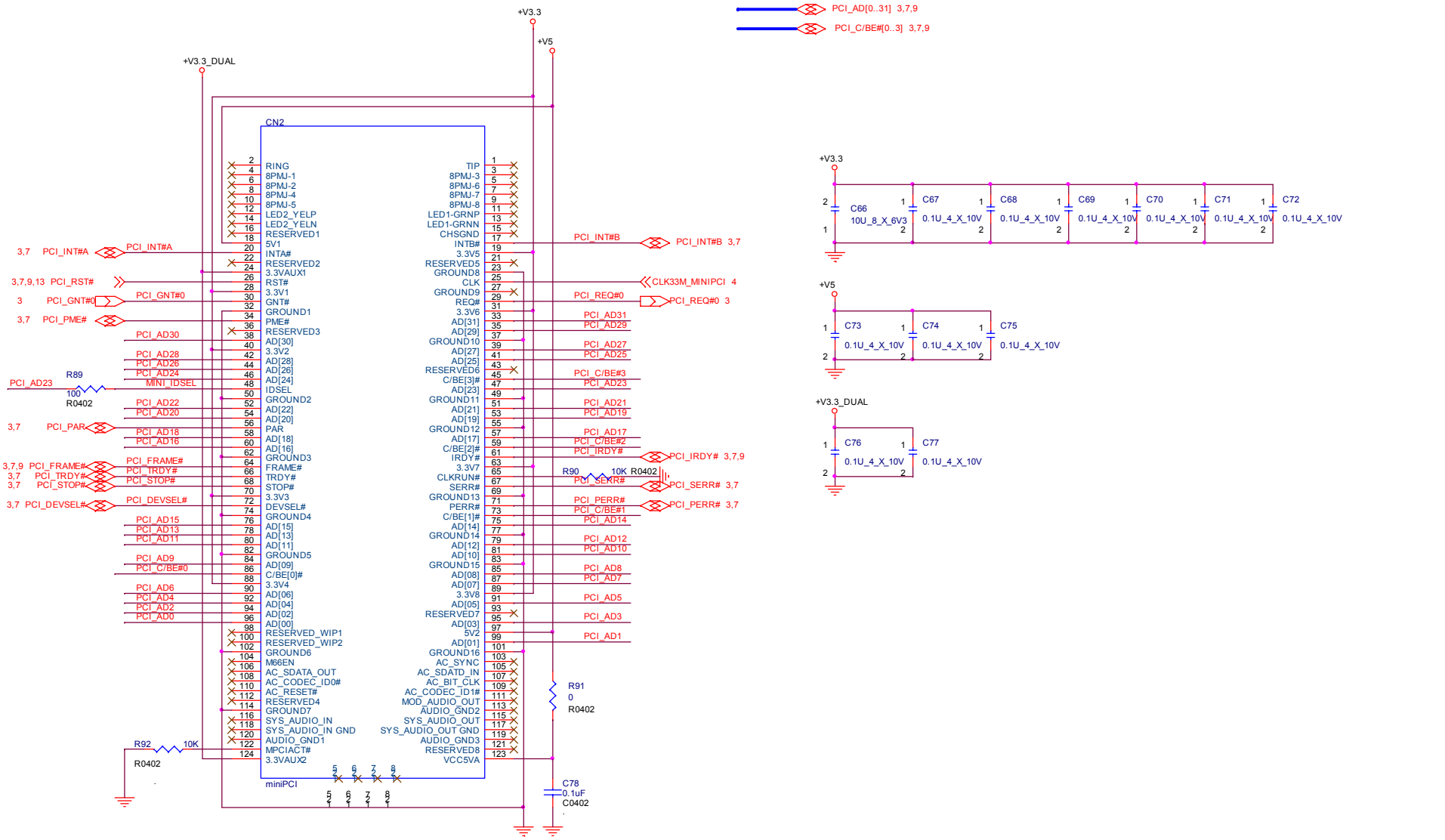
FAX:886-2-66160030
PCI SLOT1/2/3
F119 ICE-DB-9S-R10
Sunday, September 14, 2008
7
23

MiniPCI:
AD23, REQ#0,GNT#0,INT#AB



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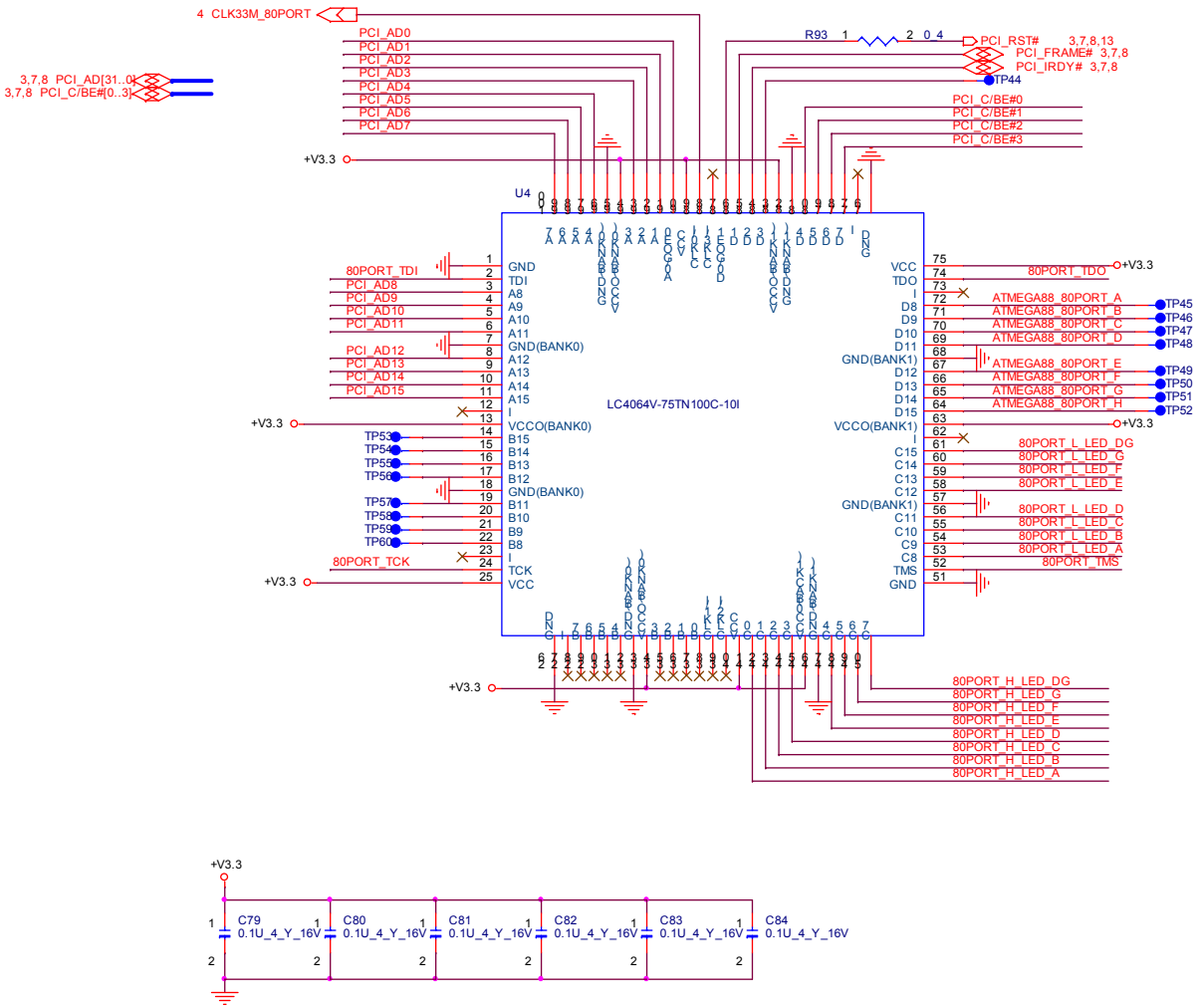
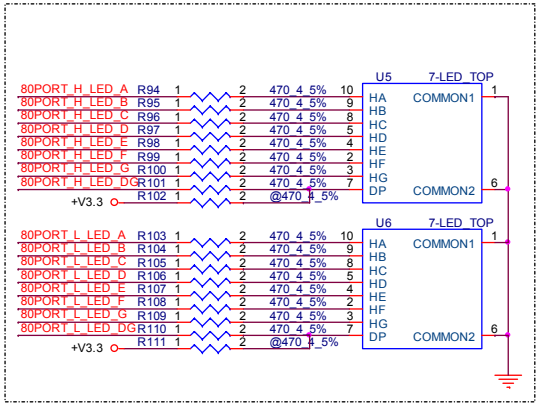
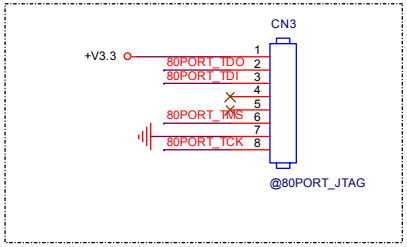
Title	MINI-PCI	
Size	Document Number: F119 ICE-DB-9S-R10	Rev 1.02
Date: Sunday, September 14, 2008	Sheet 8 of 23	



7-Segment LED with Common GND



Debug 80 Programimg Port(Reserve)



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Title	PCI 80 PORT	
Size	Document Number: F119 ICE-DB-9S-R10	Rev 1.02
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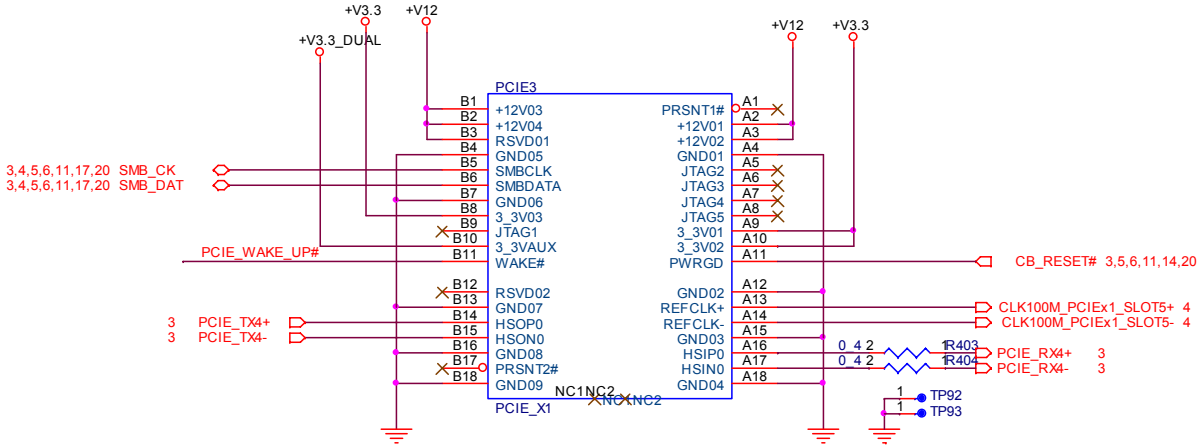
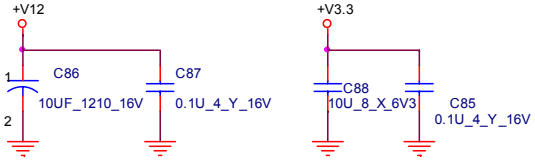
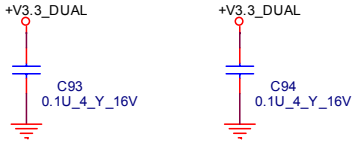
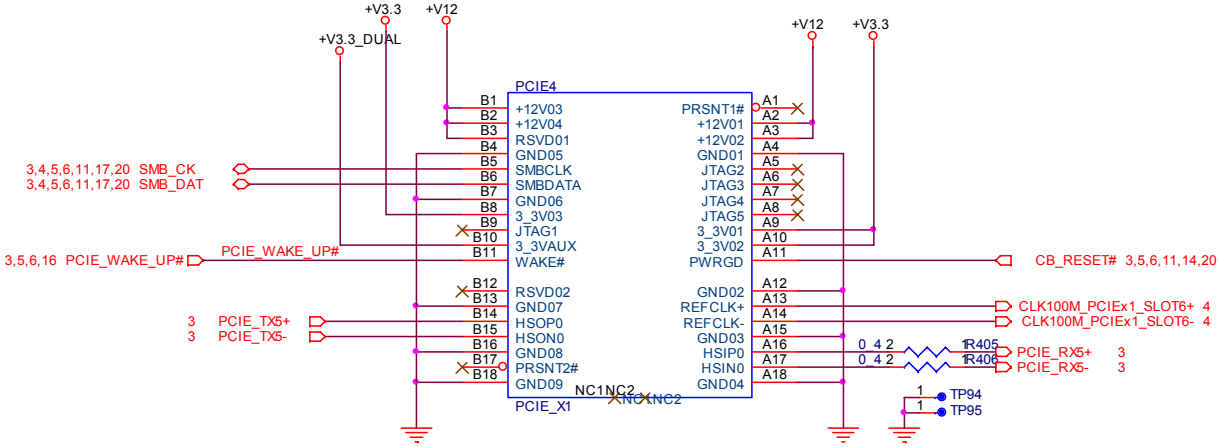
PCIEX1_Slot3

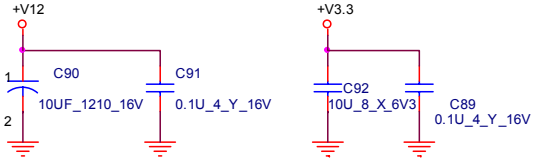






PCIEX1_Slot4





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Title: PCI ExpressX1 Slot3/4		
Size	Document Number: F119 ICE-DB-9S-R10	Rev: 1.02
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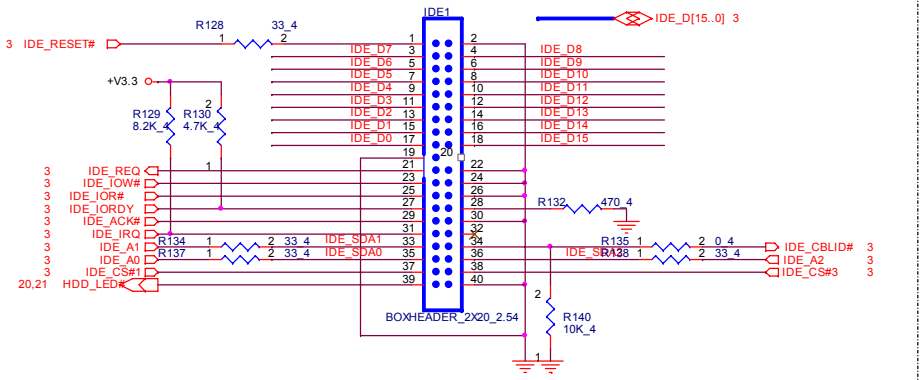
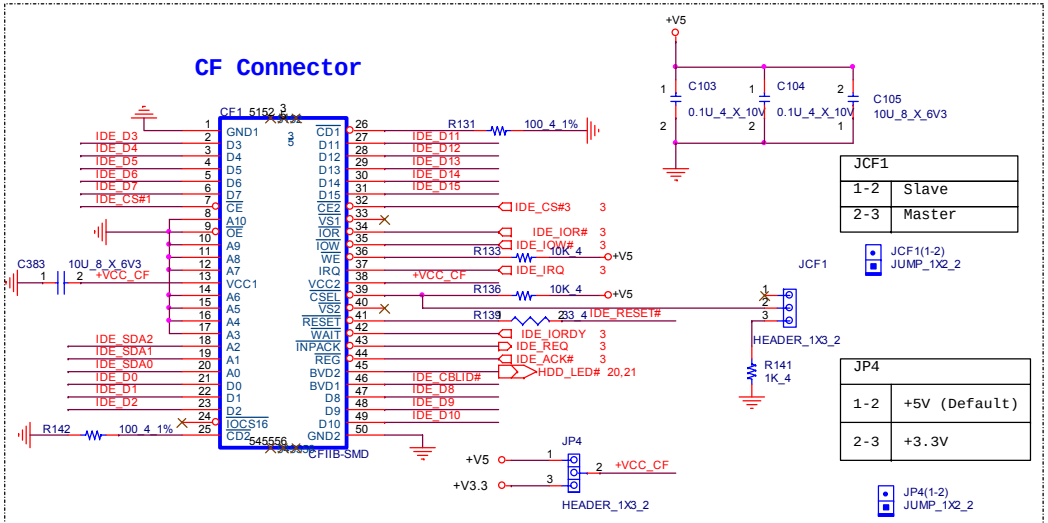
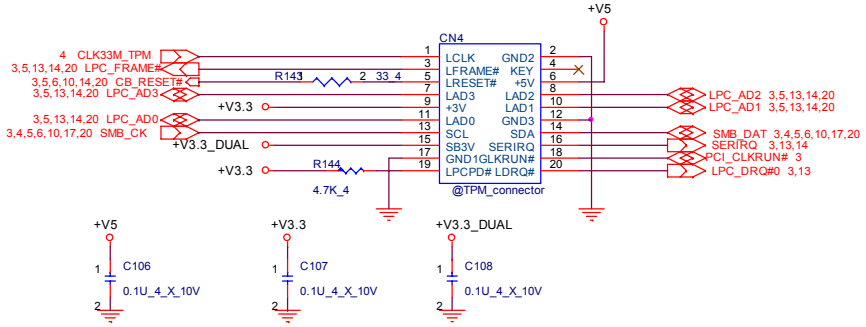
IDE Connector



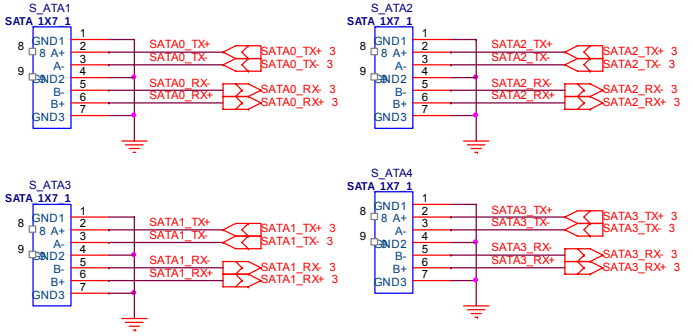
CF Connector



TPM Connector



SATA Connector



Title	IDE,SATA,TPM CF CONN
Size	Document Number: F119 ICE-DB-9S-R10
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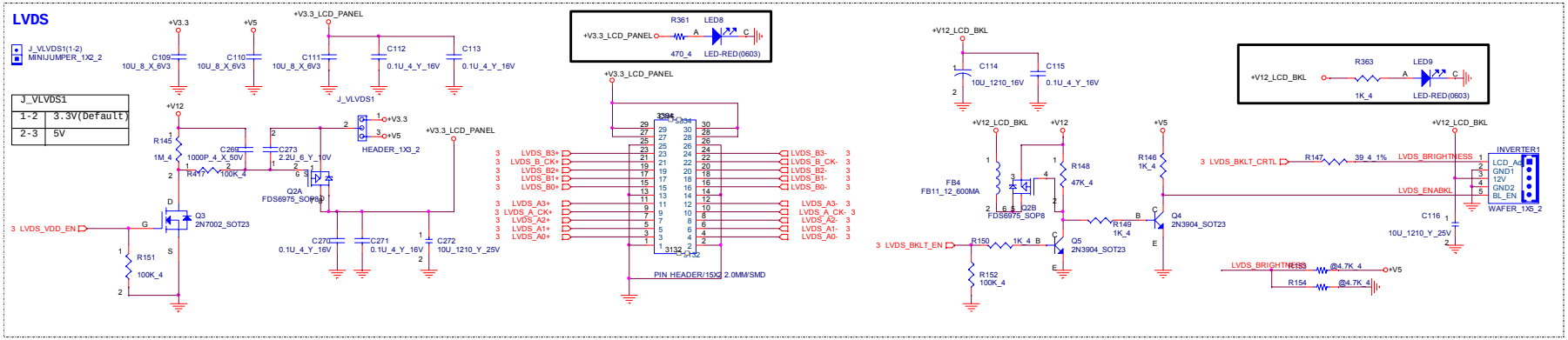
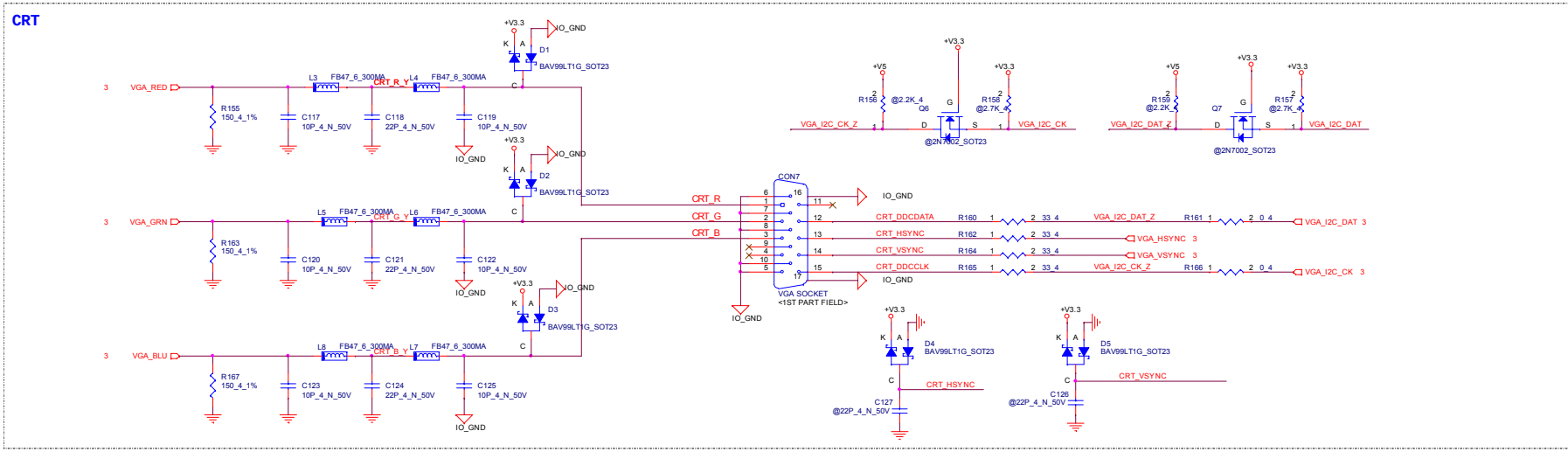
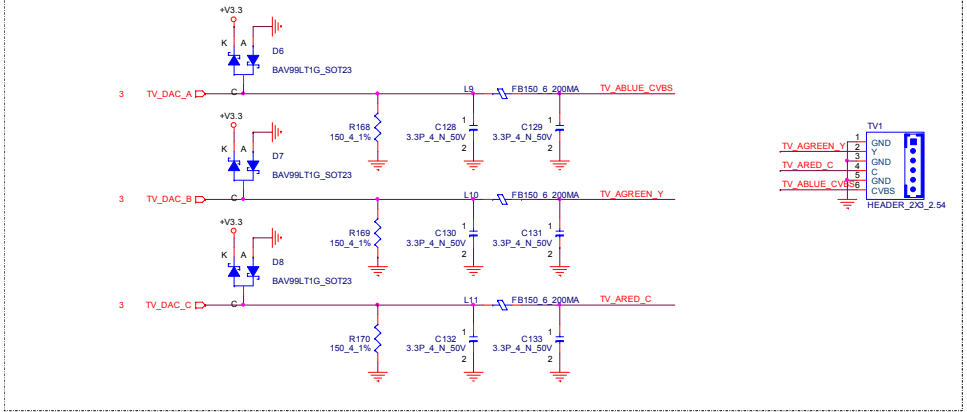
LVDS



CRT



TV-OUT



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Title	LVDS/TV/CRT	
Size	Document Number	Rev
	F119 ICE-DB-9S-R10	1.02
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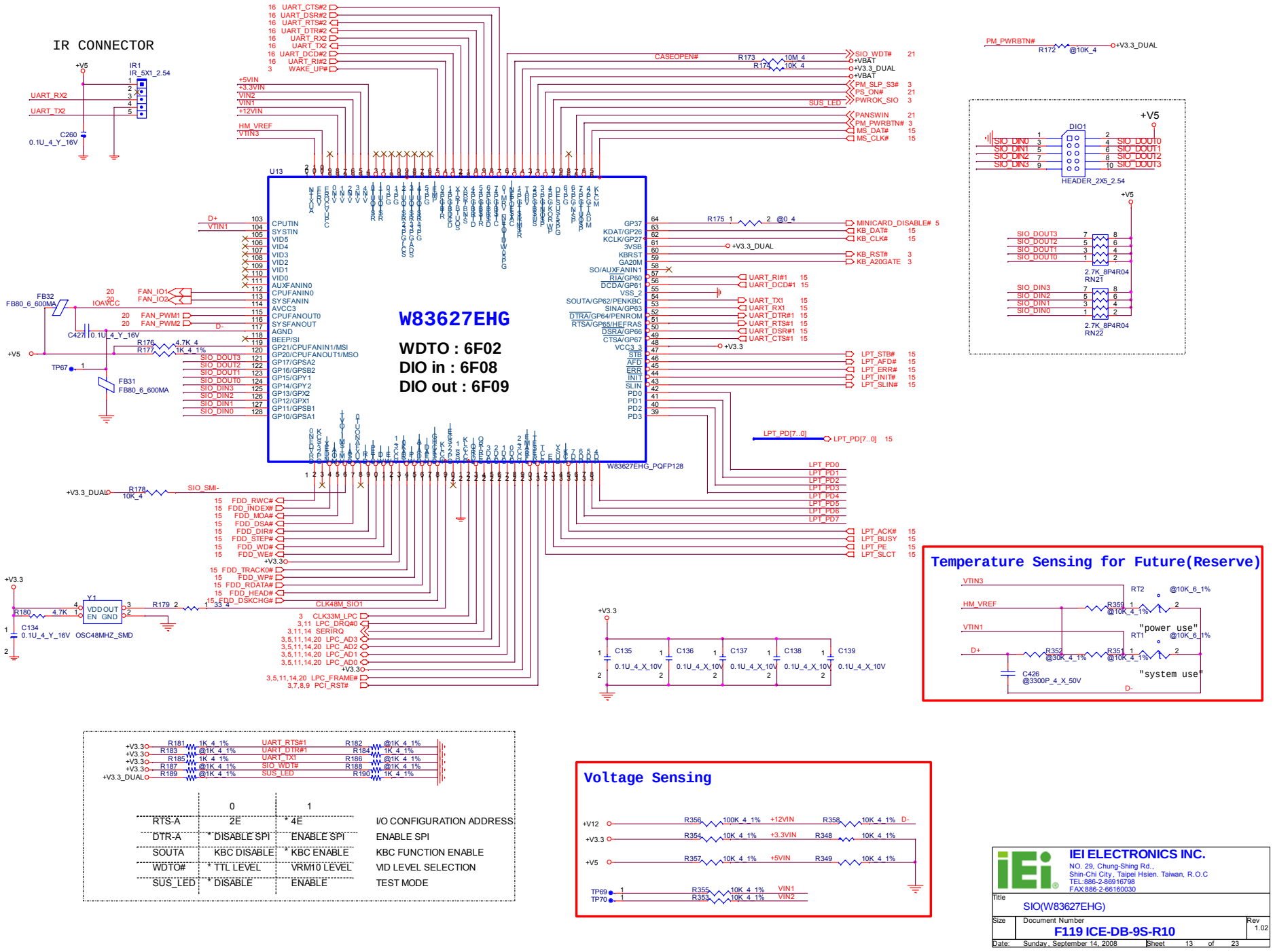

	0	1	
RTS-A	2E	* 4E	I/O CONFIGURATION ADDRESS
DTR-A	* DISABLE SPI	ENABLE SPI	ENABLE SPI
SOUTA	KBC DISABLE	* KBC ENABLE	KBC FUNCTION ENABLE
WDTO#	* TTL LEVEL	VRM10 LEVEL	VID LEVEL SELECTION
SUS_LED	* DISABLE	ENABLE	TEST MODE

Title	SIO(W83627EHG)
Size	Document Number: F119 ICE-DB-9S-R10
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Date:	Sunday, September 14, 2008
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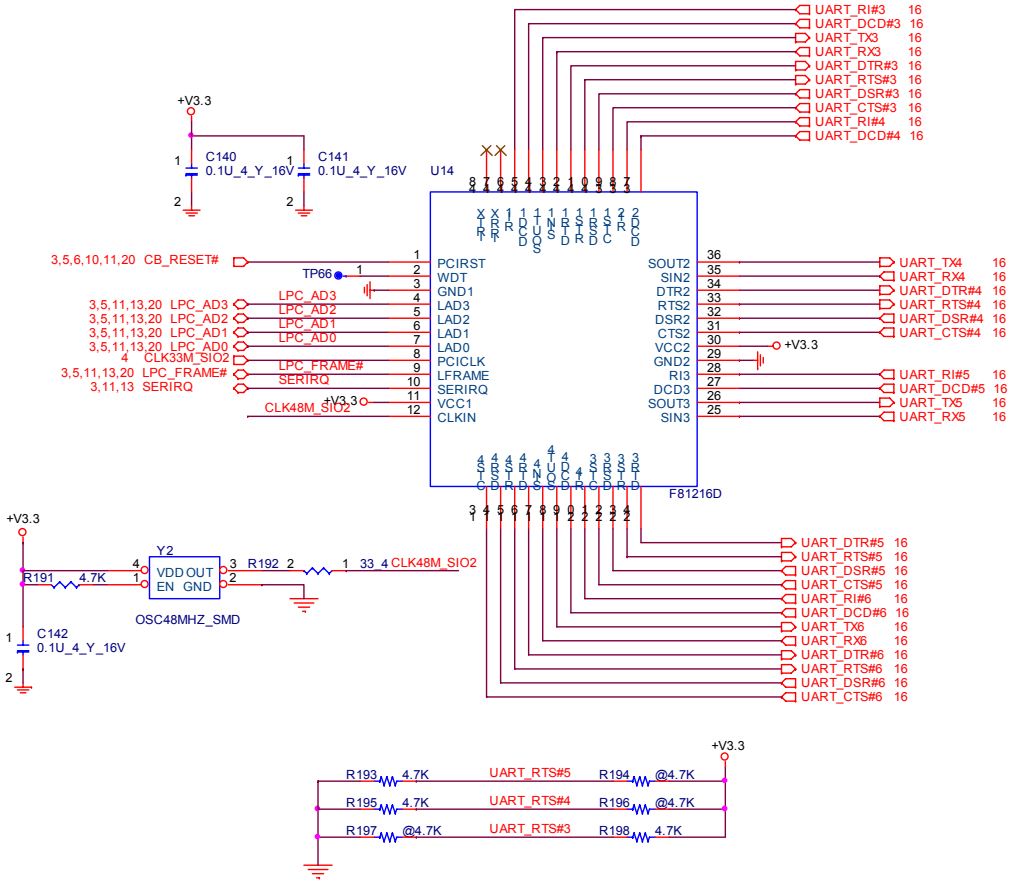
Default Address: 2E/2F, Entry Key=0X77



F81216_PIN18	ON: UART 4 Addr:0x2e8 IRQ9 OFF :UART 4 Disabled
F81216_PIN26	ON: UART 3 Addr:0x3e8 IRQ5 OFF :UART 3 Disabled
F81216_PIN34 F81216_PIN36	(X,ON) : UART 2 Addr:0x2f8 IRQ4 (ON,OFF): UART 2 Addr:0x2e0 IRQ4 (OFF,OFF):UART 2 disabled.
F81216_PIN42 F81216_PIN44	(X,ON) : UART 1 Addr:0x3f8 IRQ3 (ON,OFF): UART 1 Addr:0x3e0 IRQ3 (OFF,OFF):UART 1 disabled.
F81216_PIN24	ON: Watch Dog Timer enabled and setting to 10 second when the clock input is 24Mhz. If the clock input is 48Mhz , the timer is setting to 5 second. OFF :disabled.

PIN33	PIN23	PIN41	Address	Entry Key
0	0	0	0x4E/0x4F	0x77
0	0	1	0x2E/0x2F	0x77(D)
0	1	0	0x4e/0x4f	0xa0
0	1	1	0x2E/0x2F	0xa0
1	0	0	0x4E/0x4F	0x87
1	0	1	0x2E/0x2F	0x87
1	1	0	0x4e/0x4f	0x67
1	1	1	0x2E/0x2F	0x67

ON:1
OFF:0
D:default

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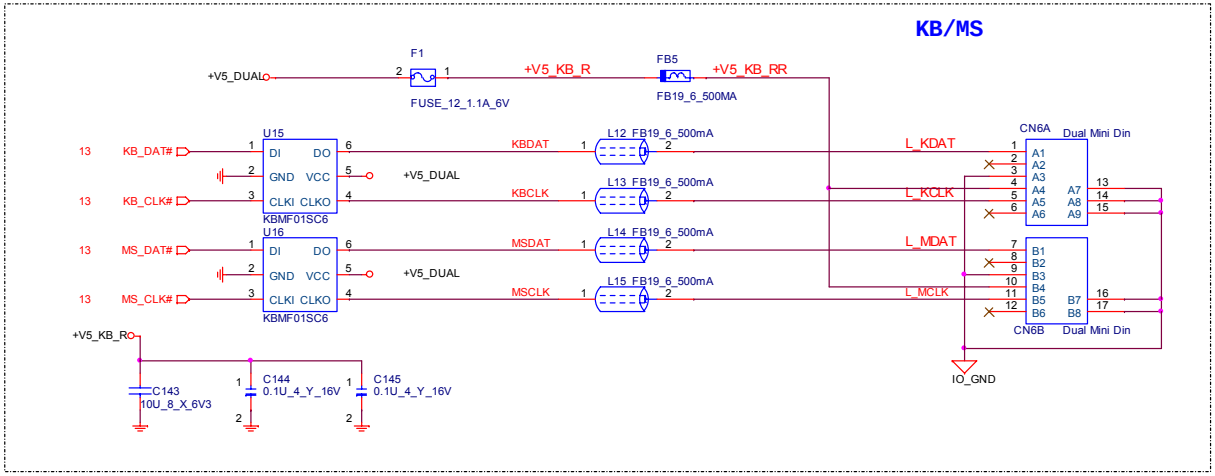
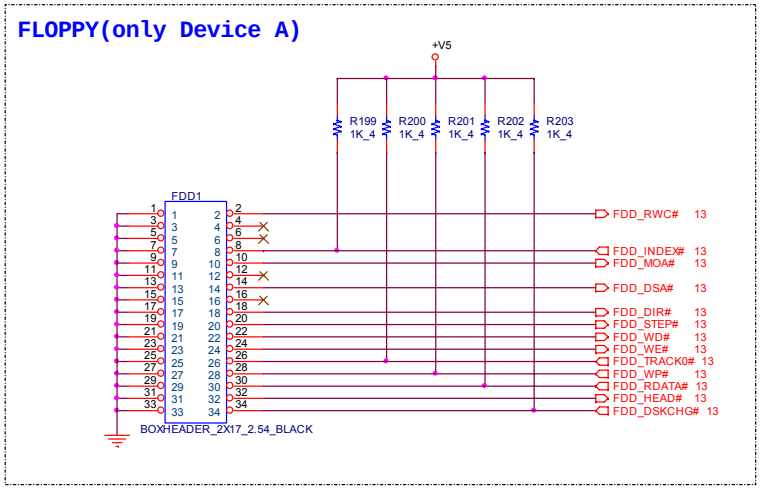
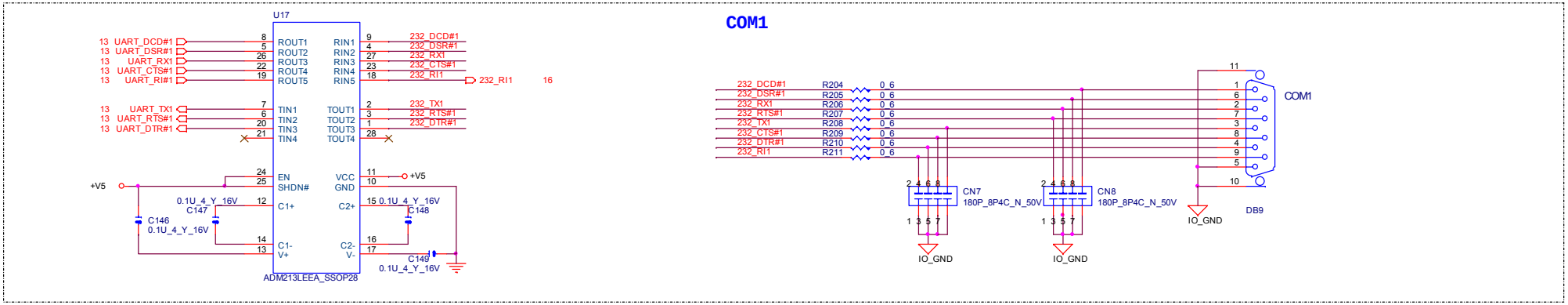
Title: SIO(F81216D)

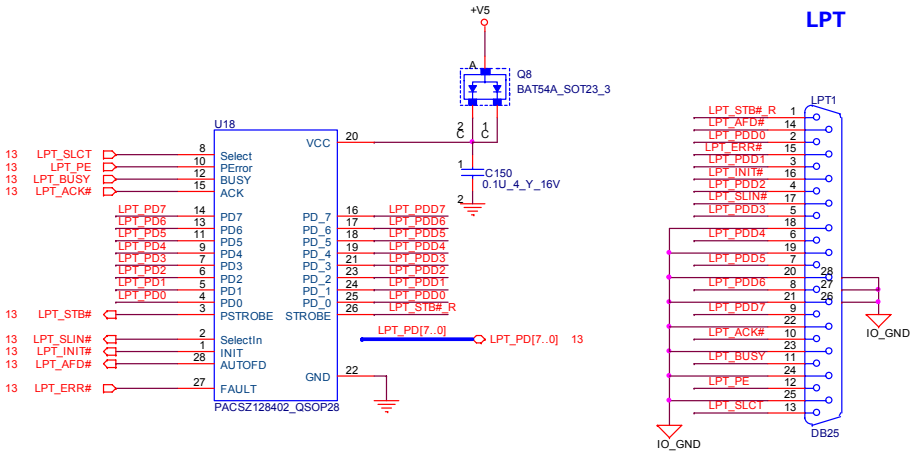
Size | Document Number: F119 ICE-DB-9S-R10 | Rev: 1.02

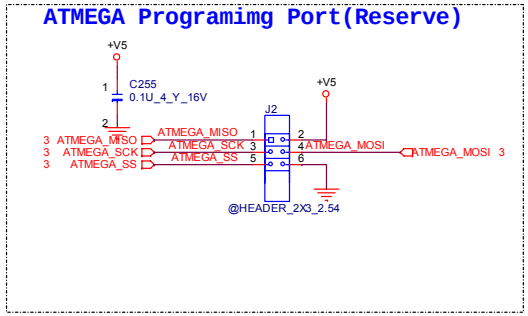
Date: Sunday, September 14, 2008 | Sheet 14 of 23











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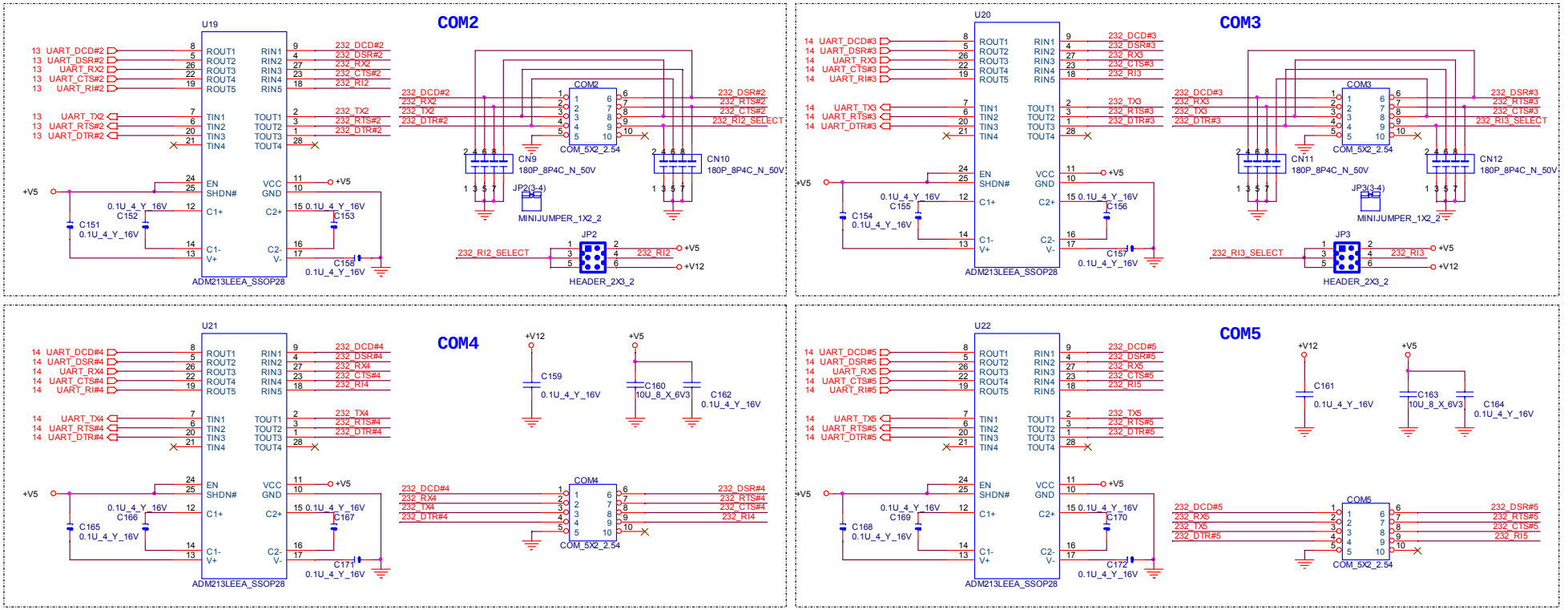
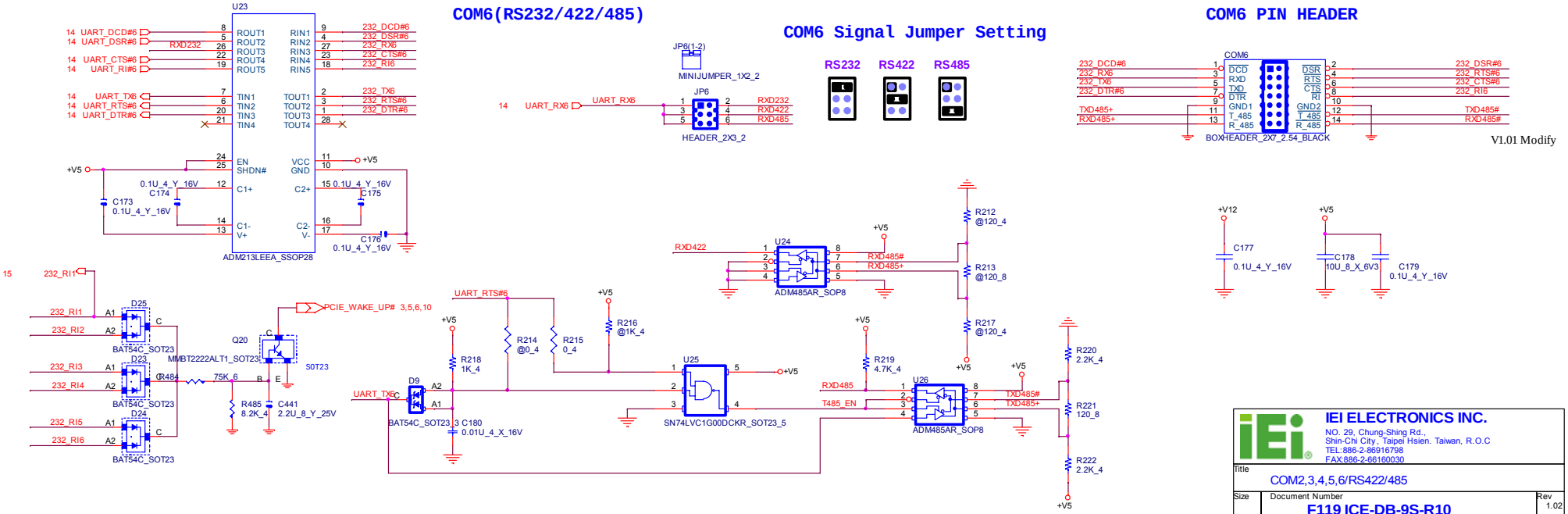
TEL:886-2-86916798 FAX:886-2-66160030		
Title: LPT,FLOPPY,KB/MS,COM1		
Size	Document Number: F119 ICE-DB-9S-R10	Rev: 1.02
Date: Sunday, September 14, 2008	Sheet 15 of 23	





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TEL:886-2-86916798		
FAX:886-2-66160030		
Title	COM2,3,4,5,6/RS422/485	
Size	Document Number	Rev
	F119 ICE-DB-9S-R10	1.02
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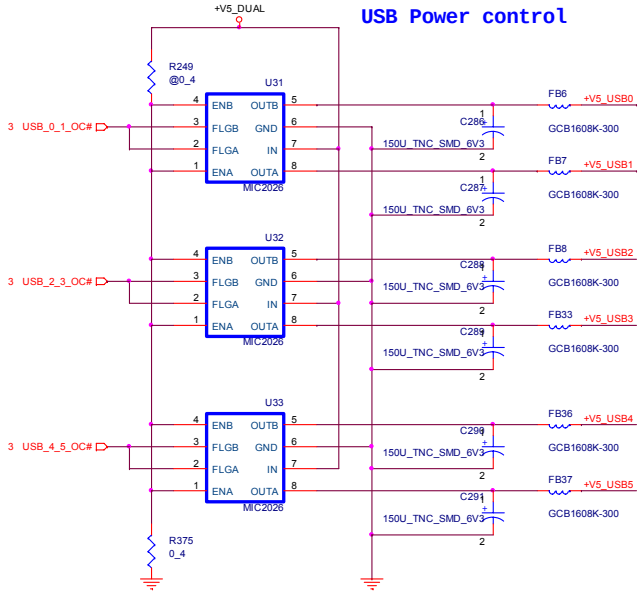

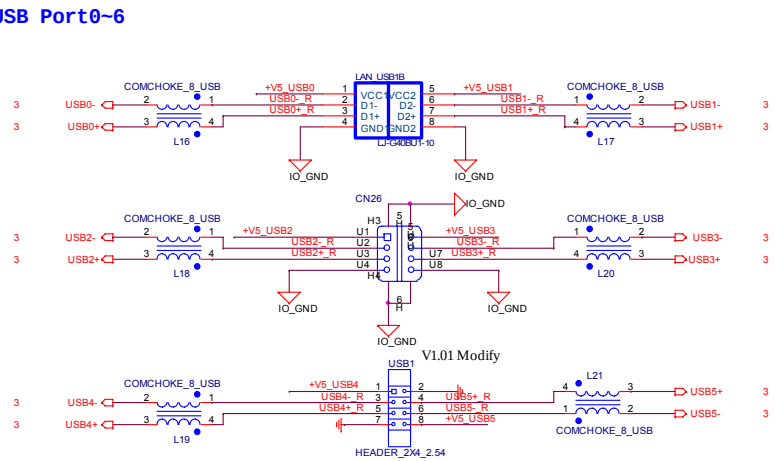

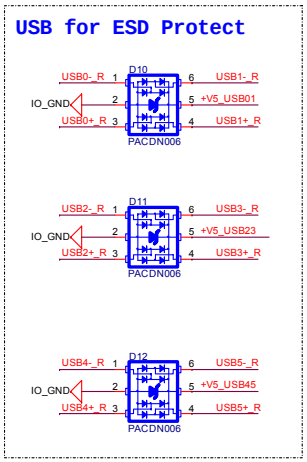

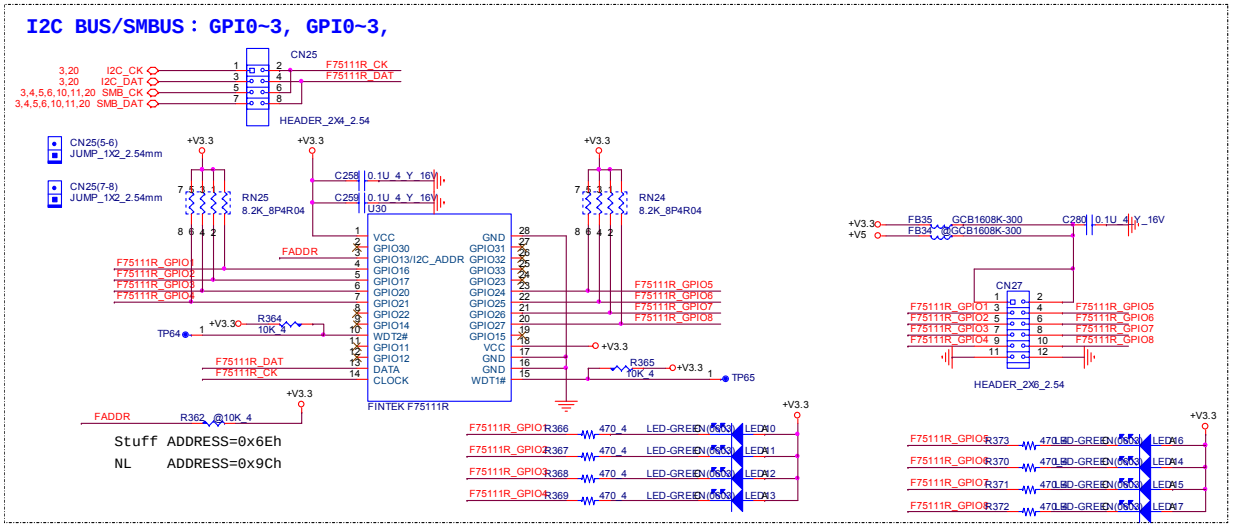

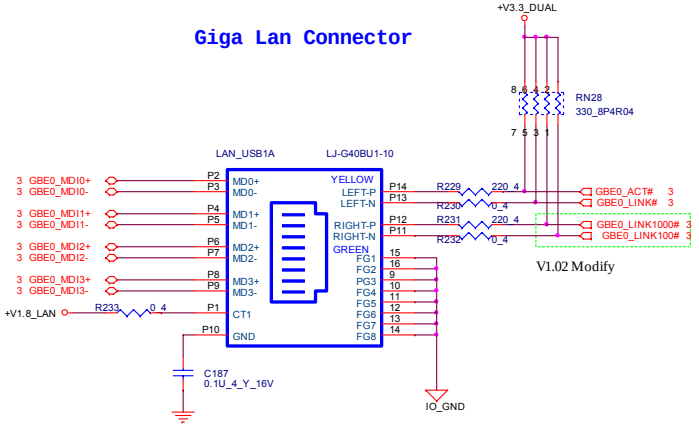

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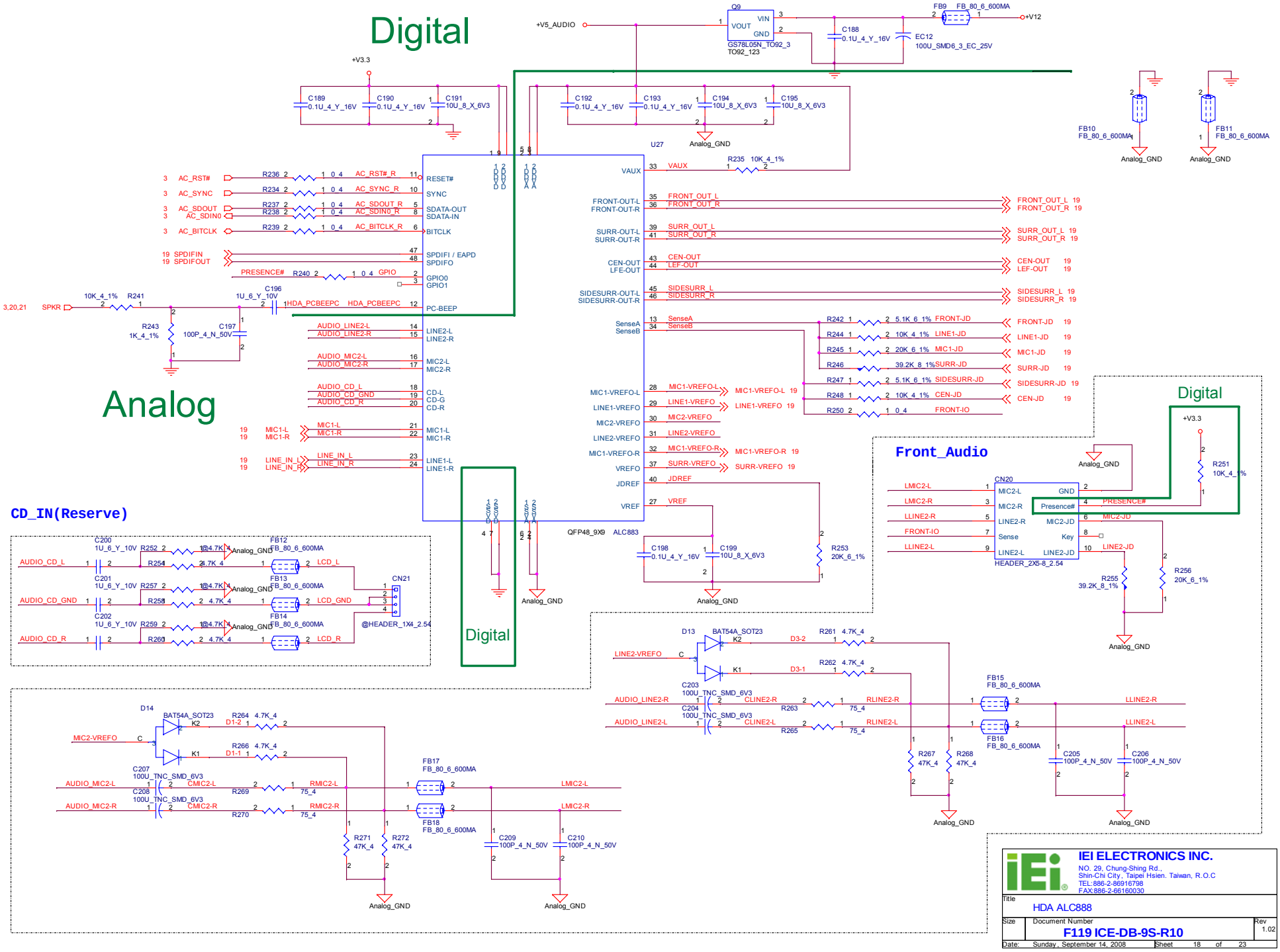
TEL:886-2-86916798 FAX:886-2-66160030			
Title	LAN,USB01,2,3,4,5,I2C GPIO		
Size	Document Number		Rev
	F119 ICE-DB-9S-R10		1.02
Date: Monday, September 15, 2008	Sheet 17 of 23		


Digital
Analog
Digital
Front_Audio
CD_IN(Reserve)
U27
ALC883
QFP48_9X9
IEI ELECTRONICS INC.
NO. 29, Chung-Shing Rd.,
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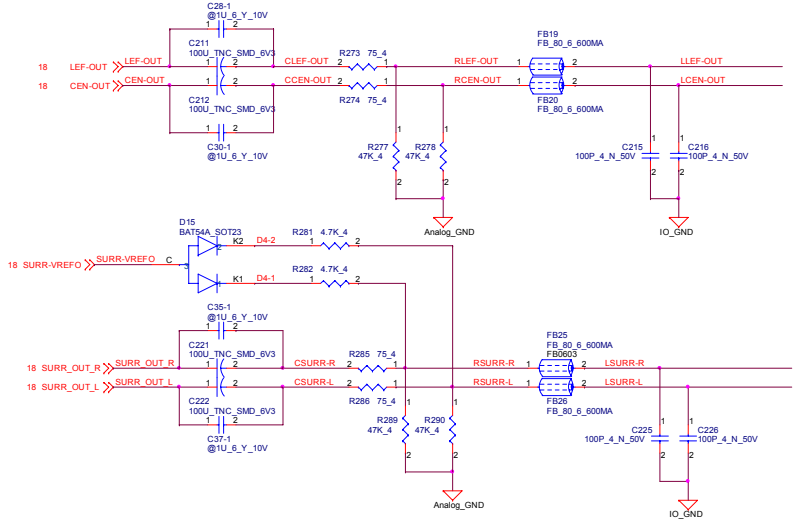
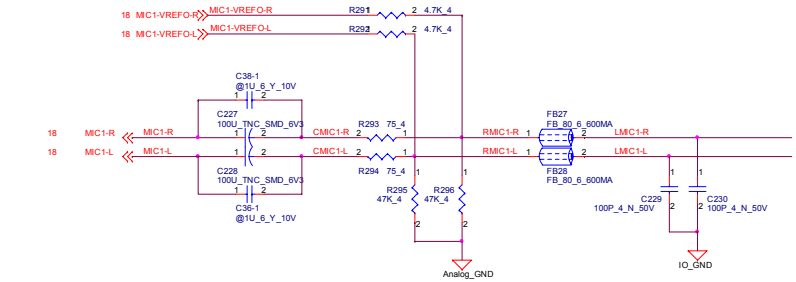
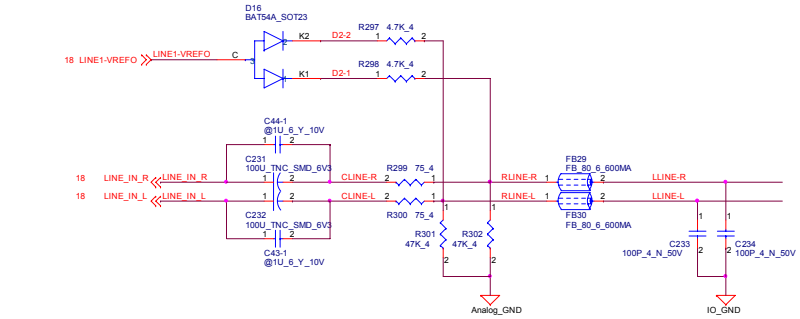
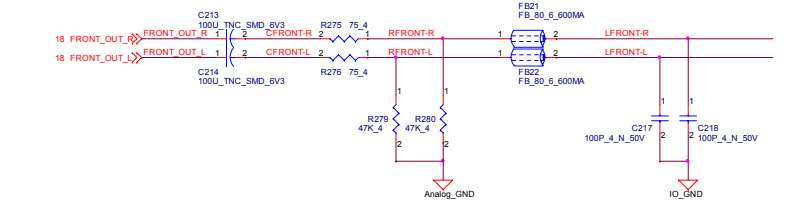
TEL:886-2-86916798
FAX:886-2-66160030
Title
HDA ALC888
Size
Document Number
F119 ICE-DB-9S-R10
Rev
1.02
Date: Sunday, September 14, 2008
Sheet 18 of 23

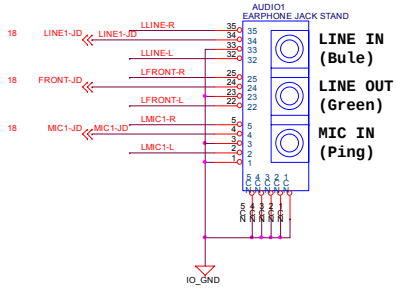








Audio Rear Jack

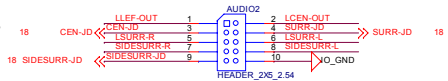


LINE IN (Bule)

LINE OUT (Green)

MIC IN (Ping)

Audio Rear Header



CEN/LFE OUT (Orange)

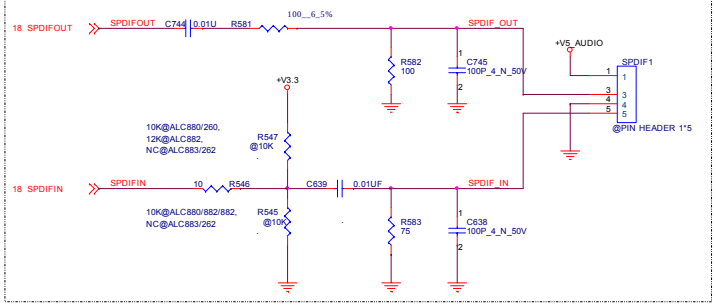
SURR. OUT (Black)

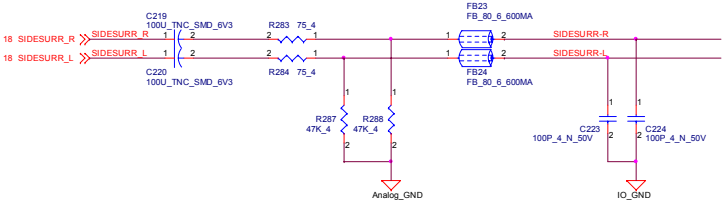
SIDE OUT (Gray)

Desktop Configuation 1: (7.1 Channel Solution)
Rear Panel: 6 jacks have specific functionality
Front Panel: 2 jacks are Universal Audio Jack

Pin Assignment	Location	FUNCTION
FRONT(pin-35/36)	Back Panel	Front line out w/ ampifier,Line_in
SURR (pin-39/41)	Back Panel	Surround line out, Line_in
CEN/LFE (pin-43/44)	Back Panel	Center/Lft line out,Line_in
SIDESURR (pin-45/46)	Back Panel	Side surround line out,Line_in
LINE1 (pin-23/24)	Back Panel	Line in / Shared surround out
MIC1 (pin-21/22)	Back Panel	Mic in / Shared Center-Lft out/Line_in
LINE2 (pin-14/15)	Front Panel	Headphone out/ line in/ mic in
MIC2 (pin-16/17)	Front Panel	Mic in/ Headphone out / line in

SPDIF Connector(Reserve)





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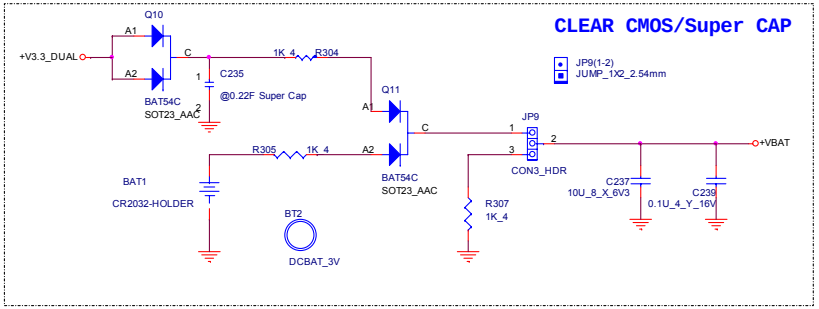

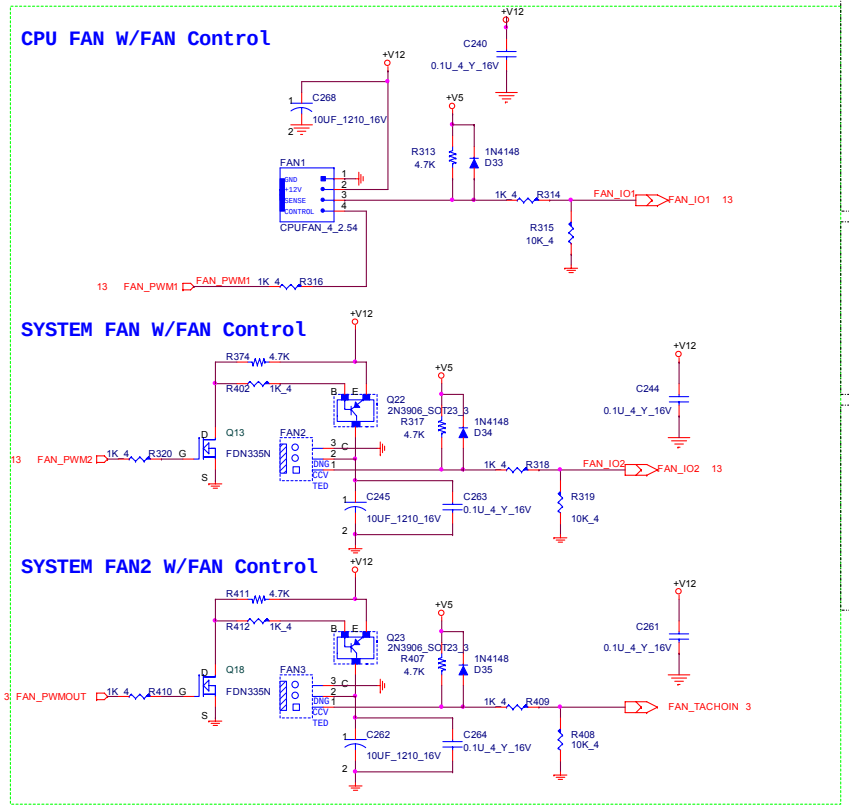

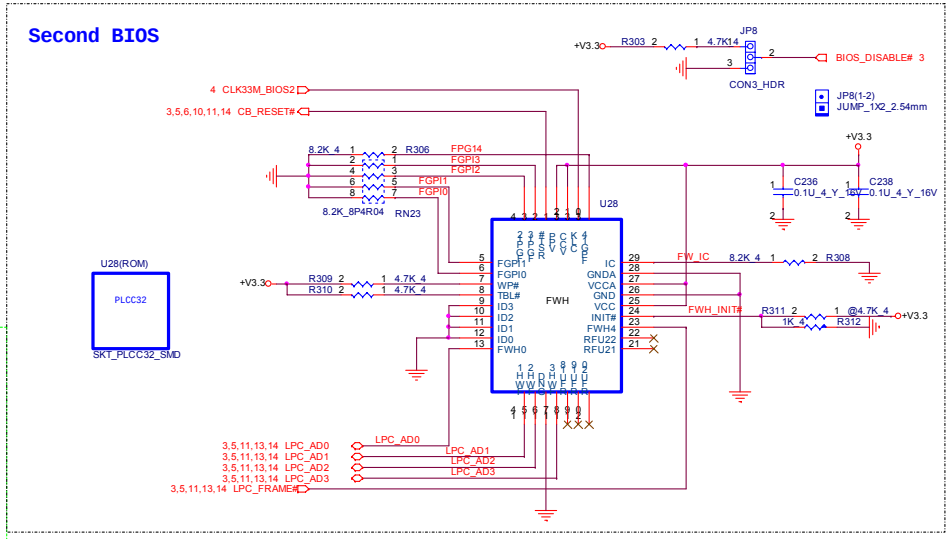

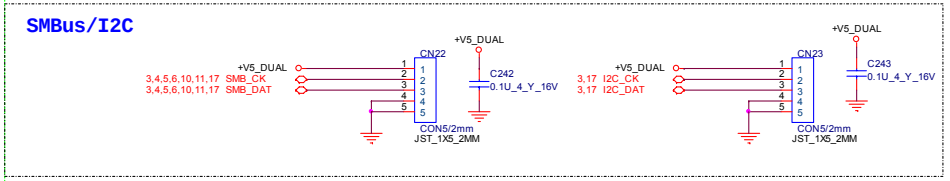

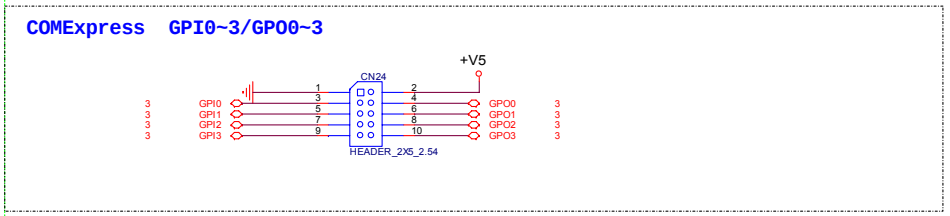

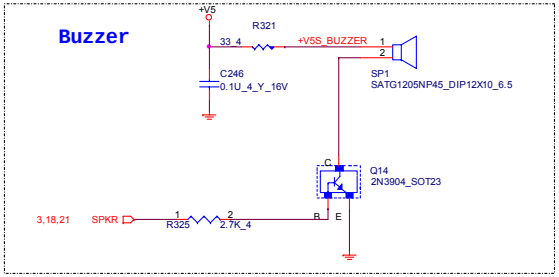

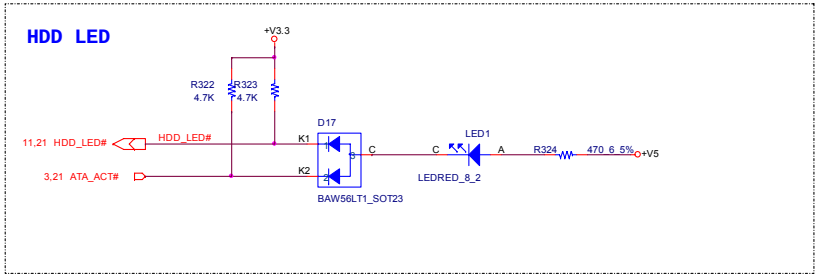

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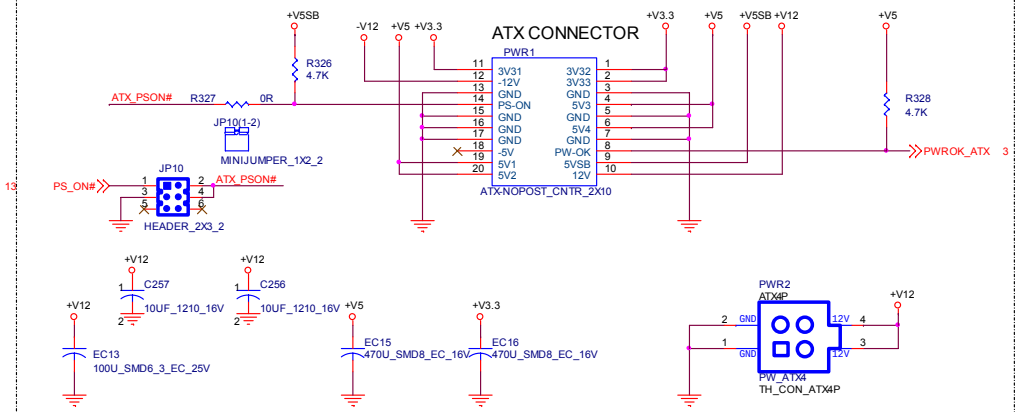
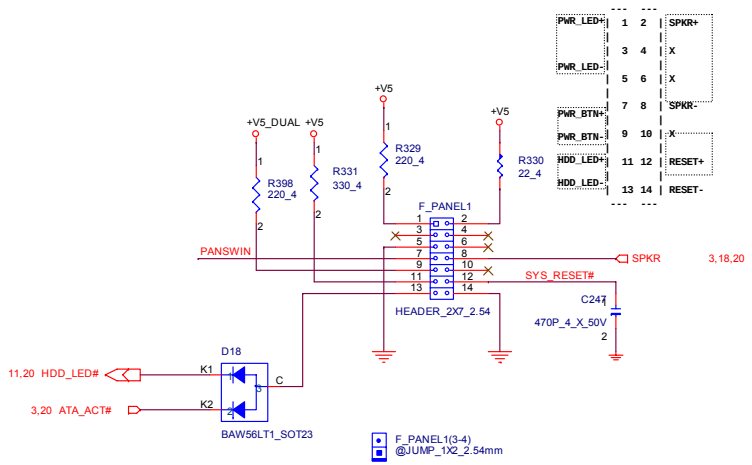
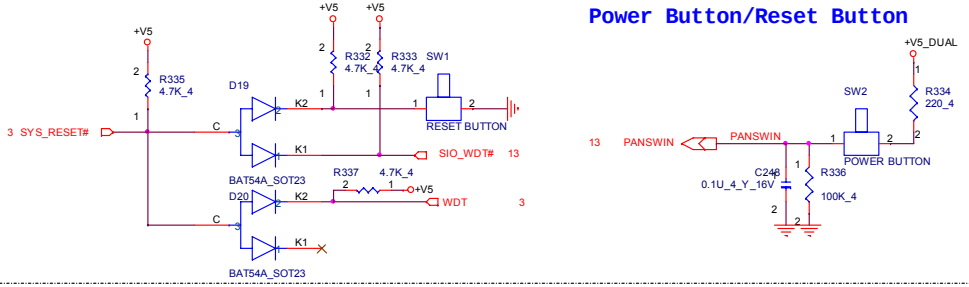
ATX Power Connector



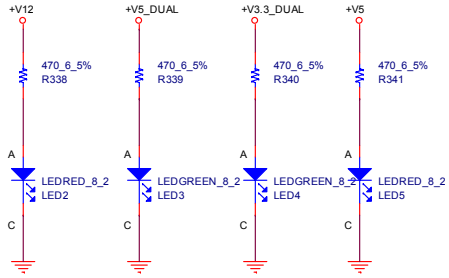
Frount Panel



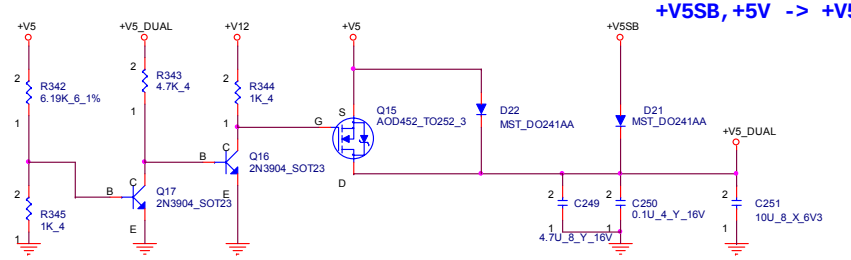
Power Button/Reset Button



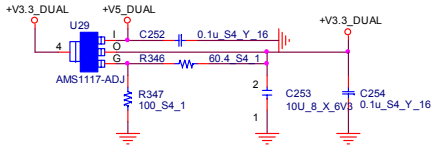
POWER LED(For Debug Use)



+V5SB,+5V -> +V5A@10A



+V5_DUAL -> +V3.3_DUAL@1A



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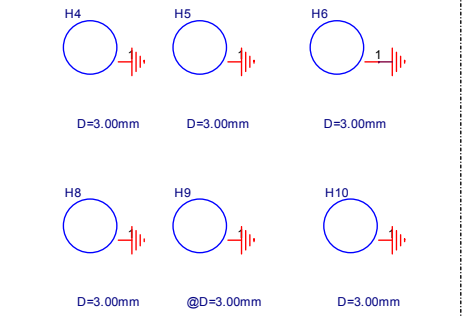
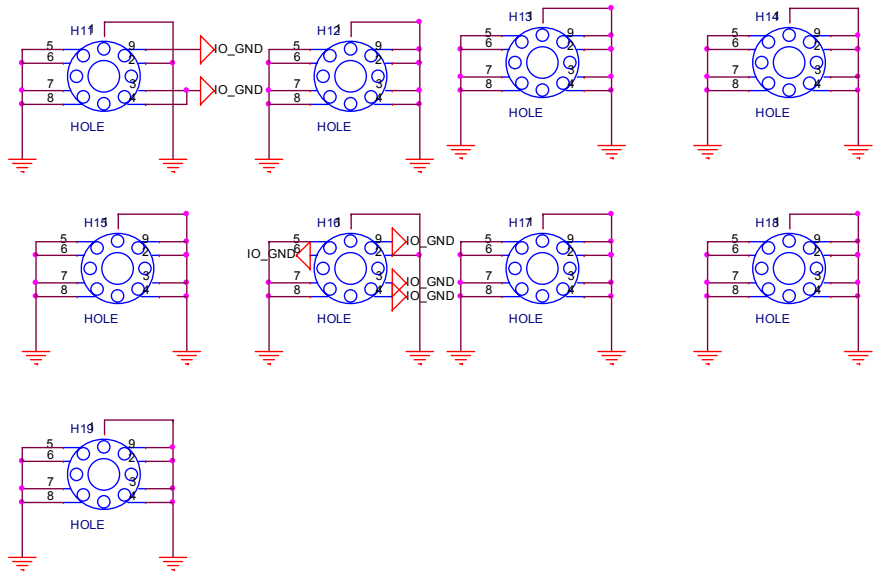
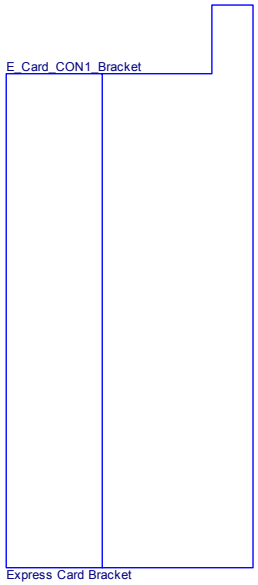
COM Module

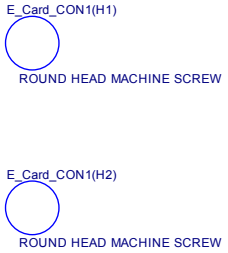


ATX

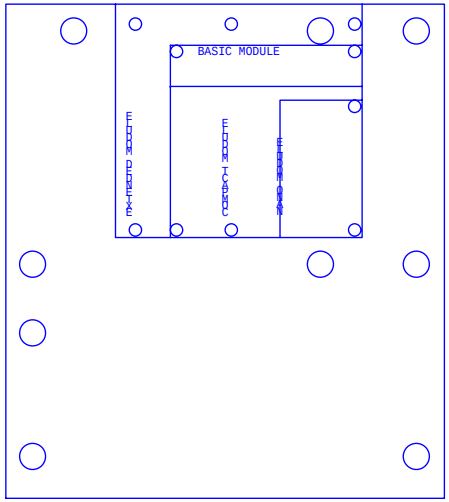


Express Card Module





PCB1



PCB_F119V101

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