

DIO-64/DIO-48

User's Manual

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DIO-64 64 Bit Digital I/O With Timer/Counter Board

1. Features

- 32 digital input lines
- 32 digital output lines
- Buffer output for higher driving capability
- 3 independent programmable 16 bit down counter
- One 16 bit counter , one 32 bit counter with a 4 MHz time base
- Breadboard area for add-on circuit
- Backward compatible to 720 series card

2. Applications

- Digital I/O control
- Contact closure monitoring
- Alarm monitoring
- BCD interface driver
- Event and frequency counting

3. Product Check List

The package includes the following items:

- One piece of DIO-64 card
- One company floppy diskette or CD
- One Quick Start Guide

Attention!

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

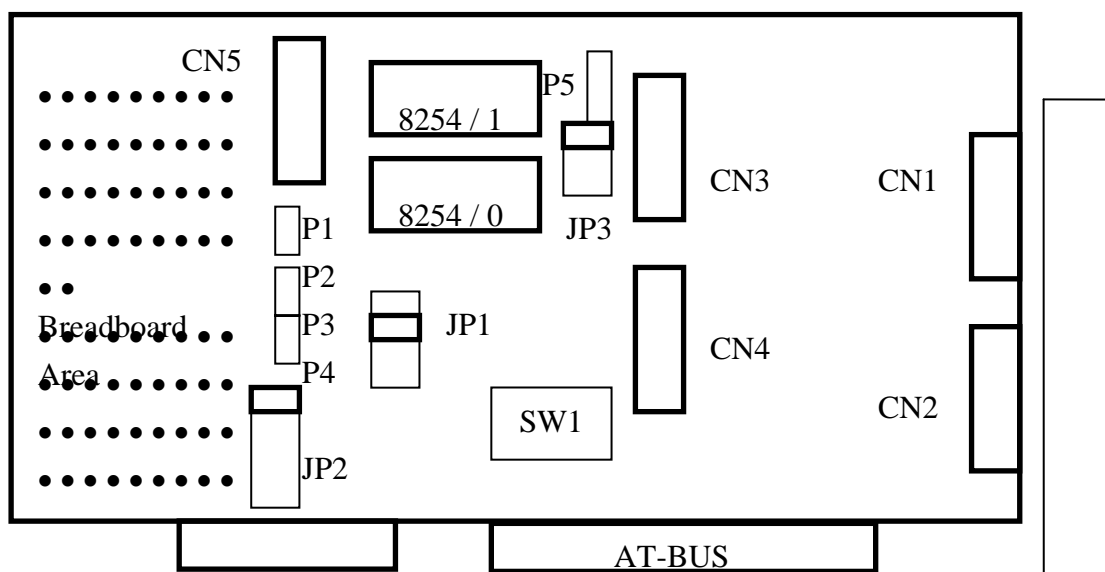
4. Specification

Model Name	DIO-64/3	DIO-64/6
Digital Input		
Channels	32	
Compatibility	5 V/TTL	
Input Voltage	Logic 0: 0.8 V max. Logic 1: 2.0 V min.	
Response Speed	1.0 MHz (Typical)	
Digital Output		
Channels	32	
Compatibility	5 V/TTL	
Output Voltage	Logic 0: 0.4 V max. Logic 1: 2.4 V min.	
Output Capability	Sink: 0.8 mA @ 0.8 V Source: -2.4 mA @ 2.0 V	
Response Speed	1.0 MHz (Typical)	
Timer/Counter		
Channels	3 independent	6 independent
Resolution	16-bit	
Input Frequency	10 MHz max.	
Clock Source	250 kHz/500 kHz/1 MHz/2 MHz	
Reference Clock	Internal: 4 MHz	
General		
Bus Type	ISA	
I/O Connector	20-pin box header x 5	
Dimensions (L x W x D)	930 mm x 135 mm x 22 mm	
Power Consumption	500 mA @ +5 V	
Operating Temperature	0 ~ 60 °C	
Storage Temperature	-20 ~ 70 °C	
Humidity	5 ~ 85% RH, non-condensing	

5. Functional Description

The DIO-64 provides 32 digital input channels , 32 output channels and 6 counter/timer channels The DIO-64 consists of two 16 bit input port and two 16 bit output port . The user can use the DB-16P (or 782 series) to connect the interface of the input port (CN2, CN4) for isolation purpose. The user can use DB-16R (or 785 series) to interface to the output port (CN1, CN3) for relay control. There are four clock sources, 2 M, 1 M, 500 k, 250 k, on the board. The user can choose any one by jumper setting .The user can use frequency from the soldering pad.

5.1. Layout



Model :

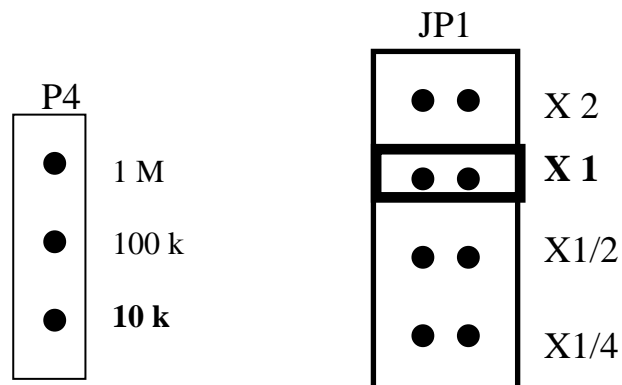
DIO-64 / 3 : 32 Digital I/O with 3 Timer / Counter Board
(One 8254 chip)

DIO-64 / 6 : 32 Digital I/O with 6 Timer / Counter Board
(Two 8254 chip)

5.2. Jumper setting

5.2.1 JP1 Clock source

The DIO-64 offers three clock sources which are 1 M, 100 k, 10 k. These frequencies can be double, half or quartered by jumper setting.



X 1 : Default setting

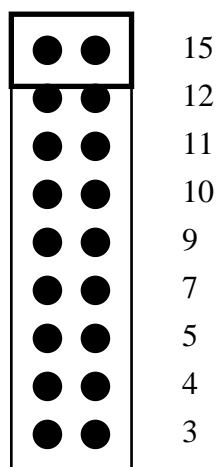
For Example:

If you want to get a 10 k clock source, you should insert the jumper on the X 1 first and then take the 10 k clock source from p4 the corresponding soldering pad.

5.2.2 Interrupt Setting

The DIO-64 provides interrupt function when the second 8254 chip is installed. (Ref. Order information DIO-64/6 on board two 8254 chip) You can use timer pacer, external pacer or event counting trigger interrupt.

The interrupt levels setting by JP2

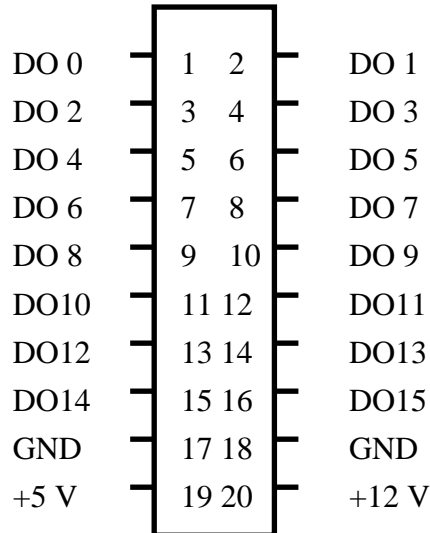


Default setting : IRQ15

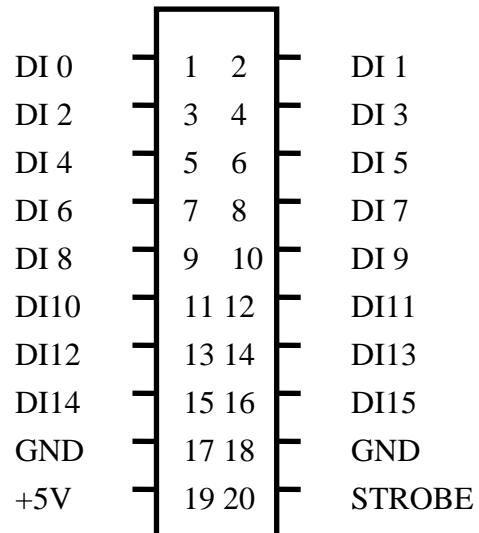
Note : Be sure there is no other add-on card in the same interrupt level.

5.3. Pin Assignment

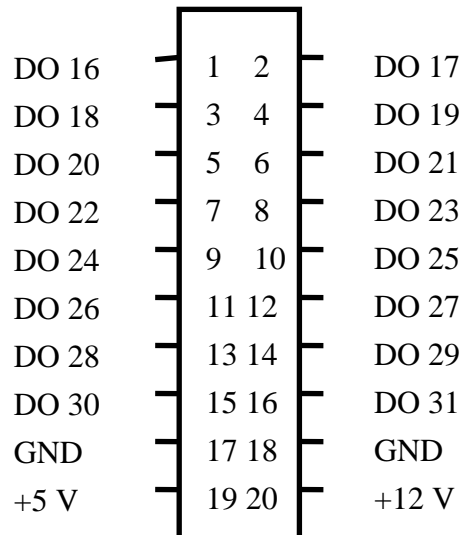
CN 1



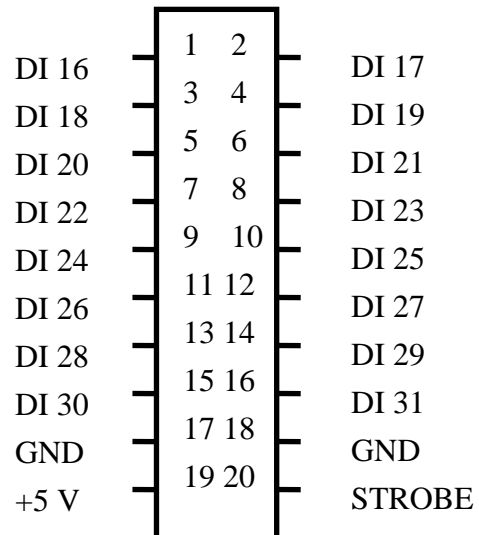
CN 2



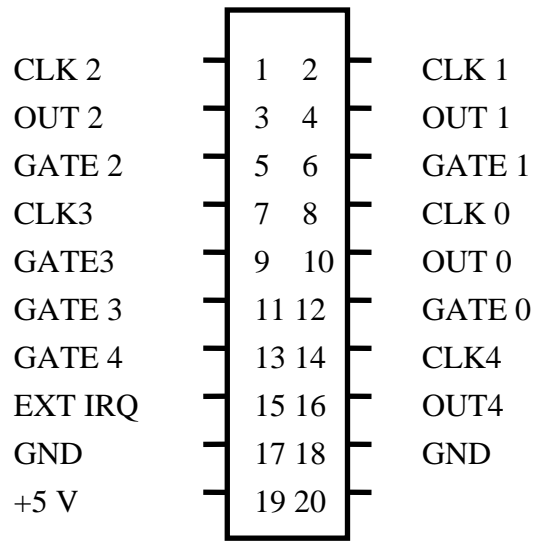
CN 3



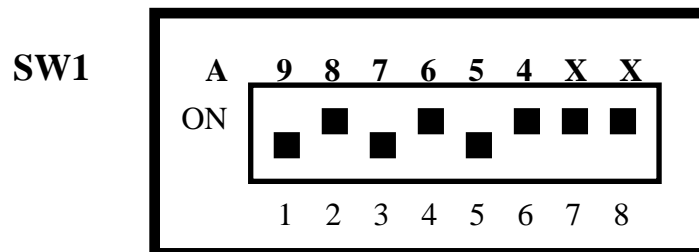
CN 4



CN5



5.4. BASE Address Setting



Default Base Address (2A0)

For Example

How to select 2 A 0 (Hex)

OFF → 1
ON → 0

	2		A				0
	OFF	ON	OFF	ON	OFF	ON	X
→	1	0	1	0	1	0	X
	A9	A8	A7	A6	A5	A4	X

The detail SW1 base addresses setting. Please refer to 5.4.1 Base Address Table.

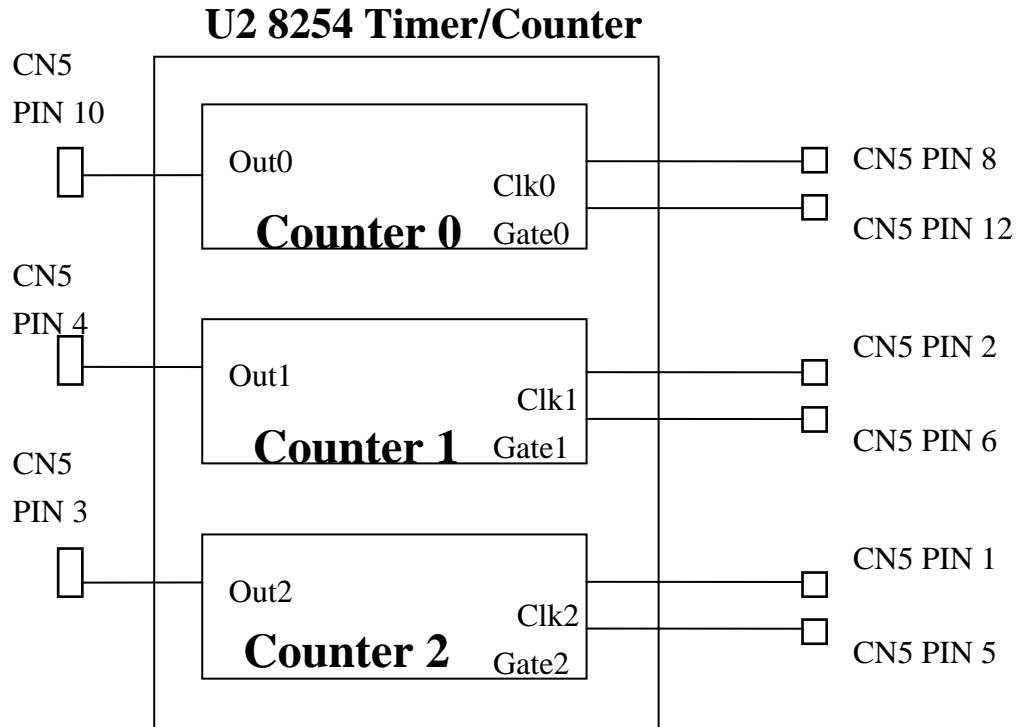
5.4.1 Base Address Table:

(*): Default setting

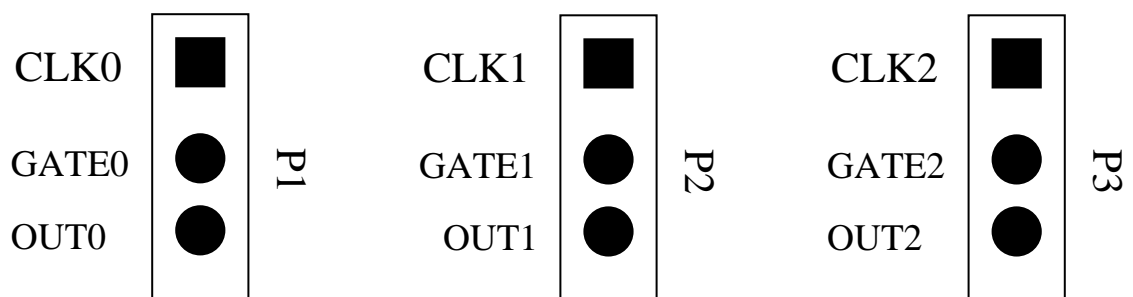
IO Address	1 A9	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F	OFF	ON	ON	ON	OFF	ON
230-23F	OFF	ON	ON	ON	OFF	OFF
240-24F	OFF	ON	ON	OFF	ON	ON
250-25F	OFF	ON	ON	OFF	ON	OFF
260-26F	OFF	ON	ON	OFF	OFF	ON
270-27F	OFF	ON	ON	OFF	OFF	OFF
280-28F	OFF	ON	OFF	ON	ON	ON
290-29F	OFF	ON	OFF	ON	ON	OFF
2A0-2AF(*)	OFF	ON	OFF	ON	OFF	ON
2B0-2BF	OFF	ON	OFF	ON	OFF	OFF
2C0-2CF	OFF	ON	OFF	OFF	ON	ON
2D0-2DF	OFF	ON	OFF	OFF	ON	OFF
2E0-2EF	OFF	ON	OFF	OFF	OFF	ON
2F0-2FF	OFF	ON	OFF	OFF	OFF	OFF
300-30F	OFF	OFF	ON	ON	ON	ON
310-31F	OFF	OFF	ON	ON	ON	OFF
320-32F	OFF	OFF	ON	ON	OFF	ON
330-33F	OFF	OFF	ON	ON	OFF	OFF
340-34F	OFF	OFF	ON	OFF	ON	ON
350-35F	OFF	OFF	ON	OFF	ON	OFF
360-36F	OFF	OFF	ON	OFF	OFF	ON
370-37F	OFF	OFF	ON	OFF	OFF	OFF
380-38F	OFF	OFF	OFF	ON	ON	ON
390-39F	OFF	OFF	OFF	ON	ON	OFF
3A0-3AF	OFF	OFF	OFF	ON	OFF	ON
3B0-3BF	OFF	OFF	OFF	ON	OFF	OFF
3C0-3CF	OFF	OFF	OFF	OFF	ON	ON
3D0-3DF	OFF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

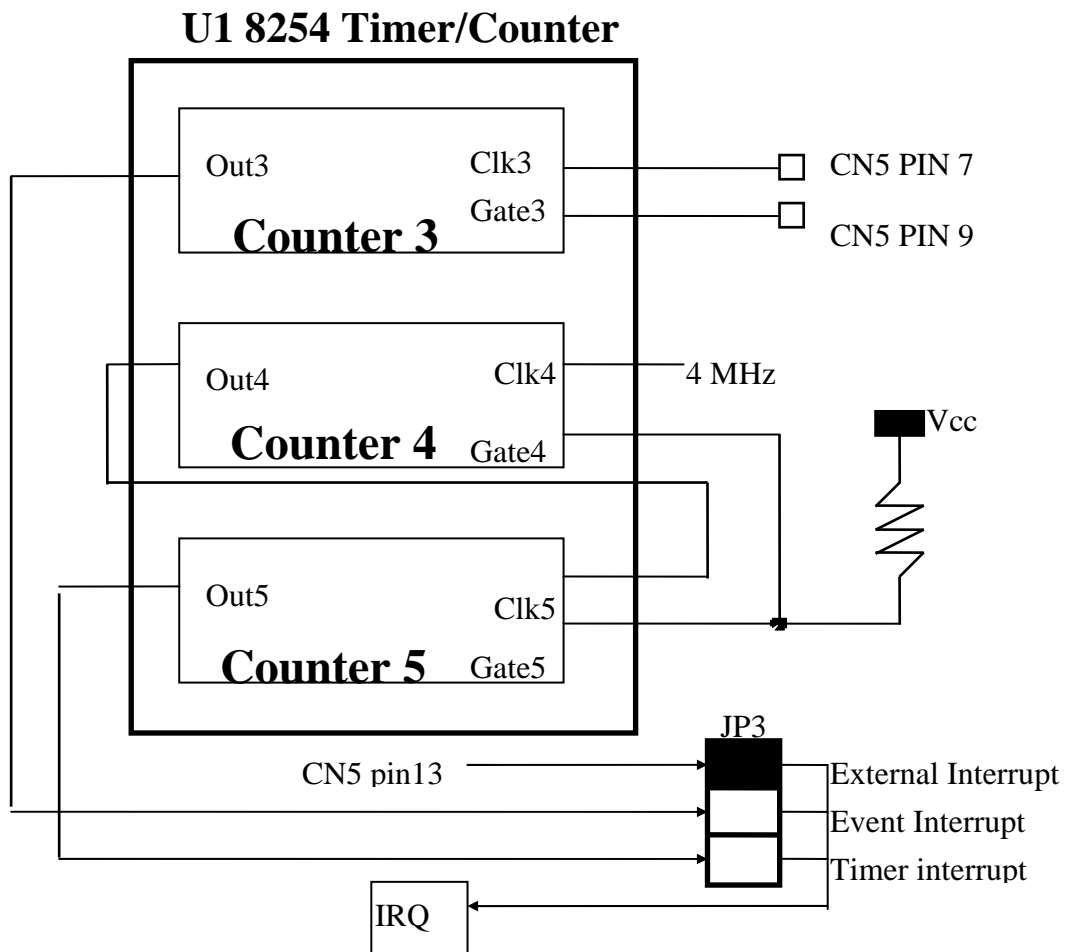
5.5. Timer /counter signal

The First 8254 Chip is for general purpose timer/counter.

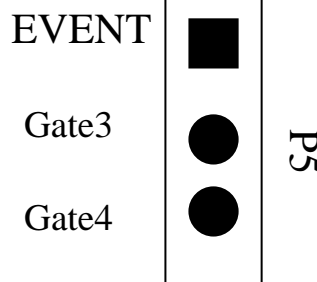


Pad assignment





Pad assignment



1. The second 8254 chip is used to generate interrupt trigger signals.
2. The counter3 accept event signal and its will generate trigger signal of interrupt.
3. The counter 4 and counter 5 are cascaded together, the clock source is 4 MHz, it can generate timer pacer trigger of interrupt.

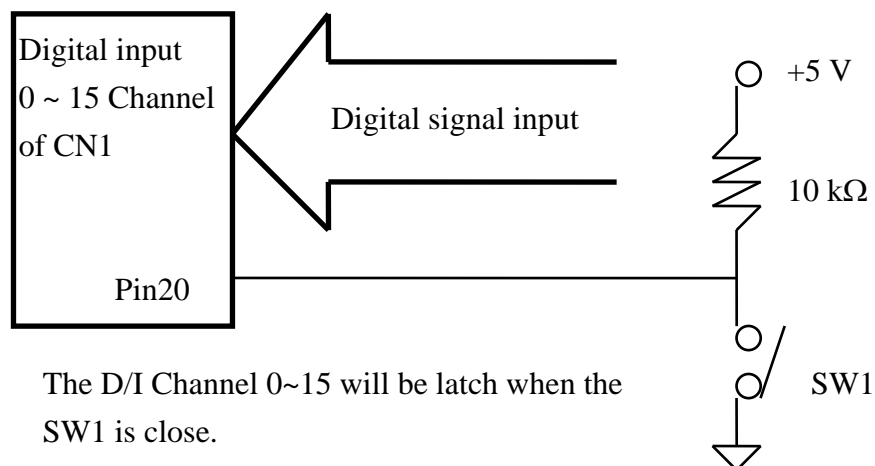
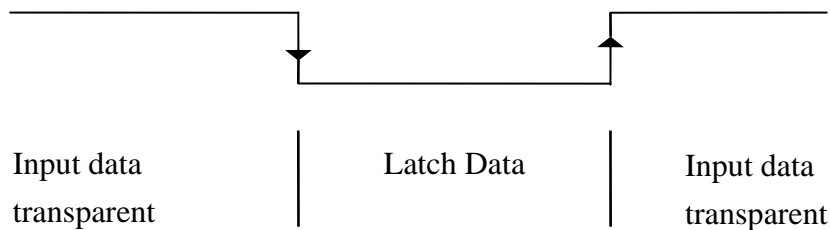
Note : The second 8254 chip is option (Ref. Order information)

If the second 8254 chip is not installed only the external interrupt function can be used.

5.6. How to latch the digital input

In some application, you want to use an external signal to latch the input; you can use the STROBE pin. Refer to the following figure.

STROBE CN2 Pin 20 or CN4 Pin 20



Note : If no signal is connected to strobe pin , the input data is transparent.

6. I/O Register & Programming

6.1. I/O Registers

The DIO-64 I/O registers are showed in Table 3-1

I/O Address	Read	Write
Base+0	D/I CH: 0~7	D/O CH 0~7
Base+1	D/I CH 8~15	D/O CH 8~15
Base+2	D/I CH 16~23	D/O CH 16~23
Base+3	D/I CH 24~31	D/O CH 24~31
Base+4	Counter 0	
Base+5	Counter 1	
Base+6	Counter 2	
Base+7	Control Word of Counter 0~2	
Base+8	Counter 3	
Base+9	Counter 4	
Base+A	Counter 5	
Base+B	Control Word of Counter 3~5	

Table 3.1

D/I: Digital Input

D/O: Digital Output

Counter n : Timer/Counter Channel

6.2. Digital Input and Digital Output

The DIO-64 provides 32 digital input channels and 32 digital output Channel

6.2.1 Digital Input Data Format

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base+0	D/I 7	D/I 6	D/I 5	D/I 4	D/I 3	D/I 2	D/I 1	D/I 0
Base+1	D/I 15	D/I 14	D/I 13	D/I 12	D/I 11	D/I 10	D/I 9	D/I 8
Base+2	D/I 23	D/I 22	D/I 21	D/I 20	D/I 19	D/I 18	D/I 17	D/I 16
Base+3	D/I 31	D/I 30	D/I 29	D/I 28	D/I 27	D/I 26	D/I 25	D/I 24

6.2.2 Digital Output Data Format

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Base+0	D/O 7	D/O 6	D/O 5	D/O 4	D/O 3	D/O 2	D/O 1	D/O 0
Base+1	D/O 15	D/O 14	D/O 13	D/O 12	D/O 11	D/O 10	D/O 9	D/O 8
Base+2	D/O 23	D/O 22	D/O 21	D/O 20	D/O 19	D/O 18	D/O 17	D/O 16
Base+3	D/O 31	D/O 30	D/O 29	D/O 28	D/O 27	D/O 26	D/O 25	D/O 24

6.3. Programming

6.3.1 Digital Input

The digital input states are read as a byte from the port at I/O register Base+n (ref. sec. 3)

For example: (Basic Language)

Bas=&H2A0	'Set Base Address
DIVALUE0=INP(BAS+0)	'Read D/I Channel 0~7
DIVALUE1=INP(BAS+1)	'Read D/I Channel 8~15
DIVALUE2=INP(BAS+2)	'Read D/I Channel 16~23
DIVALUE3=INP(BAS+3)	'Read D/I Channel 24~31

6.3.2 Digital Output

The digital output states are written a byte to the I/O registers Base+n (ref. sec 3.)

For Example (Basic Language)

BAS=&H2A0	'Set Base address 2A0 Hex
OUT BAS+0 , &H1	'Set D/O Channel 0 High
OUT BAS+1 , &HFF	'Set D/O Channel 8~15 High
OUT BAS+2 , &H8	'Set D/O Channel 19 High
OUT BAS+3 , &H0	'Set D/O Channel 24~32 Low

6.4 Timer / Counter

6.4.1 8254 Programmable Interval Timer

The 8254 contains three independent, programmable, multi-mode 16-bit timers/counters. It is designed as a general purpose device.

The 8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be programmed clocked at rates from DC to 8 MHz. The software controls the loading and starting of the counters to provides accurate multiple time delays.

For more information about the 8254, please refer the Intel Microprocessor and Peripheral Handbook

6.4.2 I/O Register

Base+4	Low Byte or High Byte of Counter 0
Base+5	Low Byte or High Byte of Counter 1
Base+6	Low Byte or High Byte of Counter 2
Base+7	Counter 0~2 Control Word
Base+8	Low Byte or High Byte of Counter 3
Base+9	Low Byte or High Byte of Counter 4
Base+A	Low Byte or High Byte of Counter 5
Base+B	Counter 3~5 Control Word

6.4.3 Control Word Format

Base+7 (Counter 0~2) and Base+B (Counter 3~5)

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Note :

SCn : Select Counter

RLn : Read/Load

Mn : Mode

SC - Select Counter

SC1	SC0	Counter
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL - Read/Load

RL1	RL0	Read/Load
0	0	Counter Latching Operation
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only
1	1	Read/Load least significant byte first , then most significant byte

M - Mode

M2	M1	M0	Mode
0	0	0	Mode 0 (Interrupt on terminal count)
0	0	1	Mode 1 (Programmable One-Shot)
0	1	0	Mode 2 (Rate Generator)
0	1	1	Mode 3 (Square Wave Rate Genrate)
1	0	0	Mode 4 (Software Strobe)
1	0	1	Mode 5 (Hardware Triggered Trobe)

Please Ref. Intel Data Sheet mode Control of 8253 or 8254 Chip

BCD

0	Binary counter, 16-bits
1	BCD Counter , 4-decades

6.5 Programming Timer/Counter

Programming in Basic Language

First, Initial the Timer/Counter Channel, Read/Write Control, Mode, BCD.

Example :

- (1) Counter Select : channel 0
- (2) Read/Write Control : Read least significant byte then most significant byte
- (3) Mode Control : Mode 0 (Interrupt on terminal count)
- (4) BCD mode

The control word shows as following tables (Ref. Sec. 3.4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
0	0	1	1	0	0	0	0
8	4	2	1	8	4	2	1

Control Word : 0x3 0

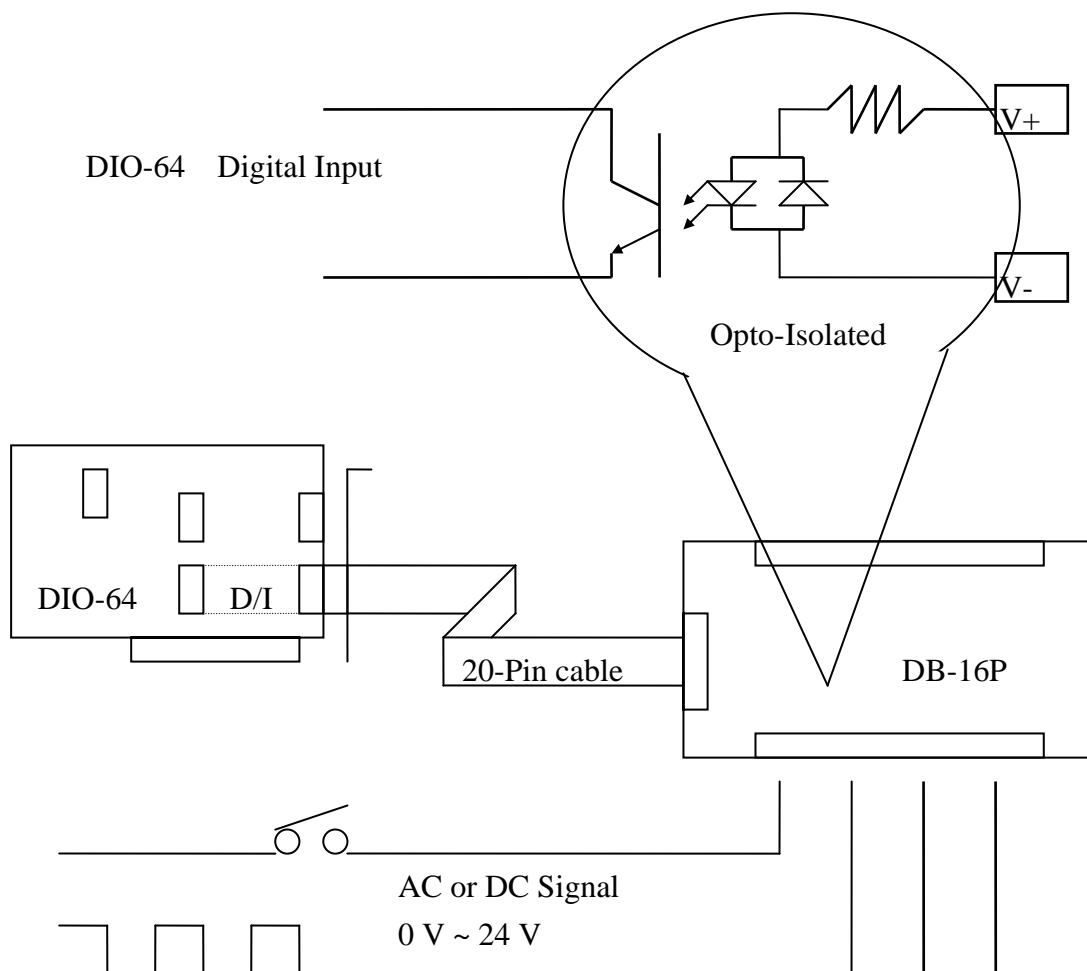
```

Bas=&h2C0          ' Set Base Address
' Initial 8254
Out Bas + 7 , &H30    ' Write First 8254 Chip Control Word
Out Bas + 4 , &H10    ' Write LSB First
Out Bas + 4 , &H10    ' Then Write MSB
' Read Counter
WHILE CDATA> 0
    LSB = Inp(Bas+4)    ' Read Counter Channel 0 LSB
    MSB= Inp(Bas+4)    ' Read Counter Channel 0 MSB
    CDATA=MSB*256+LSB
    PRINT " Counter Value = "; CDATA
WEND
END
  
```

7. Terminal Board

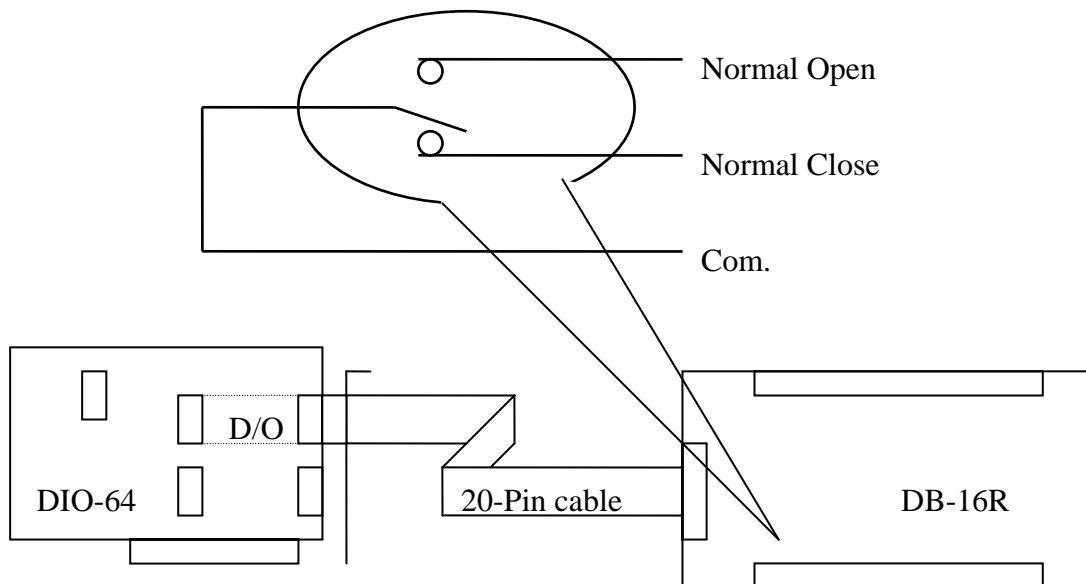
7.1 DB-16P

The DB-16P is a 16 Channel isolated digital input daughter board. The optically isolated inputs of the DB-16P consist of a bi-directional optocoupler with a resistor for current sensing. You can use the DB-16P to sense DC signal from TTL levels up to 24 V, or use the DB-16P to sense a wide range of AC signals. You can use the board to isolate the computer from large common-mode voltages, ground loops and voltage spikes that often occur in industrial environments.



7.2 DB-16R

The DB-16R 16 channel relay output board consists of 16 Form C relays for efficient switch of load by programmed control. It is connector and functionally compatible with 785 series board but with industrial type terminal block. The relays are energized by applying 5V voltage signal to the appropriate relay channel on the 20-pin flat connector. 16 indicator LEDs, one for each relay, light when their associated relay is activated. To avoid overloading your PC's power supply, this board provides a screw terminal for power supply.



Note:

Channel : 16 Form C Relay

Relay : Switching up to 0.5 A at 110 V_{AC} / 1 A at 24 V_{DC}

DIO-48 48 Bit OPTO-22 Compatible DI/O Board

1. Features

- 48 digital I/O lines
- OPTO-22 pin compatible
- Buffer output for higher driving capability than 8255
- High output driving capability
- One 16 bit programmable event counter
- One 32 bit programmable timer
- Programmable interrupt handling
- 32.768 kHz , 1 MHz, 2 MHz or 4 MHz clock source
- IRQ level: IRQ3 ~ IRQ15

2. Applications

- Interfacing with any OPTO-22 compatible I/O module
- Digital I/O control
- Contact closure monitoring
- Useful with parallel interface devices

3. Product Check List

The package includes the following items:

- One piece of DIO-48 card
- One company floppy diskette or CD
- One Quick Start Guide

Attention!

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

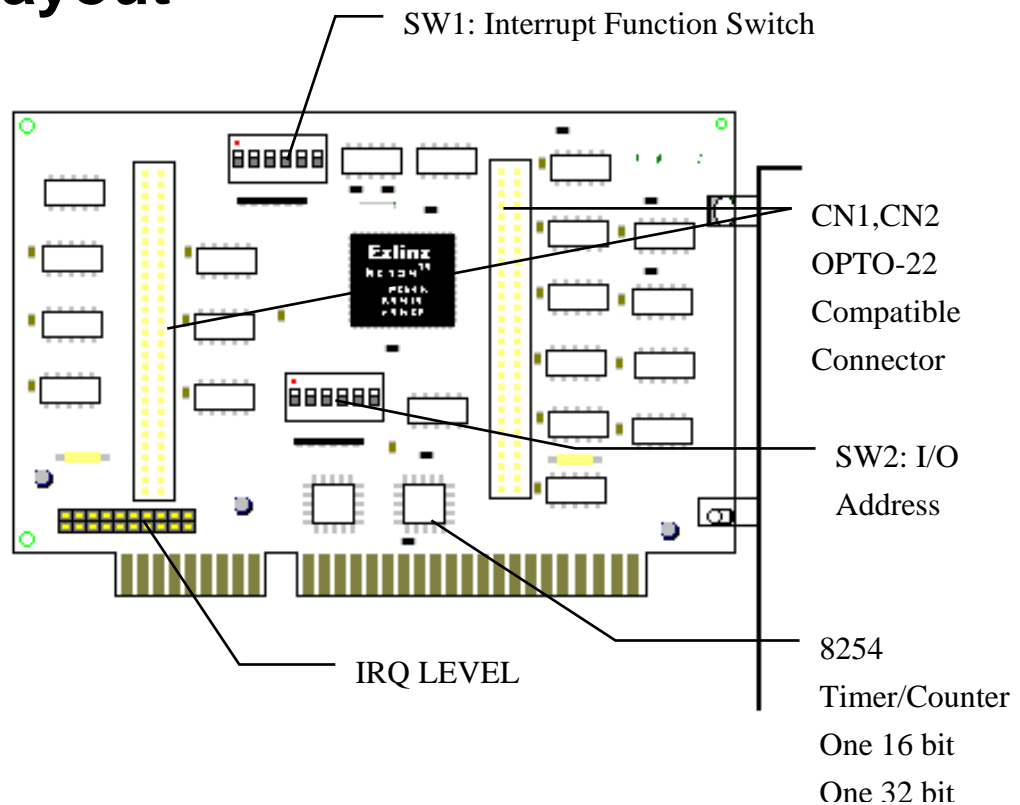
4. Specification

Model Name		DIO-48
Digital Input		
Channels	48 (OPTO-22 compatible)	
Compatibility	5 V/TTL	
Input Voltage	Logic 0: 0.8 V max. Logic 1: 2.0 V min.	
Response Speed	1.0 MHz (Typical)	
Digital Output		
Channels	48 (OPTO-22 compatible)	
Compatibility	5 V/TTL	
Output Voltage	Logic 0: 0.4 V max. Logic 1: 2.4 V min.	
Output Capability	Sink: 0.8 mA @ 0.8 V Source: -2.4 mA @ 2.0 V	
Response Speed	1.0 MHz (Typical)	
Timer/Counter		
Channels	3 independent	
Resolution	16-bit	
Input Frequency	10 MHz max.	
Clock Source	32.768 kHz/2 MHz/4 MHz	
General		
Bus Type	ISA	
I/O Connector	50-pin box header x 2	
Dimensions (L x W x D)	159 mm x 120 mm x 22 mm	
Power Consumption	900 mA @ +5 V	
Operating Temperature	0 ~ 60 °C	
Storage Temperature	-20 ~ 70 °C	
Humidity	5 ~ 85% RH, non-condensing	

5. Functional Description

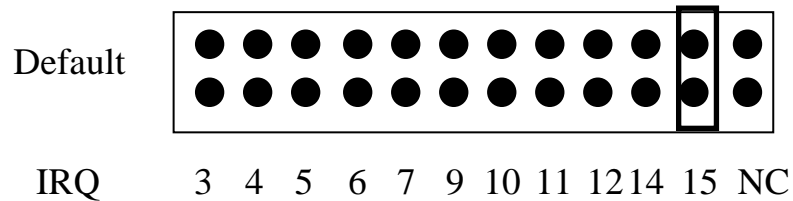
The DIO-48 provides 48 TTL digital I/O lines. It emulates two channel 8255 mode 0 (basic input / output mode) and has an increased output current of 15 mA (source) and 64 mA (sink), allowing it to drive LED, relay, etc. Each connector consists of three 8-bit bi-directional ports and two input lines for interrupt enable and interrupt. The eight-bit ports are named port A (PA), port B (PB), port C (PC). The port C can be split into two nibble-wide ports. All ports are configured as inputs upon power-up or reset. The DIO-48 uses 3 consecutive I/O locations in I/O addressing space. The base address is selectable using a 6-position dip switch from 200 to 3FF hex. The interrupt signal can be connected to any of the interrupt levels 2 through 15 available on the PC bus via a jumper.

5.1 Layout



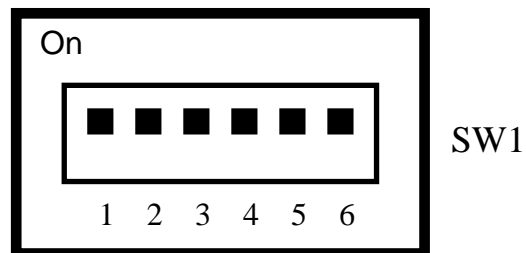
5.2 Jumper setting

5.2.1 Interrupt jumper setting



5.2.2 IRQ Source Selection

The DIO-48 provides event trigger mode & timer trigger mode for interrupt handling. You can use SW1 to set trigger method and clock source.



SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6
IRQ	Function	Selection	Trigger Edge	Clock	Source Selection

SW1-1	SW1-2	SW1-3	Mode.	Interrupt Function
On	On	On	0	Event Trigger from CN1PC0
Off	On	On	1	Timer Trigger
On	Off	On	2	CN1PC3
Off	Off	On	3	CN1PC3 & !CN1PC7
On	On	Off	4	CN2PC3
Off	On	Off	5	CN2PC3 & !CN2PC7
On	Off	Off	6	Soft Trigger
Off	Off	Off	7	Disable Interrupt

Note:

Mode 0 (Event trigger) : Clock source CN1PC0 via 8254 counter 0 (16 bit) to generate an interrupt

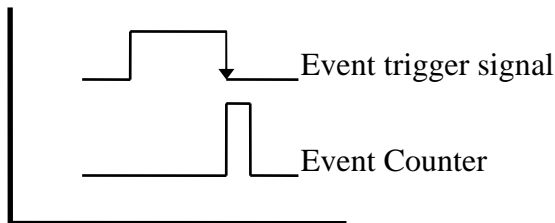
Mode 1 (Timer trigger) : Clock source 2 MHz or 32.768 kHz internal clock via 8254 counter 1 cascaded to counter 2 (32 bit) to generate an interrupt

Mode 2 ~ Mode 5 : Direct generate interrupt signal from PC3 or PC7 (! : NOT logic)

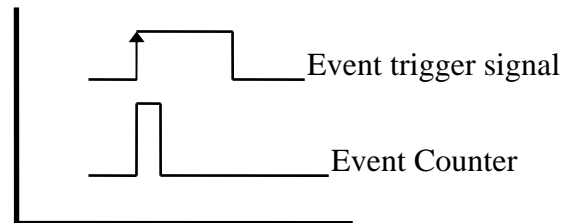
Mode 6 (Soft trigger) : Direct generate interrupt signal from I/O register (programmable).

Mode 7 (Disable) : Disable interrupt function.

SW1-4	Function
On	Falling Edge Trigger
Off	Rising Edge Trigger

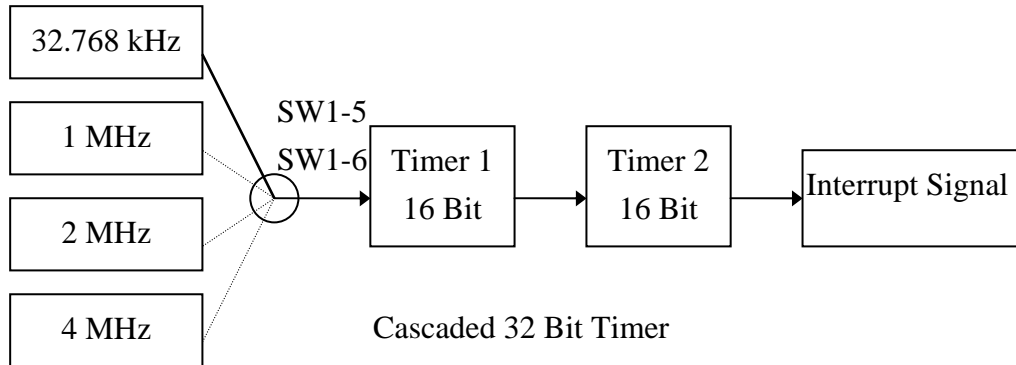


Falling Edge Trigger

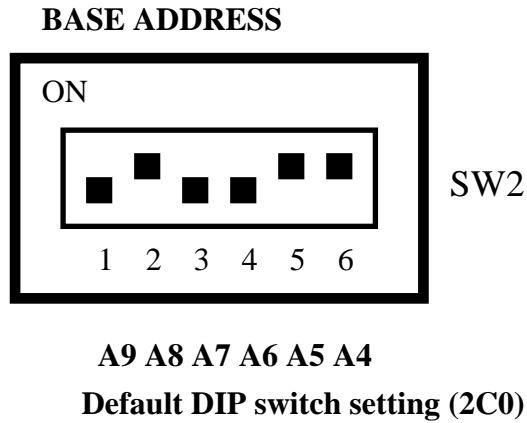


Rising Edge Trigger

SW1-5	SW1-6	Function
ON	ON	32.768 kHz (RTC)
OFF	ON	1 MHz
ON	OFF	2 MHz
OFF	OFF	4 MHz



5.3 BASE Address Setting



For Example

How to select 2 C 0 (Hex)

OFF → 1
ON → 0

2		C				0
OFF	ON	OFF	OFF	ON	ON	
1	0	1	1	0	0	
A9	A8	A7	A6	A5	A4	

→

The detail SW2 base addresses setting. Please refer to **5.3.1 Base Address Table**.

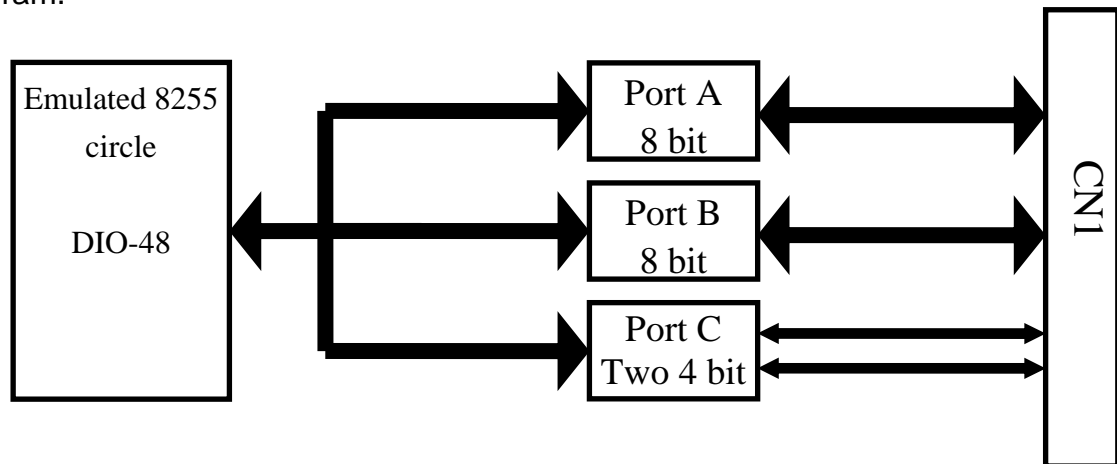
5.3.1 Base Address Table:

(*): Default setting

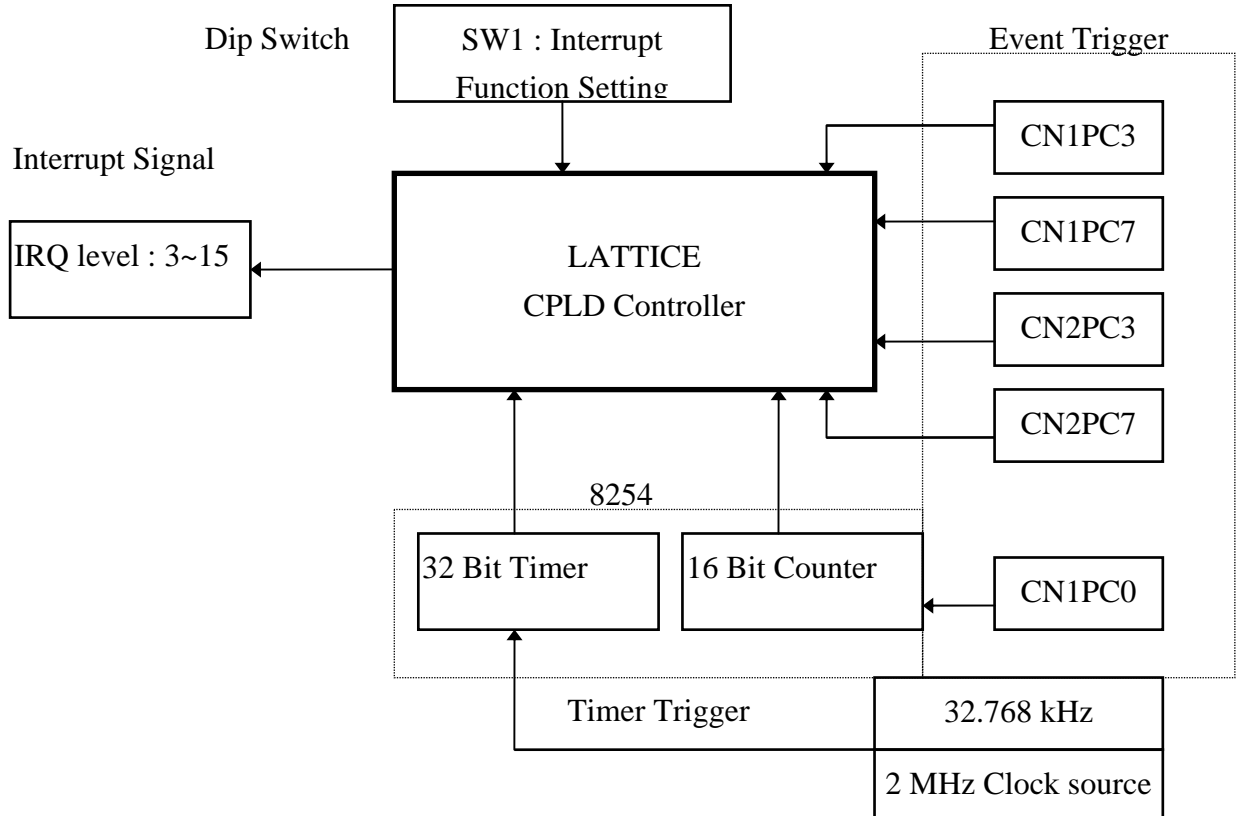
IO Address	1 A9	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F	OFF	ON	ON	ON	OFF	ON
230-23F	OFF	ON	ON	ON	OFF	OFF
240-24F	OFF	ON	ON	OFF	ON	ON
250-25F	OFF	ON	ON	OFF	ON	OFF
260-26F	OFF	ON	ON	OFF	OFF	ON
270-27F	OFF	ON	ON	OFF	OFF	OFF
280-28F	OFF	ON	OFF	ON	ON	ON
290-29F	OFF	ON	OFF	ON	ON	OFF
2A0-2AF	OFF	ON	OFF	ON	OFF	ON
2B0-2BF	OFF	ON	OFF	ON	OFF	OFF
2C0-2CF(*)	OFF	ON	OFF	OFF	ON	ON
2D0-2DF	OFF	ON	OFF	OFF	ON	OFF
2E0-2EF	OFF	ON	OFF	OFF	OFF	ON
2F0-2FF	OFF	ON	OFF	OFF	OFF	OFF
300-30F	OFF	OFF	ON	ON	ON	ON
310-31F	OFF	OFF	ON	ON	ON	OFF
320-32F	OFF	OFF	ON	ON	OFF	ON
330-33F	OFF	OFF	ON	ON	OFF	OFF
340-34F	OFF	OFF	ON	OFF	ON	ON
350-35F	OFF	OFF	ON	OFF	ON	OFF
360-36F	OFF	OFF	ON	OFF	OFF	ON
370-37F	OFF	OFF	ON	OFF	OFF	OFF
380-38F	OFF	OFF	OFF	ON	ON	ON
390-39F	OFF	OFF	OFF	ON	ON	OFF
3A0-3AF	OFF	OFF	OFF	ON	OFF	ON
3B0-3BF	OFF	OFF	OFF	ON	OFF	OFF
3C0-3CF	OFF	OFF	OFF	OFF	ON	ON
3D0-3DF	OFF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

5.4 Block Diagram & Pin Assignment

The CN1 and CN2 of DIO-48 emulate as Intel 8255 general purpose programmable peripheral interface. Figure shows DIO-48 I/O port block diagram.

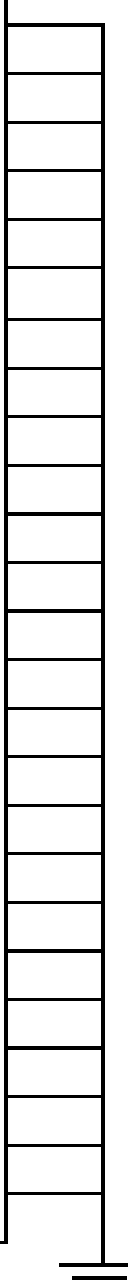


Interrupt Function Block Diagram



Pin assignment CN1 and CN2 (connector 1 and connector 2)

Port C 7	1	2	
Port C 6	3	4	
Port C 5	5	6	
Port C 4	7	8	
Port C 3	9	10	
Port C 2	11	12	
Port C 1	13	14	
Port C 0	15	16	
Port B 7	17	18	
Port B 6	19	20	
Port B 5	21	22	
Port B 4	23	24	
Port B 3	25	26	
Port B 2	27	28	
Port B 1	29	30	
Port B 0	31	32	
Port A 7	33	34	
Port A 6	35	36	
Port A 5	37	38	
Port A 4	39	40	
Port A 3	41	42	
Port A 2	43	44	
Port A 1	45	46	
Port A 0	47	48	
+5V out	49	50	



6. PROGRAMMING

The DIO-48 offers two OPTO-22 connectors which emulate MODE 0 of 8255. The mode 0 of 8255 provides basic input and output operations through each of the ports A, B and C. Output data is latched and input data follows the peripheral.

Mode 0 of 8255 PPI Functions

- 16 different configurations
- Two 8-bit port and two 4bit-ports
- Input are not latched
- Output are latched

6.1. I/O Register

Address (Hex)	Read	Write
Base+0	CN1_Port A Input	CN1_Port A Output
Base+1	CN1_Port B Input	CN1_Port B Output
Base+2	CN1_Port C Input	CN1_Port C Output
Base+3	Clear Interrupt	Configured Word
Base+4	CN2_Port A Input	CN2_Port A Output
Base+5	CN2_Port B Input	CN2_Port B Output
Base+6	CN2_Port C Input	CN2_Port C Output
Base+7	Soft Interrupt trigger	Configured Word
Base+8	NA	NA
Base+9	NA	NA
Base+A	NA	NA
Base+B	NA	NA
Base+C	8254 Counter 0 Read	8254 Counter 0 Write
Base+D	8254 Counter 1 Read	8254 Counter 1 Write
Base+E	8254 Counter 2 Read	8254 Counter 2 Write
Base+F	NA	8254 Configured Word

Note : Default base address 2C0(Hex)

CNn : Connector 1, 2

Port A : 8 bit D/I/O

Port B : 8 bit D/I/O

Port C : Two 4 bit D/I/O (nibble)

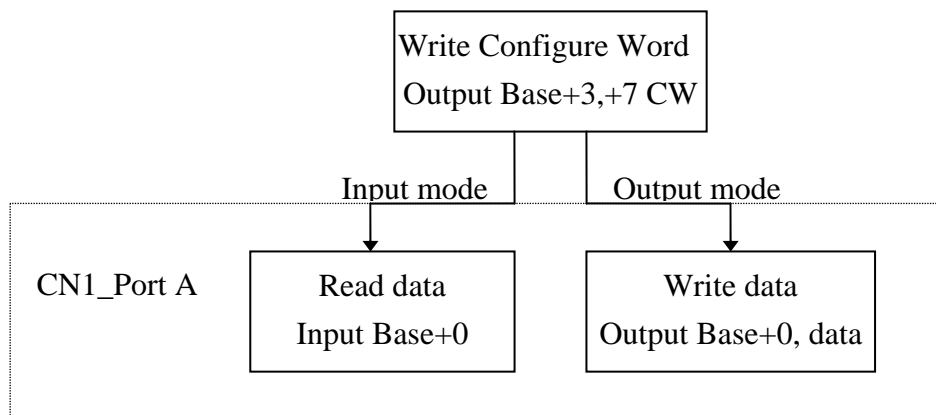
CW : Configure word (Initial digital input / output mode)

Configure Word (CW)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	?	?	0	?	?
1	0	0	Port A 1:Input 0:Output	Port C 1:Input 0:Output (High nibble)	0	Port B 1:Input 0:Output	Port C 1:Input 0:Output (Low nibble)

CW Register format

Note : When the PC is powered on or reset, all ports are configured as input mode. Please refer the CW register format table to configure each I/O port.



Configurations Table

	D4	D3	D1	D0
CW	PA0-PA7	PC4-PC7	PB0-PB7	PC0-PC3
80H	Output	Output	Output	Output
81H	Output	Output	Output	Input
82H	Output	Output	Input	Output
83H	Output	Output	Input	Input
88H	Output	Input	Output	Output
89H	Output	Input	Output	Input
8AH	Output	Input	Input	Output
8BH	Output	Input	Input	Input
90H	Input	Output	Output	Output
91H	Input	Output	Output	Input
92H	Input	Output	Input	Output
93H	Input	Output	Input	Input
98H	Input	Input	Output	Output
99H	Input	Input	Output	Input
9AH	Input	Input	Input	Output
9BH	Input	Input	Input	Input

Example :

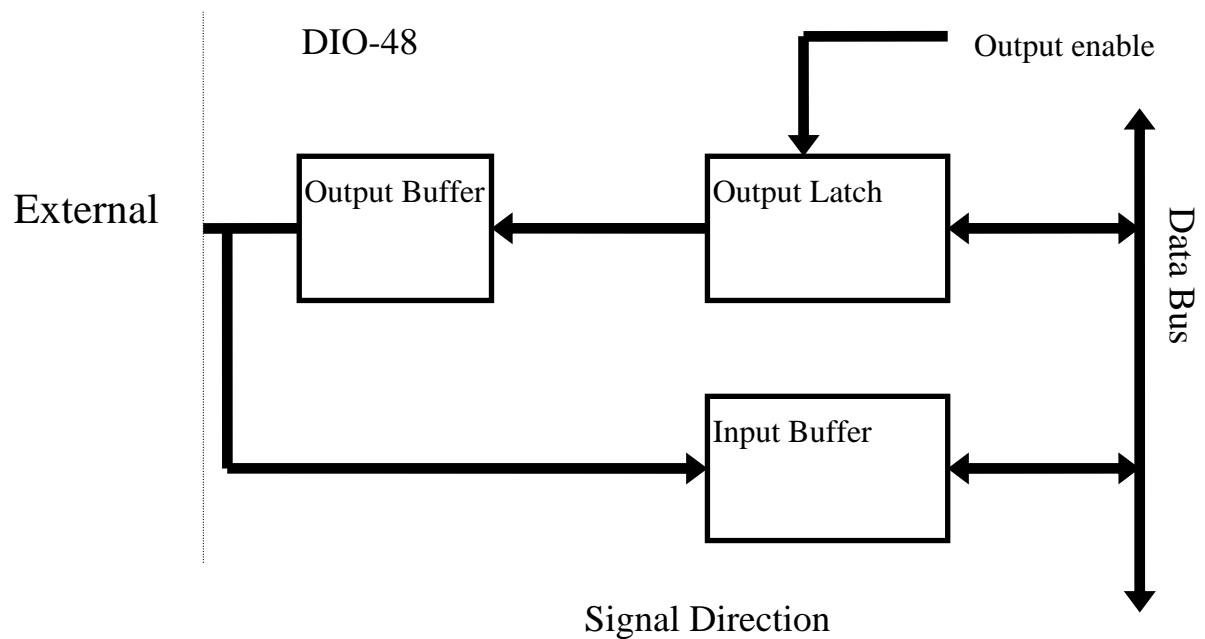
Out base+&H3 , &H80 'the CN1 all port will be configured as output mode

Out base+&H7, &H9B 'the CN2 all port will be configured as input mode

6.2. Digital Input / Output

The DIO-48 signal direction can be software programmable. When the user turn on or reset computer, all ports will be configured as input mode.

When the DIO-48 is programmed as an output mode, it will not output until program execute the output instruction.



6.2.1 D/I/O Demo program

The DIO-48 I/O card is very easy to programming input/ Output function.

Example (Quick Basic)

```
Bas=&H2C0
```

```
'===== Init DIO-48 Port A and Port B Input mode Port C output mode =====
```

```
OUT Bas+3,&H92 ' Reference Configuration table
```

```
'=====
```

```
PA = INP(Bas+0) 'Read Port A Data
```

```
PB = INP(Bas+1) 'Read Port B Data
```

```
OUT Bas+2 , &HFF 'Write Data to Port C , set Channel 0~7 is  
high
```

```
OUT Bas+3,&H80 ' Set Port A,B,C is Output Mode
```

```
OUT Bas+0, 0 ' Write Data to Port A
```

```
OUT Bas+1, 0 ' Write Data to port B
```

```
OUT Bas+2, 0 ' Write Data to Port C
```

```
OUT Bas+3,&H9B ' Set Port A,B,C is Input mode
```

```
PA=INP(Bas+0) ' Read Port A Data
```

```
PB=INP(Bas+1) ' Read Port B Date
```

```
PC=INP(Bas+2) ' Read Port C Date
```

Digital input / output example program (C Language) : DEMO_01.EXE ,
DEMO_02.EXE

6.3. Interrupt Handling

The Port C0 of each connector can generate a hardware interrupt to computer.

Use the interrupt you must set the IRQ level to be used. The JP1 is used to select IRQ level and the SW1 is used to select the desired interrupt trigger mode.

1. Set JP1 interrupt level 3~15
2. Set SW1 (1~3) to select interrupt mode


Mode 0	Event trigger (Clock source CN1_Port C 0)
Mode 1	Timer trigger (Clock Source 32.768 kHz or 1 MHz or 2 MHz or 4 MHz)
Mode 2	CN1_Port C 3 direct trigger
Mode 3	CN1_Port C 3 & !C7 direct trigger
Mode 4	CN2_Port C3 direct trigger
Mode 5	CN2_Port C3 & !C7 direct trigger
Mode 6	Soft trigger (read Base + 7)
Mode 7	Disable

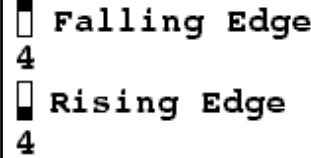
3. (Event trigger only) Set SW1 (4) to select edge trig (On : Falling edge trigger , Off : Rising edge trigger)
4. (Timer trigger only) Set SW1 (5) to select timer clock source.

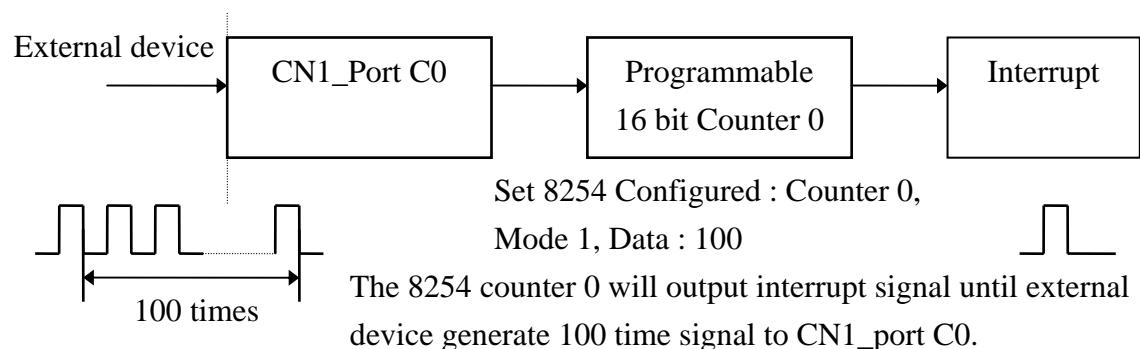
6.3.1 Interrupt Setting Example:

SW1: Setting

Mode 0 : Event Trigger
Demo program : IRQ_EVNT.EXE

On




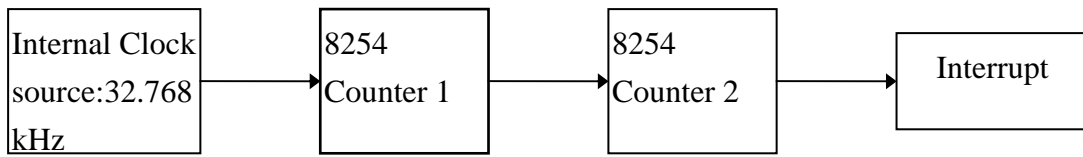


Mode 1 : Timer trigger

SW1 Setting



Demo program : IRQ_TIM.EXE



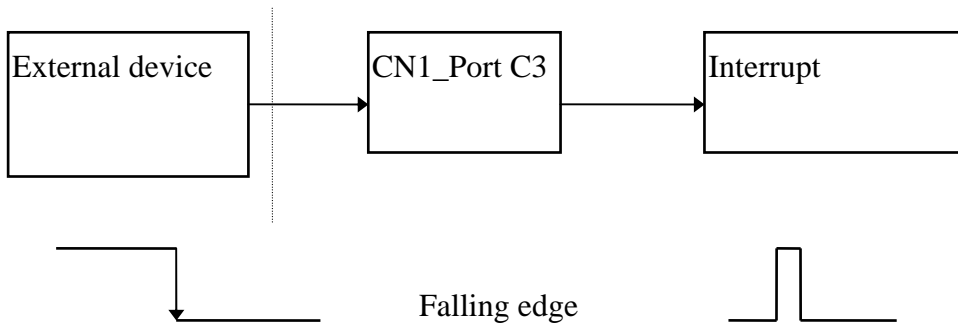
- 32.768
- 56 KHz
- 1MHz
- 2MHz
- 56
- 4MHz
- 56

8254 configured : Mode 1, Output interrupt signal freq :
 Counter 1 data : 32768 0.1 Hz
 Counter 2 data : 10
 $32.768 \text{ kHz} / (32768 \times 10) = 0.1 \text{ (Hz)}$
 Each 10 sec will generate an interrupt

Mode 2 : Direct trigger from CN1_Port C3



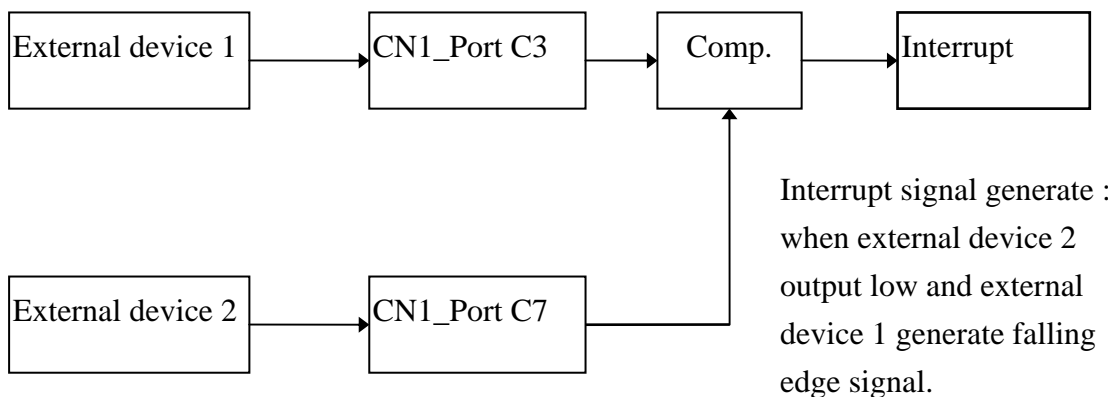
Demo program : IRQ_PC3F.EXE



Mode 3 : Direct trigger from CN1_Port C3 & !CN1_Port C7



Demo program : IRQ_PC37.EXE



Mode 4 : Direct trigger from CN2_Port C3

Demo program : IRQ_PF3F.EXE

Same as Mode 2, trigger source change to CN2_Port C3



Mode 5 : Direct trigger from CN2_Port C3 & !CN2_Port C7

Demo program : IRQ_PF37.EXE

Same as mode 3, trigger source change to CN2_Port C3 & C7



Mode 6 : Soft trigger

Demo program : IRQ_SOFT.EXE

Interrupt signal generated when you read BAS+3 register.



Mode 7 : Disable interrupt

Interrupt function disable.



6.3.2 Demo program : IRQ_TIM.EXE Source

Code:

/* Program : Pacer-trigger IRQ test program.

Description : This program generates the pacer signal by control 8254.
And 8254 will acknowledge PC by generating IRQ.

Hardware setting: The DIP switch SW1 should be set as following :

1 : OFF 2 : ON 3 : ON 4 : DON'T CARE

5 , 6 : pacer clock input select.

ON ON : RTC (real time clock 32.768 kHz)

OFF ON : 1.0 MHz

ON OFF : 2.0 MHz

OFF OFF : 4.0 MHz

IRQ : Set by IRQ 5

Note : This program can be compiled both in Turbo C 2.0 or
or Turbo C++ 3.0 and running under DOS environment.

*/

```

#include <stdio.h>
#include <conio.h>
#include <dos.h>
#ifdef __cplusplus
#define __CPPARGS      ...
#else
#define __CPPARGS
#endif
#include <stdio.h>
#include <conio.h>
#include <dos.h>
#define BASE           0x2C0
#define TIMER0         0x0C
#define TIMER1         0x0D
#define TIMER2         0x0E

int irq_gen;

void interrupt ( *old_irq5)(__CPPARGS);

void set_8254(unsigned int port,unsigned int value)
{
    unsigned int control;
    control = 0x36 | ( (port==TIMER2) ? 0x80 : 0x40 );
    outp(BASE+0x0F,control);
    outp(BASE+port,value & 0xff);
    outp(BASE+port,(value & 0xff00) >> 8 );
}

void disable_8254(unsigned int port)
{
    unsigned int control;
    control = 0x30 | ( (port==TIMER2) ? 0x80 : 0x40 );
    outp(BASE+0xF,control);
    outp(BASE+port,0x00);
    outp(BASE+port,0x00);
}

void interrupt irq5_isr(__CPPARGS)
{
    disable();
    irq_gen = 1;
    disable_8254(TIMER1);
    disable_8254(TIMER2);
}

```

```

    inp(BASE+3);          // clear irq
//  outp(0xa0,0x20); // re-enable 8259
    outp(0x20,0x20);
    enable();
}

void main(void)
{
    disable_8254(TIMER1);
    disable_8254(TIMER2);
    inp(BASE+3);          // clear previous irq
    old_irq5 = getvect(0x0d);
    setvect(0x0d, irq5_isr);
    outp(0x21, inp(0x21) & 0xdf);          // enable 8259
//  outp(0xa1, inp(0xa1) & 0xfb);

    do {
        irq_gen = 0;
        set_8254(TIMER1,0x3);
        set_8254(TIMER2,0xff);
        while(irq_gen==0);          // wait till irq happen
        printf("\n IRQ generate ... ");
    } while((getch()|32)!='q');
    setvect(0x0d, old_irq5);
    outp(0x21, inp(0x21) | 0x20);          // disable irq 5 interrupt
    getch();
}

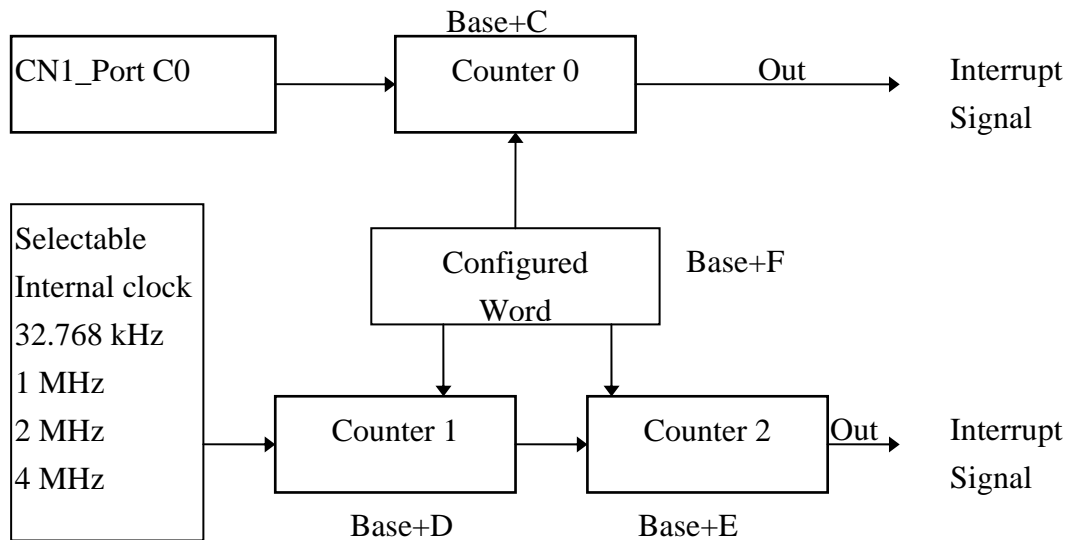
```

Demo program reference table

Function	Demo program
Event trigger	IRQ_EVNT.EXE
Timer trigger	IRQ_TIM.EXE
CN1_PC3 direct trigger	IRQ_PC3F.EXE
CN1_PC3 & PC7 direct trigger	IRQ_PC37.EXE
CN2_PC3 direct trigger	IRQ_PF3F.EXE
CN2_PC3 & PC7 direct trigger	IRQ_PF37.EXE
Soft trigger	IRQ_SOFT.EXE

6.4. 8254 Timer / Counter

The 8254 programmable timer / counter has 4 registers, it occupies 4 I/O address from Base + C through Base + F. for detail programming information about 8254. Please refer to Intel's "Microsystem Components Handbook".



Register	Function
Base+C	LSB or MSB of Counter 0
Base+D	LSB or MSB of Counter 1
Base+E	LSB or MSB of Counter 2
Base+F	Configured Word

Configured Word

Bit	7	6	5	4	3	2	1	0
	CS1	CS0	RW1	RW0	M2	M1	M0	BCD

● **CS1,CS0 : Counter Select**

CS1	CS0	Counter
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Illegal

● **RW1 , RW0 : Read / Write operation**

RW1	RW0	Operation
0	0	Counter Latch
0	1	Read/Write LSB
1	0	Read/Write MSB
1	1	Read/Write LSB First then MSB

● **M2, M1 & M0-Select Operating Mode**

M2	M1	M0	Mode
0	0	0	Interrupt Terminal Count
0	0	1	Programmable One-Shot
0	1	0	Rate Generator
0	1	1	Square Wave Rate Generator
1	0	0	Software Triggered Strobe
1	0	1	Hardware Triggered Strobe

● **BCD : Select Binary / BCD counting**

BCD	Counting
0	Binary Counter 16 bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Program :

```

BASE=0x2c0;
outp(BASE+0x0F, 0x36); /* Configured Word : Counter 0 , Read/Write LSB
                        then MSB , Square Wave Rate Generator
                        Mode , Binary Counter 16 bit */
outp(BASE+0x0C, 0xff); /* Write Counter 0 LSB */
outp(BASE+0x0C, 0x10); /* Write Counter 0 MSB */

```

7. Daughter Board

The DIO-48 offers two 50 pin Opto-22 connector which can be connected to daughter board, such as :

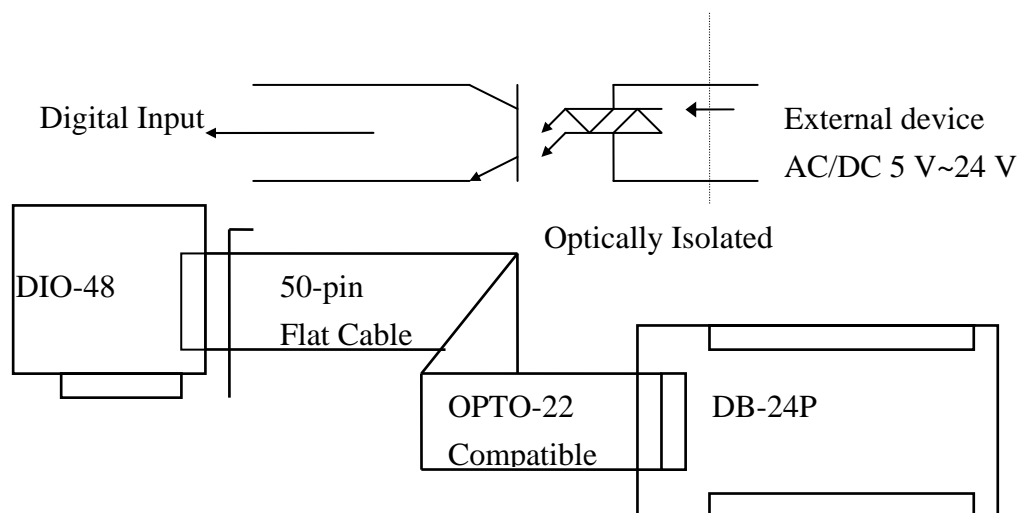
1. DB-24P 24 Opto-isolated Digital Input Terminal Board
2. DB-24R 24 Relay Output Board
3. DB-24PR 24 Power Relay Output Board

7.1 DB-24P (Isolated Input board)

The DB-24P is a 24 Opto-isolated Digital input terminal board.

Features:

- 24 optically isolated digital input channels
- AC/DC signal Input
- AC Signal Input with filter
- Input buffer with voltage comparators.
- Maximum input voltage : 24 V_{DC} or 24 V_{AC}.
- Board Dimension : 8.66"(220 mm) X 5.20" (132 mm)



7.2 DB-24R (Relay Board)

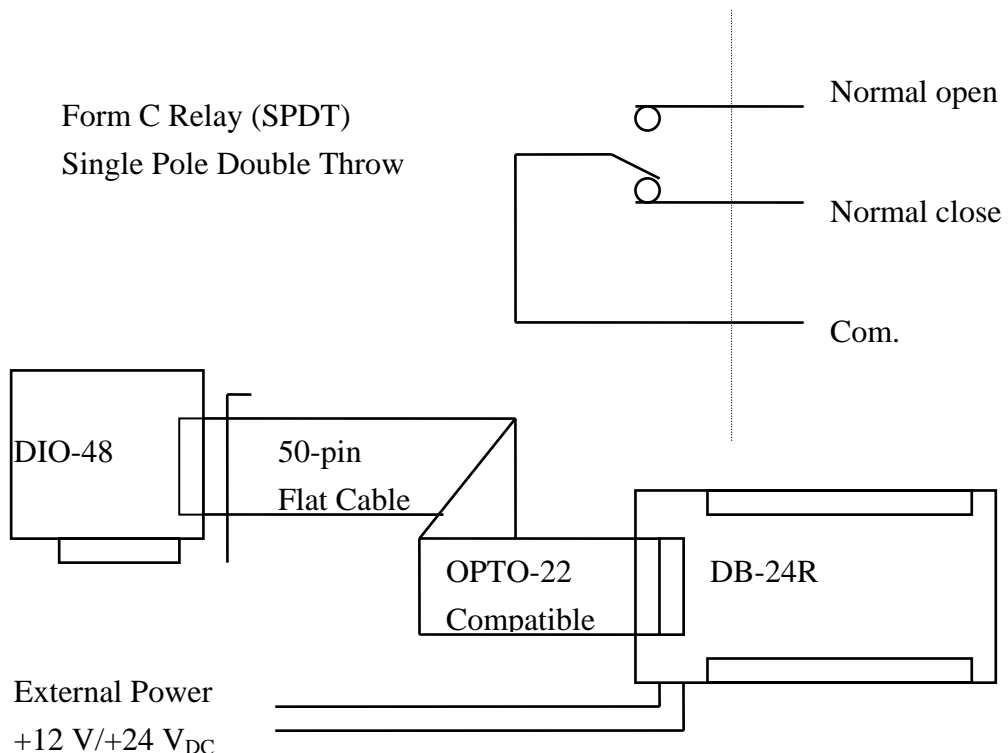
The DB-24 is a 24 channel relay output board

Features

- 24 Form C Relays
- Switch up to 1 A at 30 V_{DC} or 110 V_{AC}
- LEDs indicated relay status
- Screw terminals for easy field wiring

Order information:

- DB-24R/12 V 24 Channel Relay output Board (Coil Voltage : 12 V_{DC})
- DB-24R/24 V 24 Channel Relay output Board (Coil Voltage : 24 V_{DC})



7.3 DB-24PR (Power Relay Board)

The DB-24PR is 24 Channel Power Relay output Board.

Specification:

- 16 Form A Relays (SPST) and 8 form C Relays (SPDT)
- Switch up to 5 A at 250 V_{AC} or 30 V_{DC}
- Building varistor to protect each channel's high voltage spike.
- LED indicate relay status
- Screw terminals for easy field wiring

Order Information:

- DB-24PR/12 V : 24 Channel 5 A/250 V_{AC} Relay Board / 12 V Coil Voltage Version
- DB-24PR/24 V : 24 Channel 5 A/250 V_{AC} Relay Board / 24 V Coil Voltage Version

